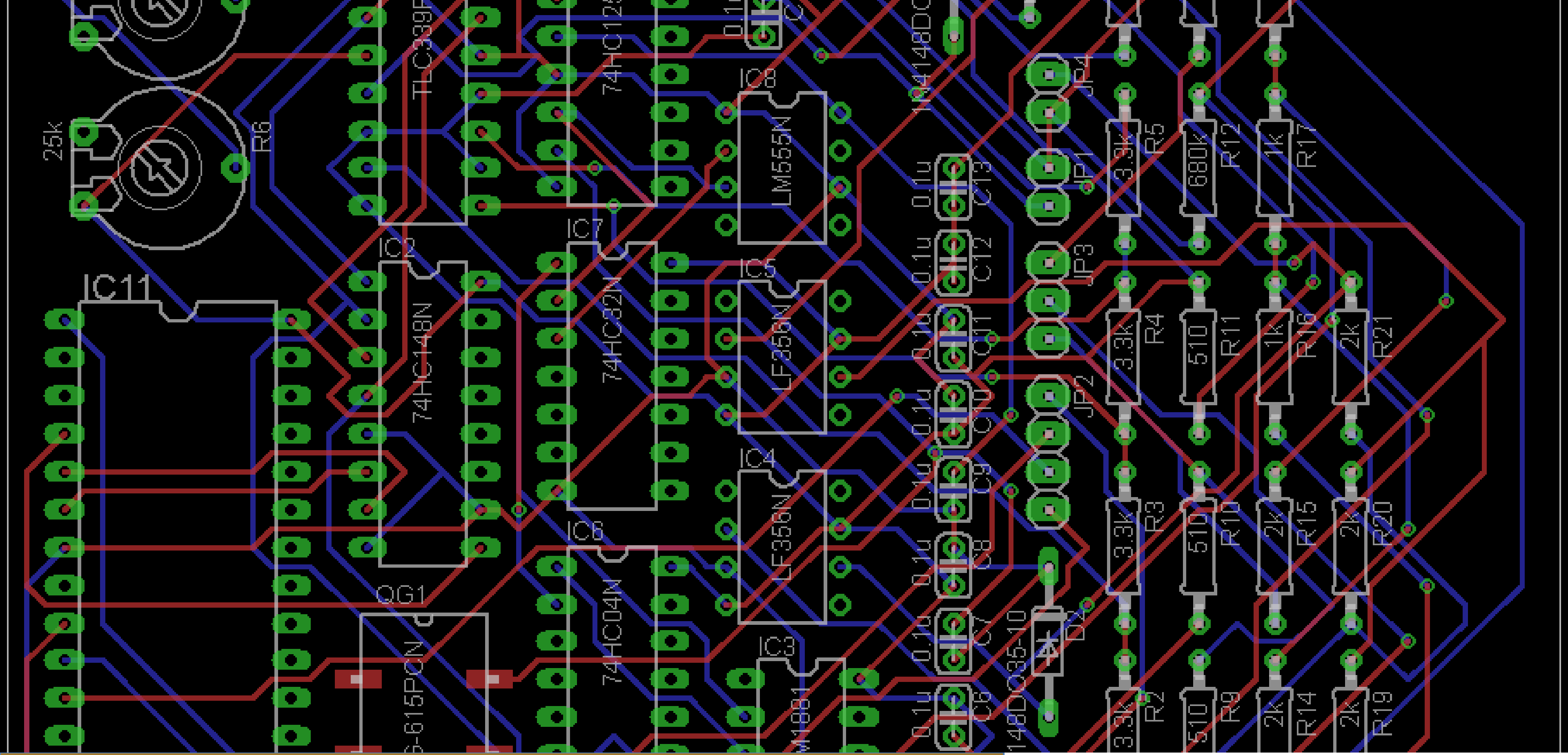


CASE STUDY:
HARDWARE SOS

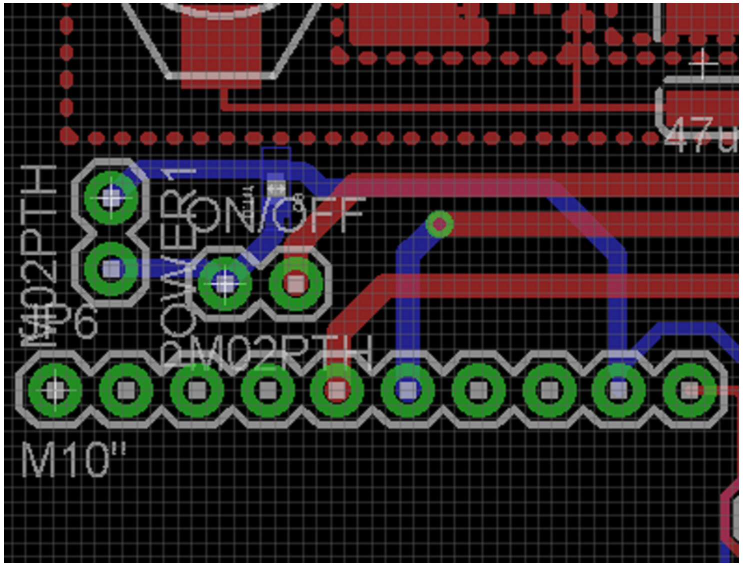
OUTLINE

- Parts Completion Check
- Footprint Verification Check
- Parts Placement Check
- Space Conflicts Check
- Routing Completion Check
- Routing Minimization Check
- Via Minimization Check
- Signal Plane Check
- Silkscreen Check

PARTS COMPLETION CHECK

Values and Ratings of Passive Components

- When choosing passive components, both component value and power/voltage ratings matter
- Consider: How much current is running through your resistors? How much voltage is being dropped across your capacitors?

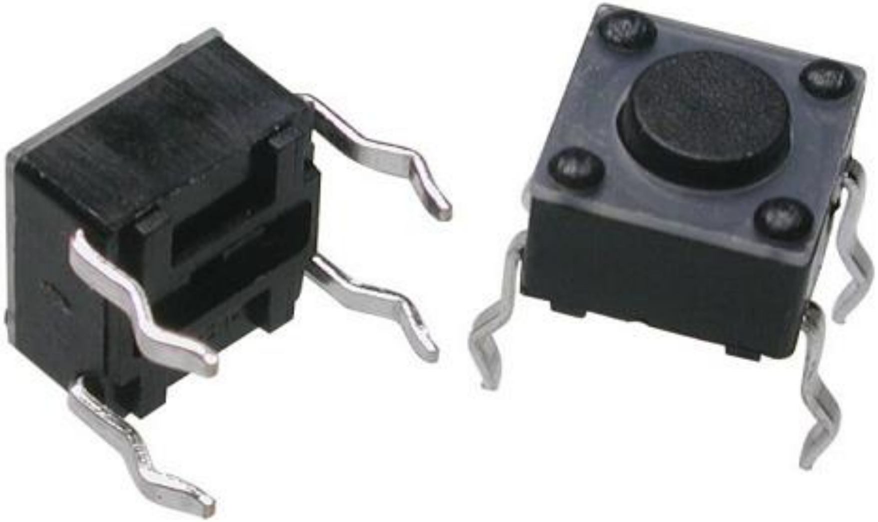


Which of these resistor packages is more likely to survive having 4 amps run through it?

PARTS COMPLETION CHECK

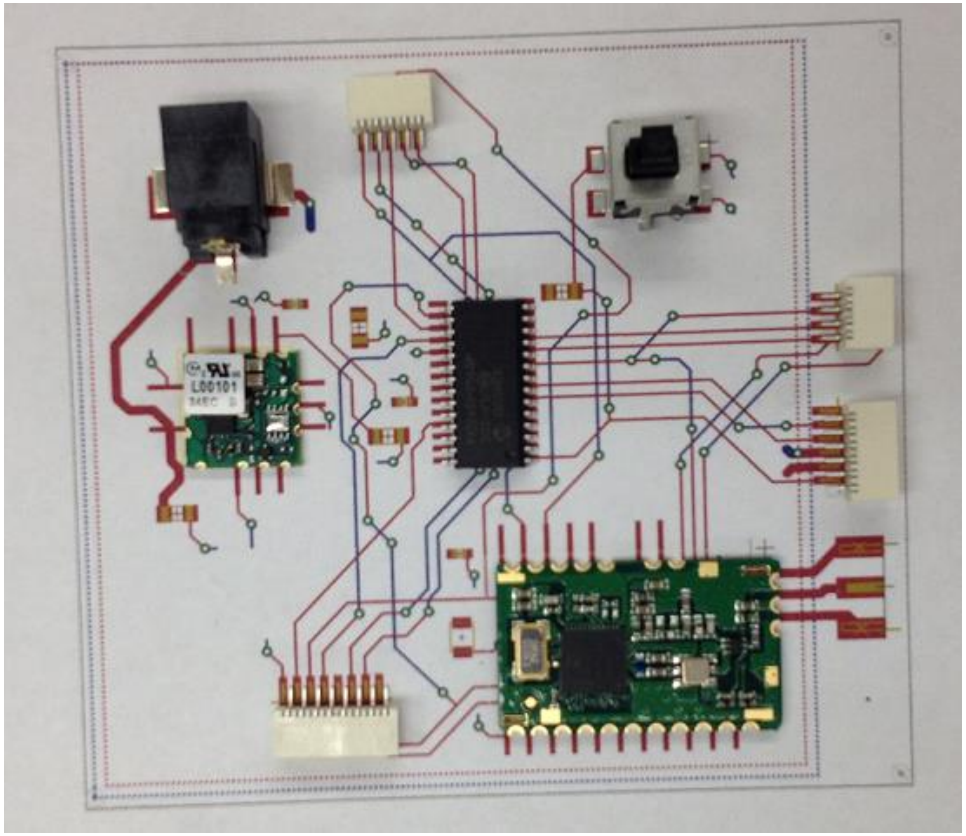
Miscellaneous PCB Components

- Does your board have…
  - A programming header? (note: use of an RJ-11 connector is not required)
  - Reset tactile switch? (tact switches are recommended over pushbuttons and other button types)
  - A power connector and LED?
  - Mounting holes?
  - Debugging support?



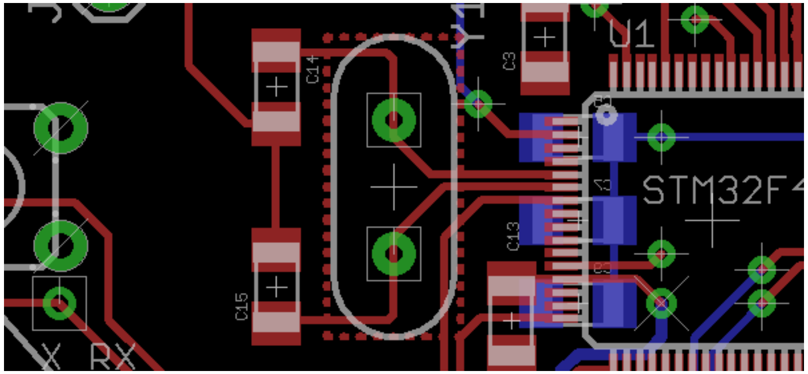
FOOTPRINT VERIFICATION CHECK

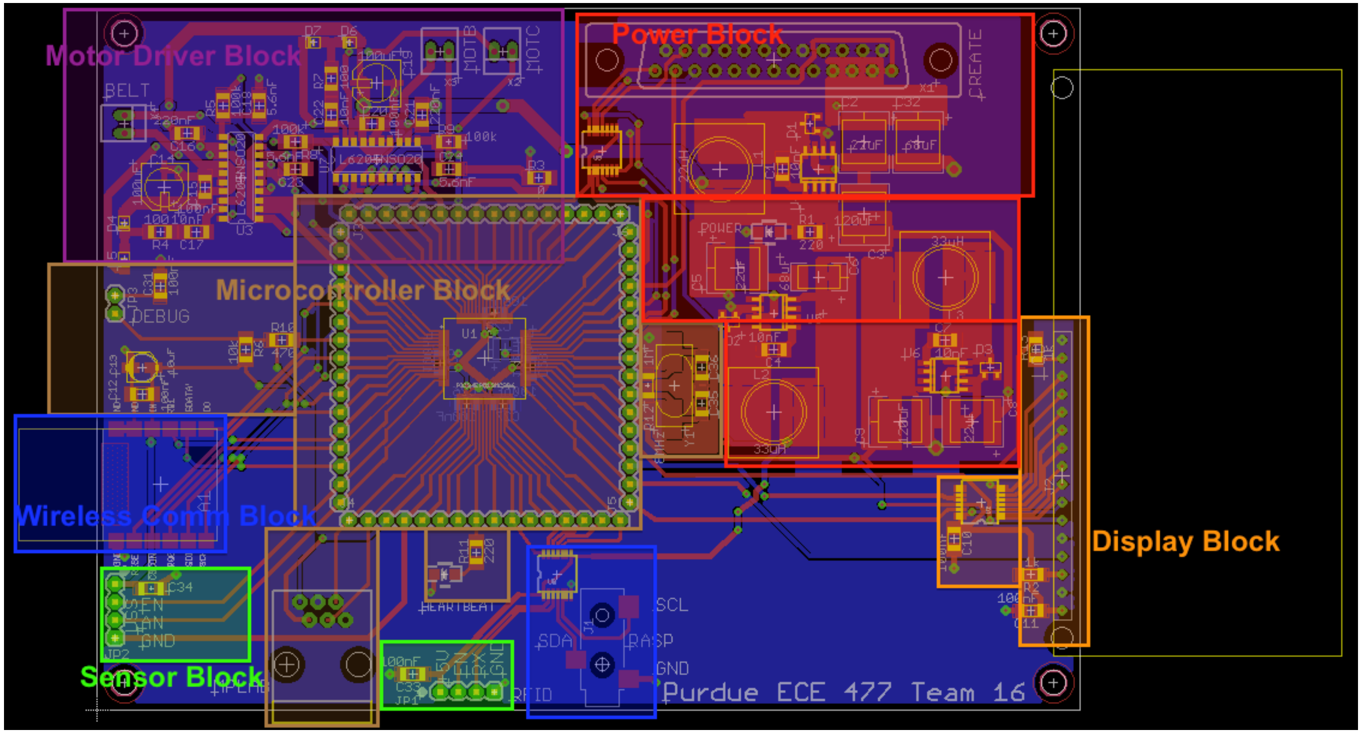
- Print a 1:1 scale layout of your board and lay your parts on the printout to ensure that layout footprints match the actual component packages
- Board doesn’t have to be fully routed; what matters is that you have at least 1 instance of every unique PCB footprint on the printout to compare against physical parts



PARTS PLACEMENT CHECK

- Is your crystal physically close to your microcontroller?
- Are decoupling capacitors near/under microcontroller?
- Have connectors been placed at board edges?
- Are parts grouped by system or a logical order that minimizes trace lengths?



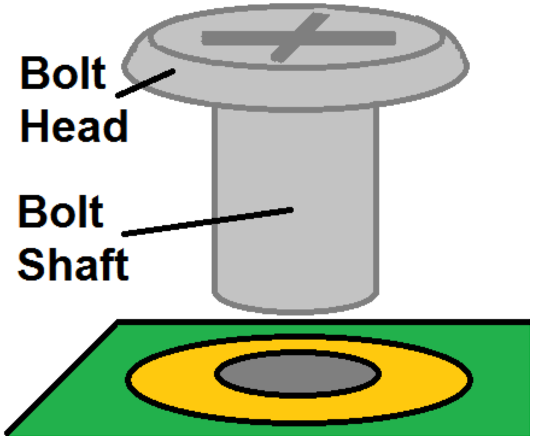


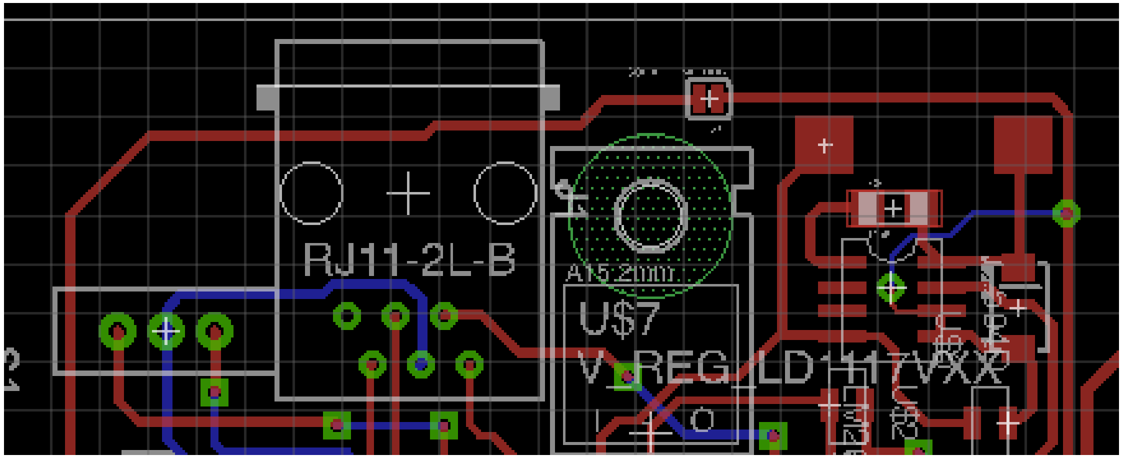
PURDUE
UNIVERSITY

MECHANICAL CHECK

X/Y-Space Conflicts

- Will your parts sit flush with the board? Has clearance been provided for the X/Y space around your parts?
- For your mounting holes, has clearance been provided for the heads of the bolts in addition to the bolt shaft?
- Best remedy to avoid these types of conflicts is to place an outline of the part in the documentation layer





MECHANICAL CHECK

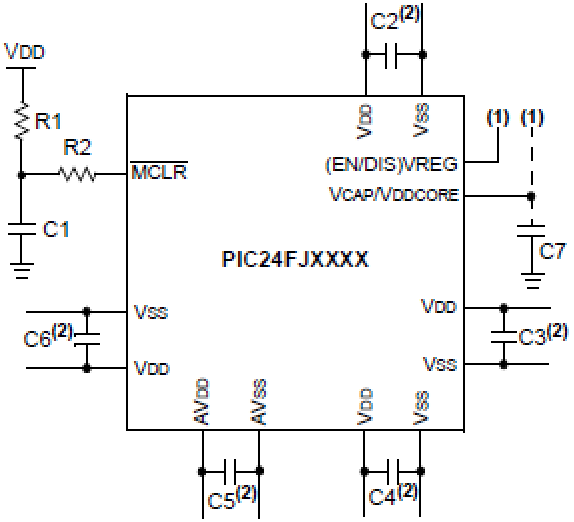
Z-Space Conflicts

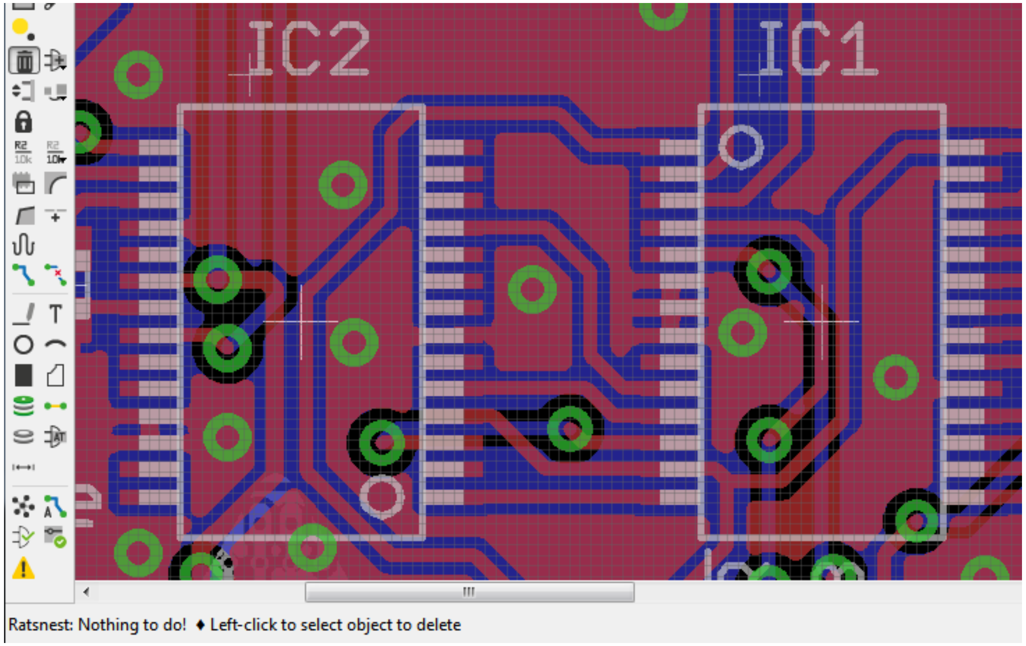
- When students add breakout boards, RPis/Atom Boards, utilize stacked PCB design, or have special packaging constraints, the height of components becomes important. If components are too tall, they may run into and/or create a short circuit with another board
- Best remedy to avoid these types of conflicts is to place an outline of the part in the documentation layer (so you know when to check for height concerns)

ROUTING CHECKS

Routing Completion Check

- Have all airwires been resolved? (If so, the Eagle ratsnest command should report “Nothing to Do”)
- Have you separated AGND from GND using a jumper, SMD resistor, or as suggested in your microcontroller connection guidelines?



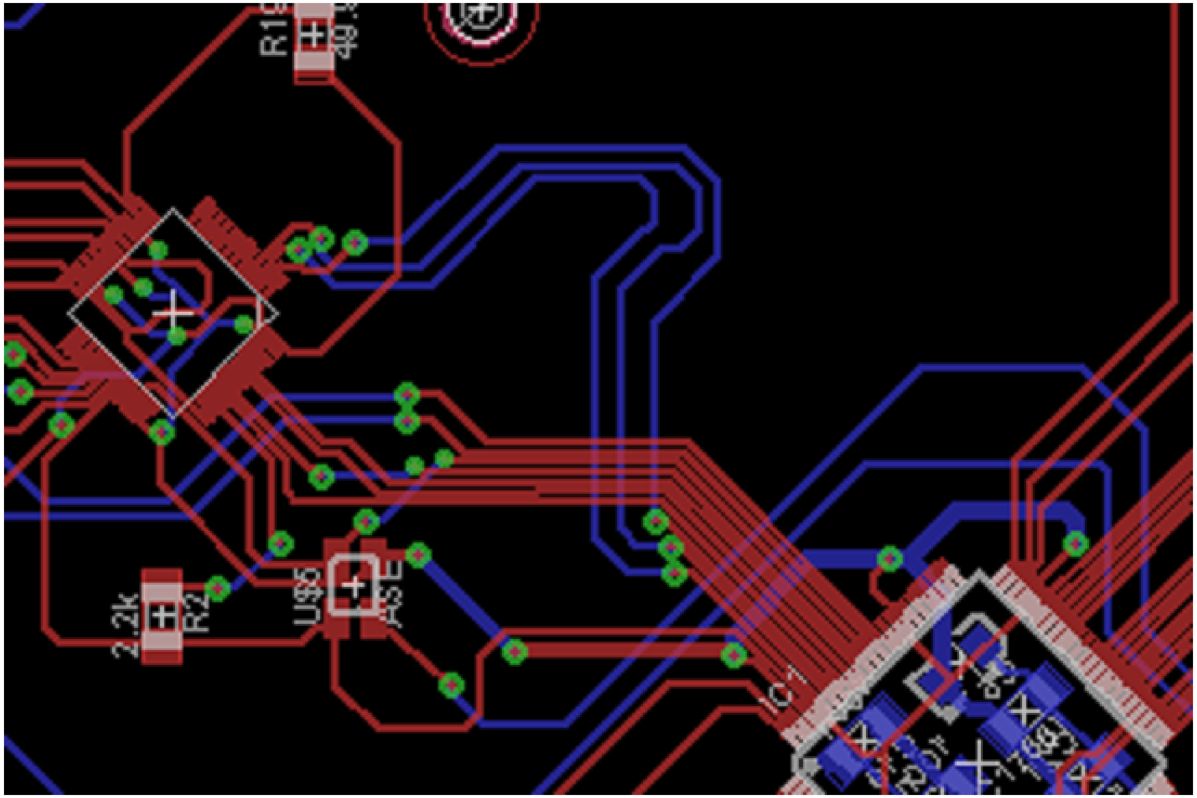


Ratsnest: Nothing to do! ♦ Left-click to select object to delete

ROUTING CHECKS

Trace Length Minimization Check

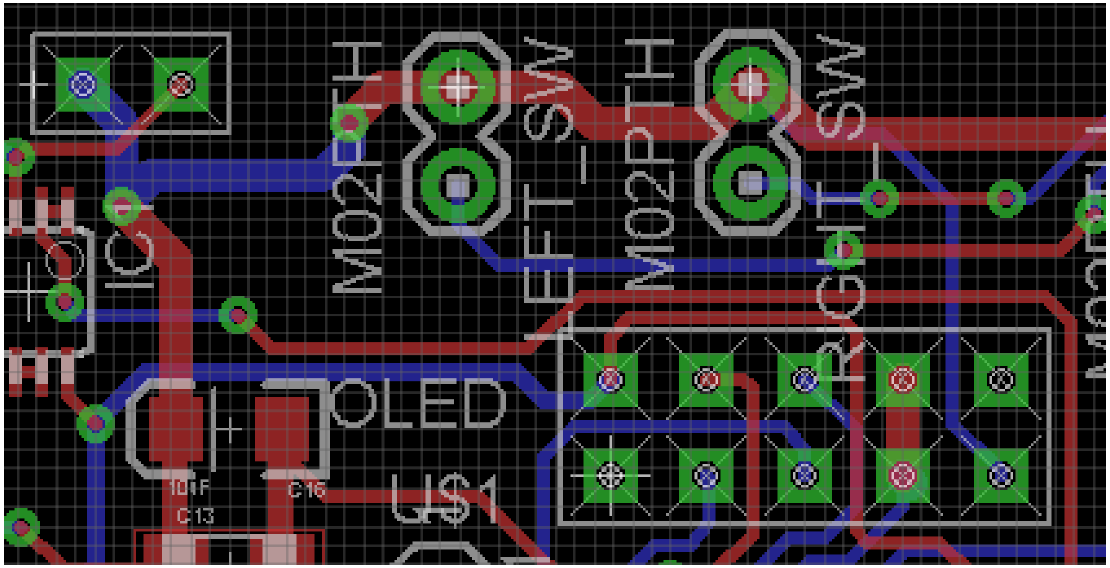
- Have unnecessary right angles been removed?
- Have PCB trace bends, loops, and spurs been removed? (Loops function like antennae at high frequencies)
- Has octagonal routing mode been used? ("Anything-goes" diagonal routing mode is not recommended for designs)



ROUTING CHECKS

Via Minimization Check

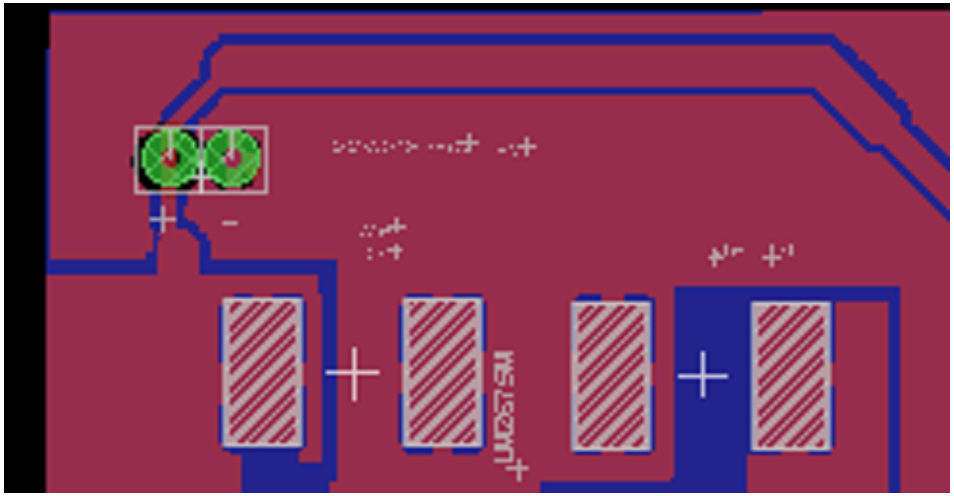
- Have unnecessary vias been removed?
- Remember: you can enter through-hole pins from either the top or bottom layers, just like vias
- Remember: you can route standard ~10 mil signal traces between pairs of 0.1” spaced through-holes without violating clearance requirements
- Remember: you can route into a pin/pad from any direction, including behind it

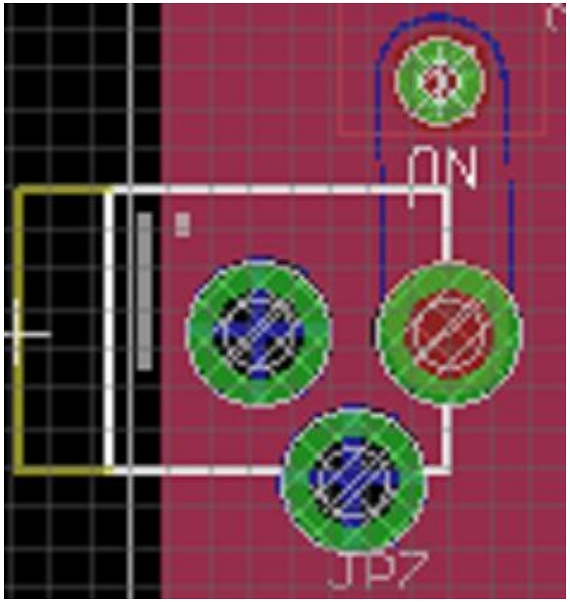


ROUTING CHECKS

Trace/Via Current Capacity Check

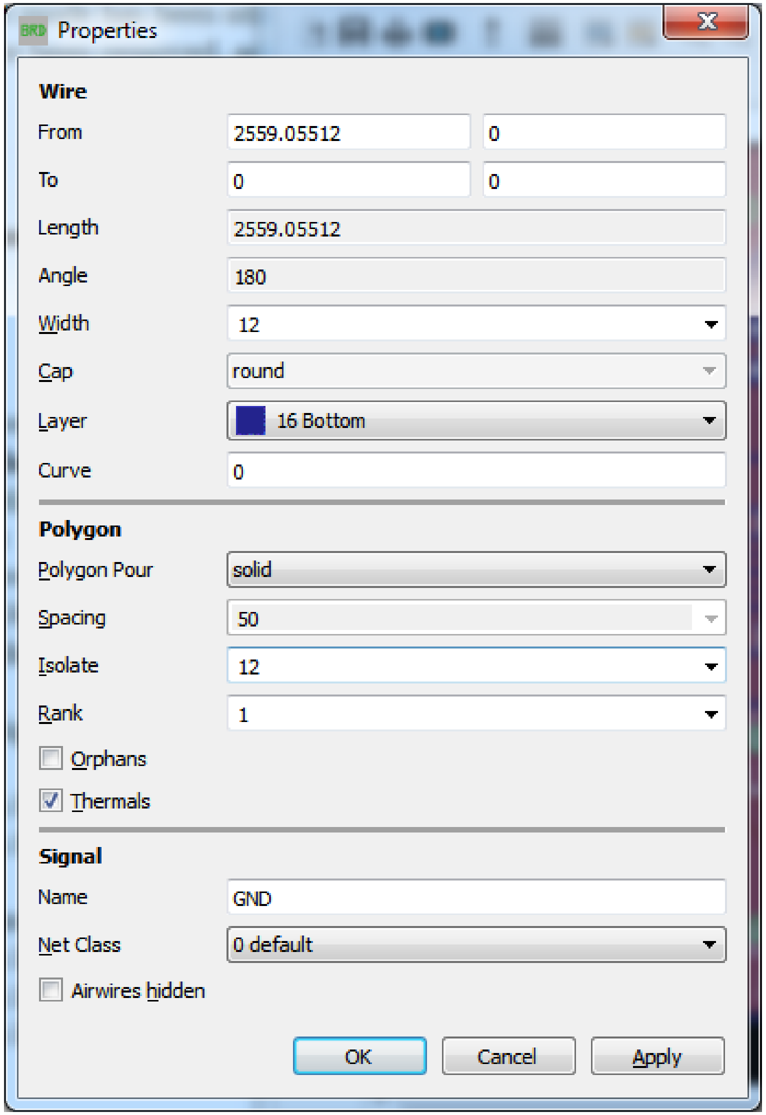
- Have traces been sized appropriately to the amount of current they are carrying? (32 mils or greater is recommended; consult trace width calculators for situations involving large amounts of current)
- Have vias in high-current traces been sized appropriately to match the trace width?





SIGNAL PLANE CHECKS

- Are signal planes being used where appropriate?
- Has the isolation on all signal planes been set to an appropriate value? (Eagle currently defaults isolation to 0; signal plane isolation of 12 mils or greater is STRONGLY recommended).



Wire

From: 2559.05512, 0
To: 0, 0
Length: 2559.05512
Angle: 180
Width: 12
Cap: round
Layer: 16 Bottom
Curve: 0

Polygon

Polygon Pour: solid
Spacing: 50
Isolate: 12
Rank: 1
☐ Orphans
☑ Thermals

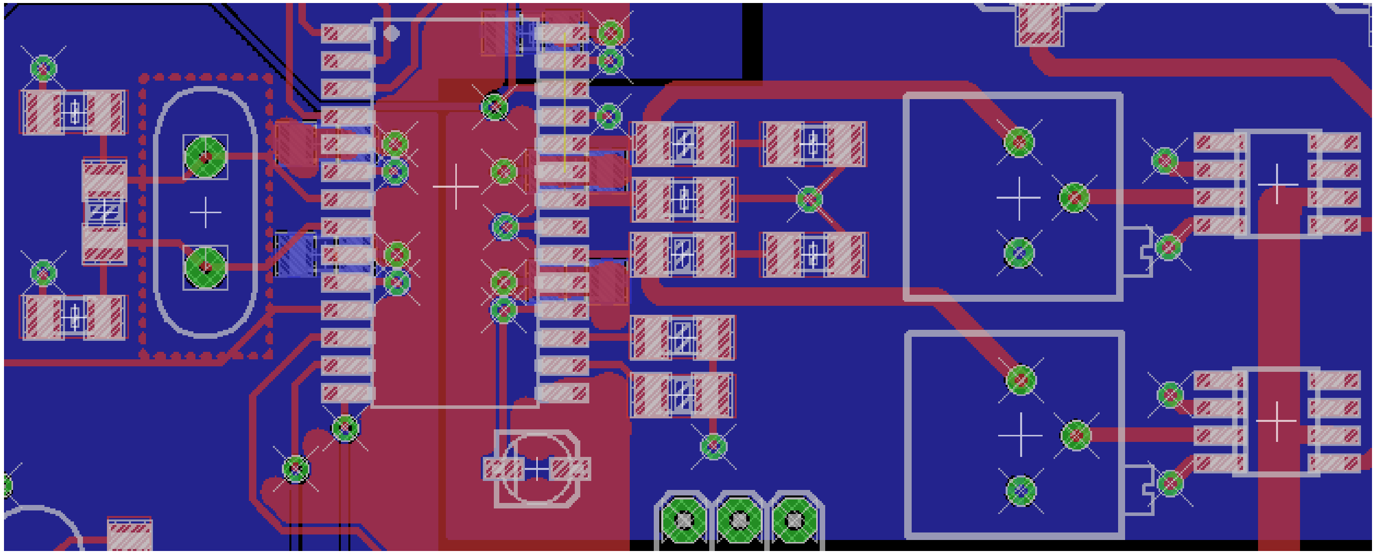
Signal

Name: GND
Net Class: 0 default
☐ Airwires hidden

PURDUE
UNIVERSITY

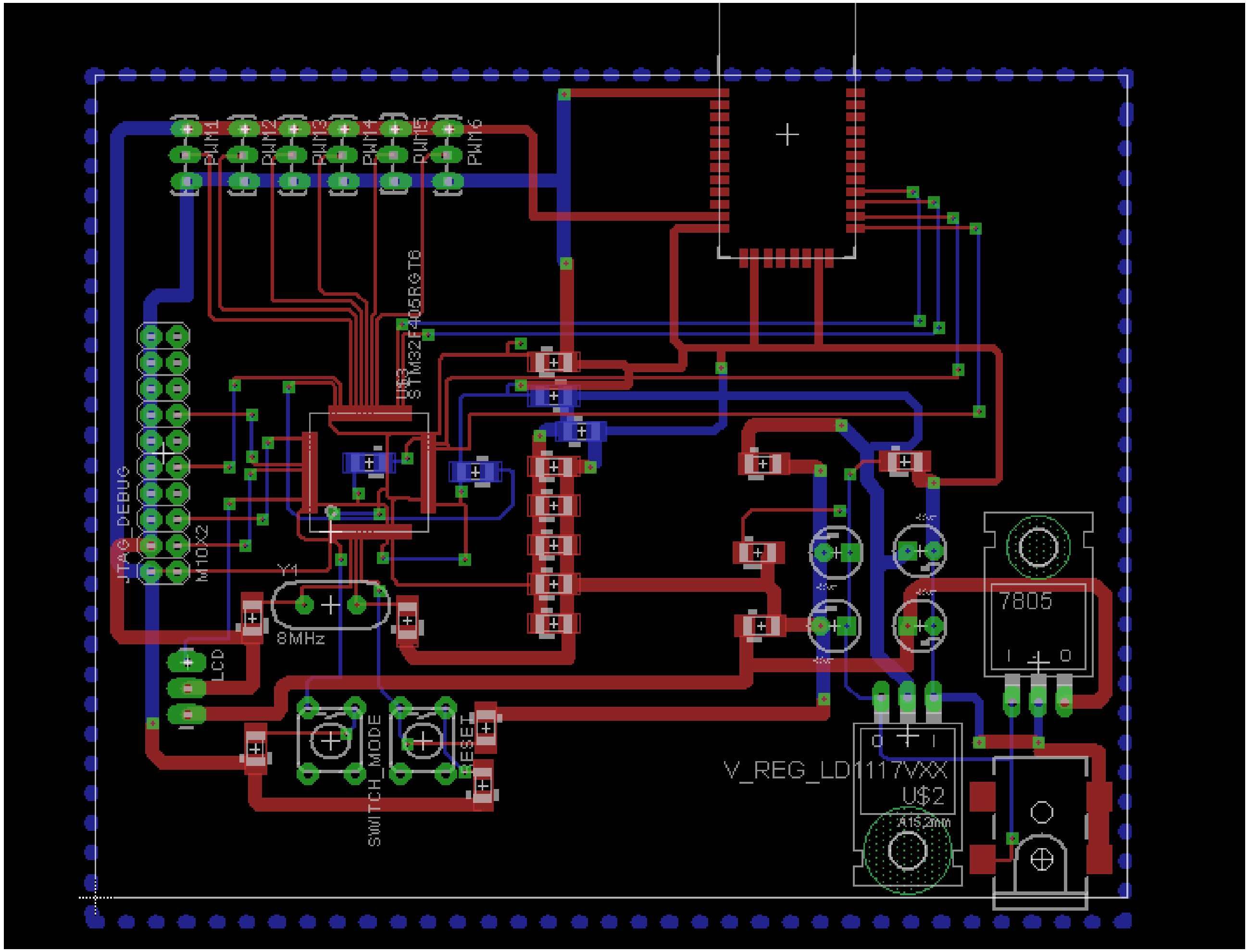
SILKSCREEN CHECKS

- Have labels been provided (in either the name or silkscreen layers) for all component IDs and appropriate connector signal names?
- Is pin 1 of all polarity-sensitive ICs and passives clearly marked?
- Have all silkscreen labels been positioned so as to not overlap pins, pads, or anywhere else that solder will be applied?



PCB LAYOUT IMPROVEMENTS

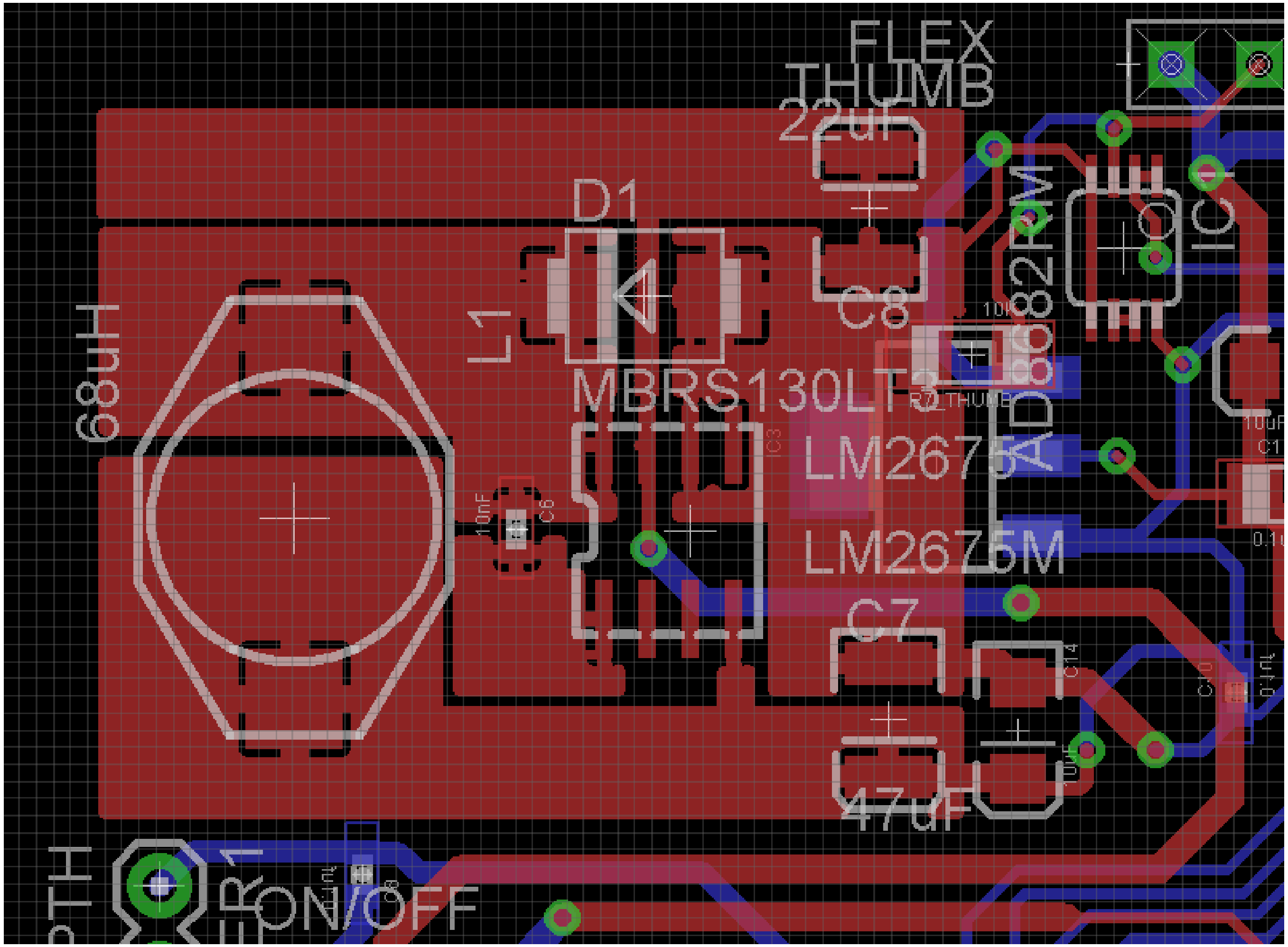
- What's good about this layout? What could be improved?



PURDUE
UNIVERSITY

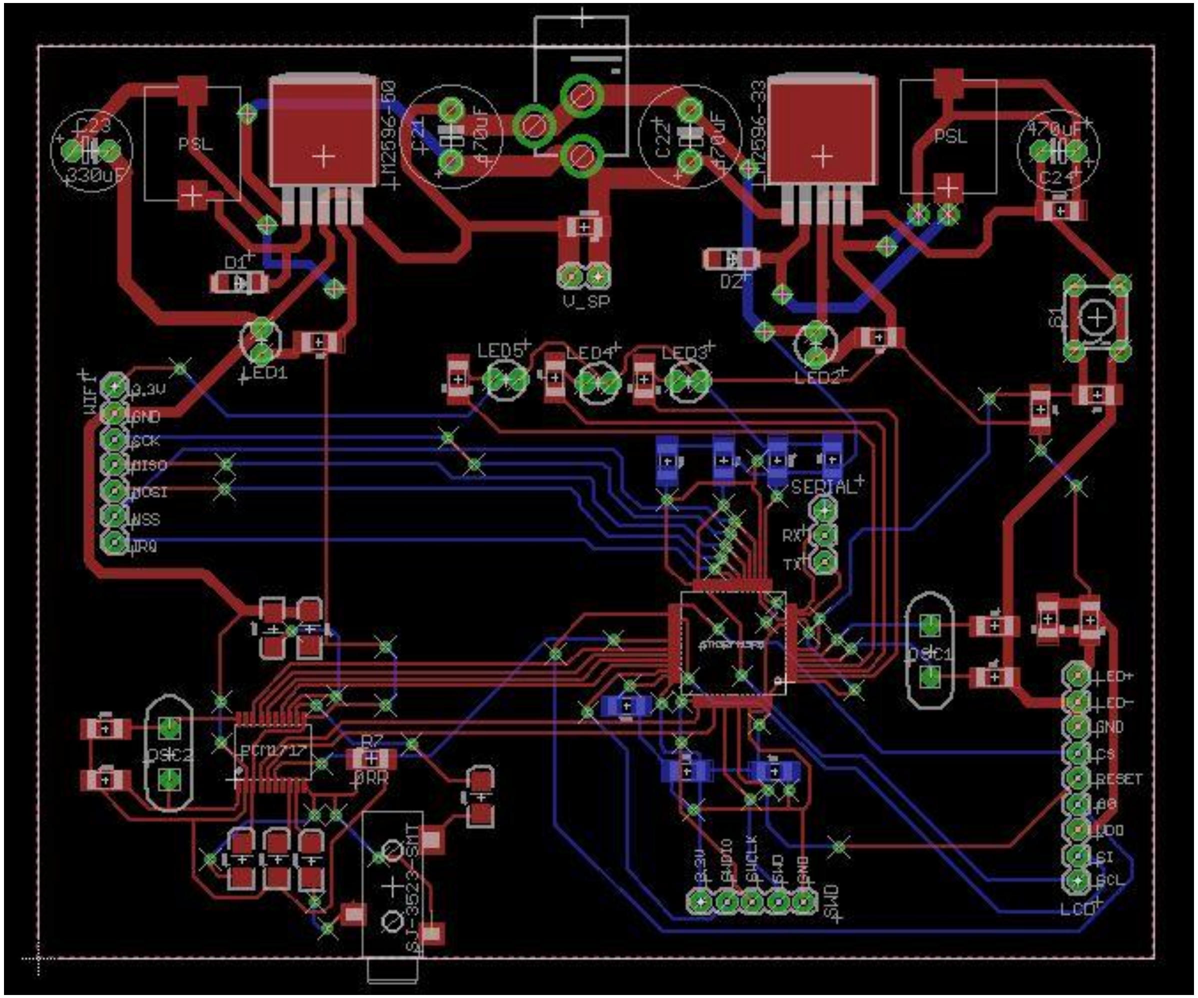
PCB LAYOUT IMPROVEMENTS

- What’s good about this layout? What could be improved?



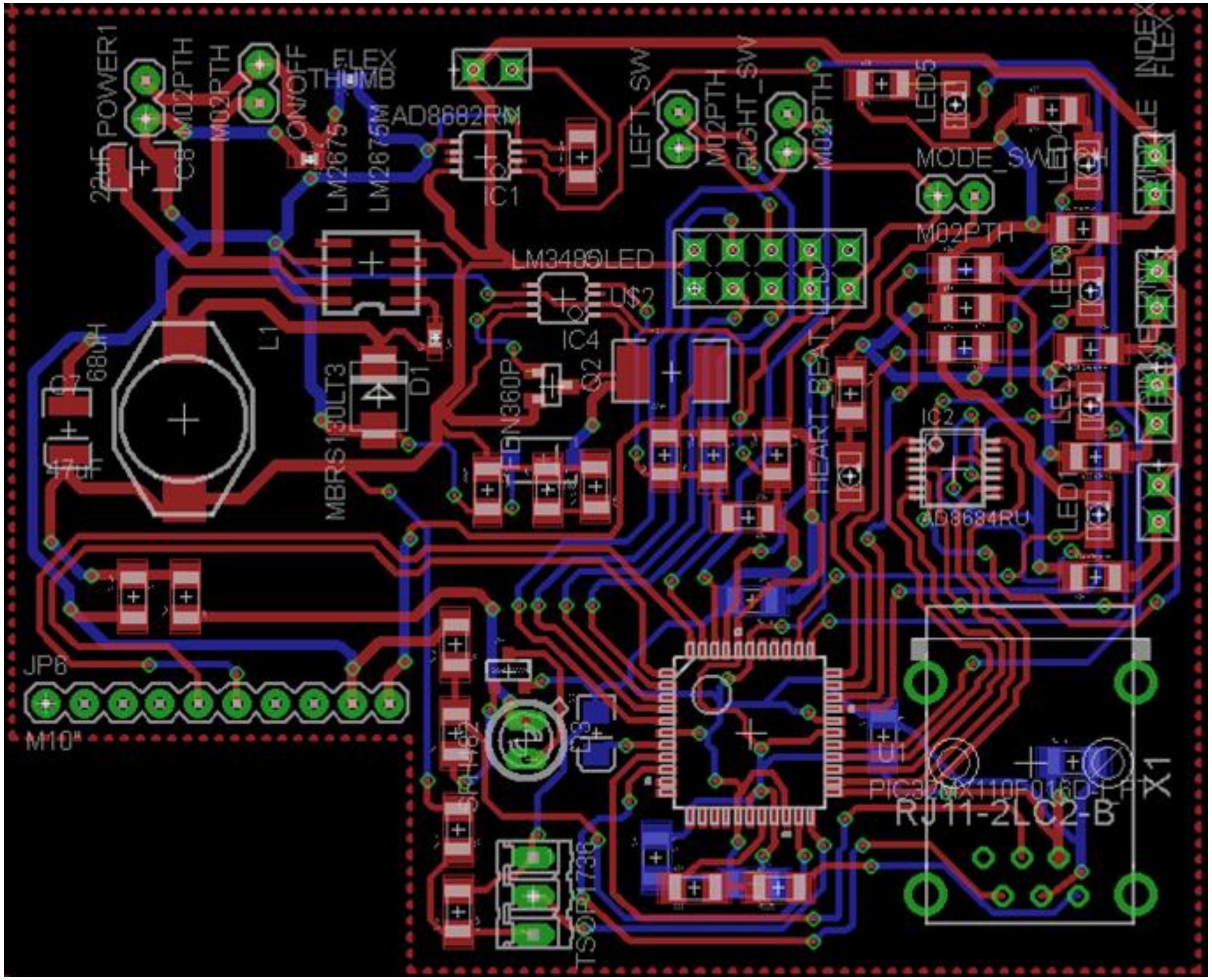
PCB LAYOUT IMPROVEMENTS

- What's good about this layout? What could be improved?



PCB LAYOUT IMPROVEMENTS

- What's good about this layout? What could be improved?



PCB LAYOUT IMPROVEMENTS

- What's good about this layout? What could be improved?