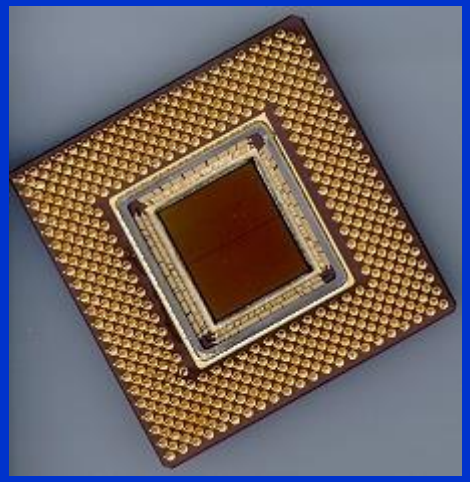
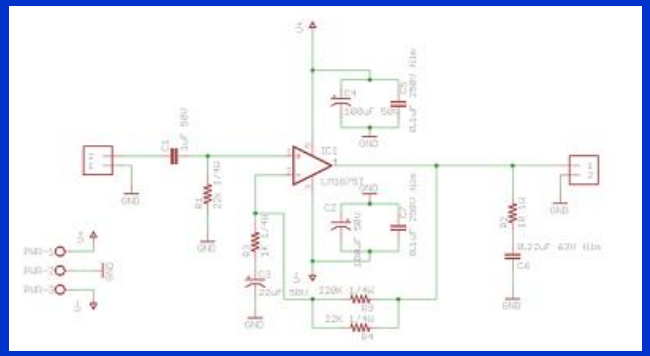


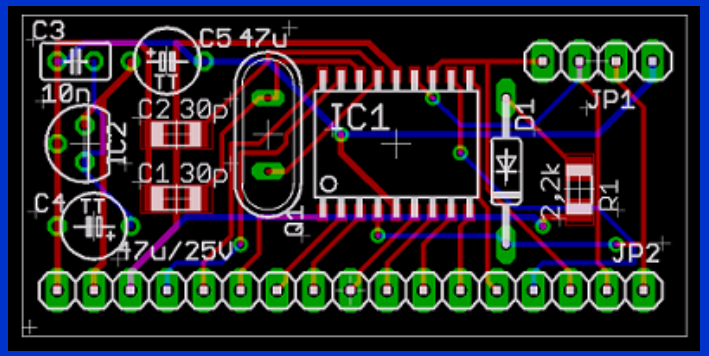
ECE 477 Digital Systems
Senior Design Project

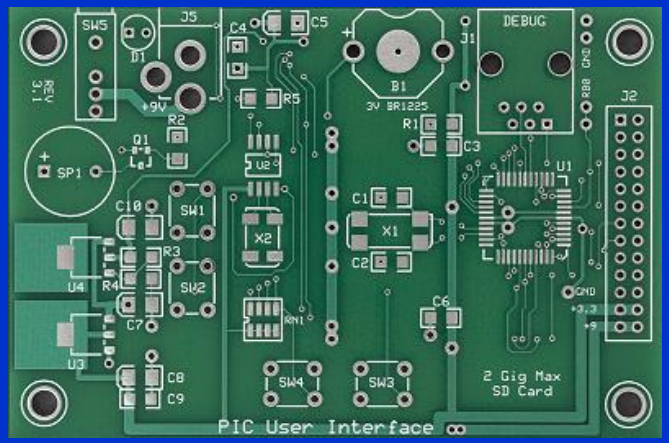
Module 3
PCB Fabrication and Layout

Overview

- **Objective:** To understand what printed circuit boards are, how they are created, and basic guidelines on PCB design





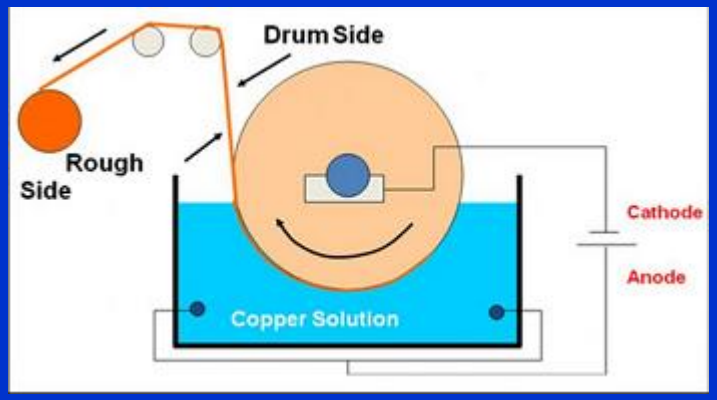


Anatomy of a PCB

- **Quick overview:**
  - **Copper foil**
  - **Substrate**
  - **Lamination**
  - **Etch**
  - **Drill**
  - **Plate**
  - **Solder mask**
  - **Silkscreen**

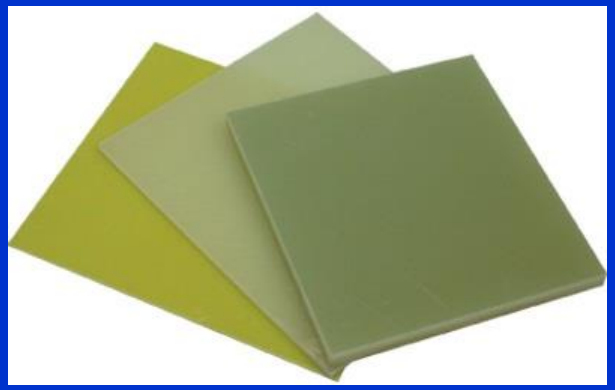
Anatomy of a PCB

- **Copper foil**
  - **electro-plated onto a large drum then scraped off (typical)**
  - **one side very smooth, one rough**



Anatomy of a PCB

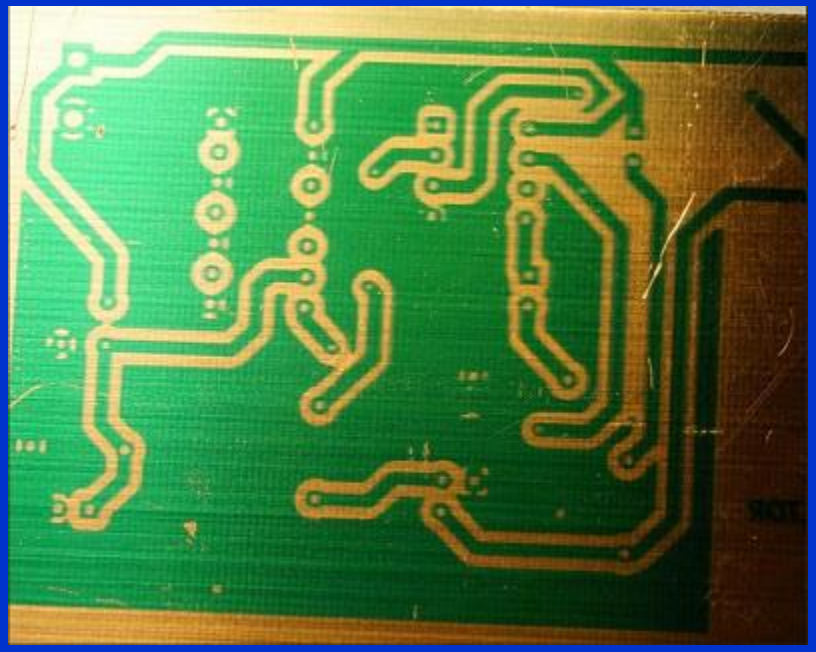
- **Substrate**
  - **FR4 (fiberglass reinforced multi-functional epoxy)**
  - **others: FR2**



- **Lamination**
  - **copper foil applied to both sides of laminate and then bonded using heat and pressure**

Anatomy of a PCB (3/8)

- **Etching**
  - **Circuit first realized here**
  - **Etch-resist applied, pattern is exposed**

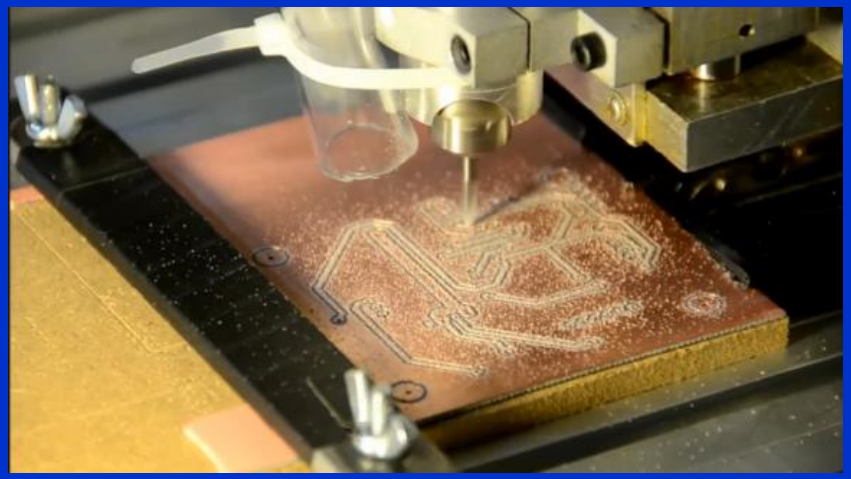


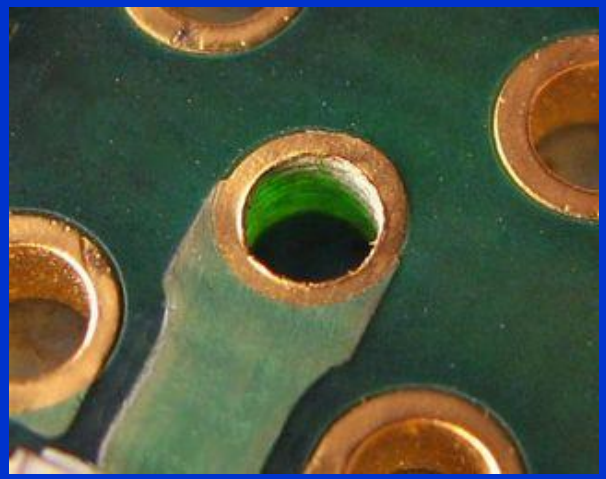
Anatomy of a PCB

- **Etching**
  - **Uncured resist is washed off and then the pattern is etched**
  - **common etchants: FeCl, Ammonia**
  - **solvent/abrasive wash to remove etch-resist**
  - **PCB then washed to remove residues from solvents and abrasive process**

Anatomy of a PCB

- **Drill / Plate**
  - **This is how the connections are made between layers**
  - **Holes drilled through where connections are desired**



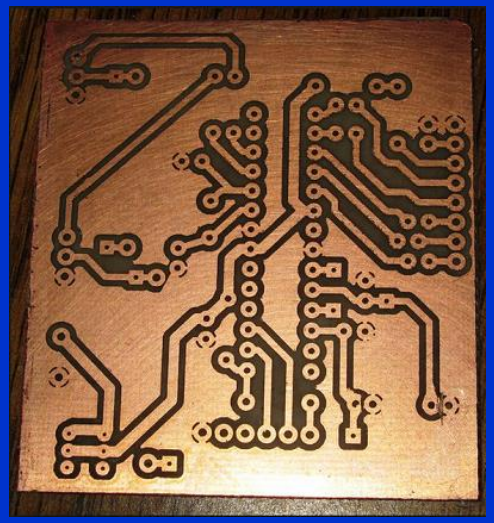


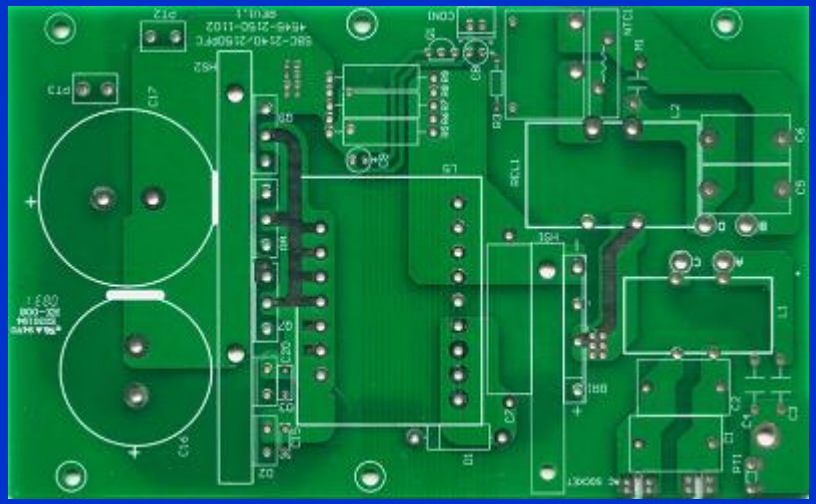
Anatomy of a PCB

- **Drill / Plate**
  - **PCB then immersed in a plating solution where a thin layer of copper forms inside the barrel of the hole**
  - **Once enough copper is deposited this way, then on to electro-plating, where ~1 mil of copper is plated on**
  - **If a gold-plate finish is required, typically applied at this time**

Anatomy of a PCB

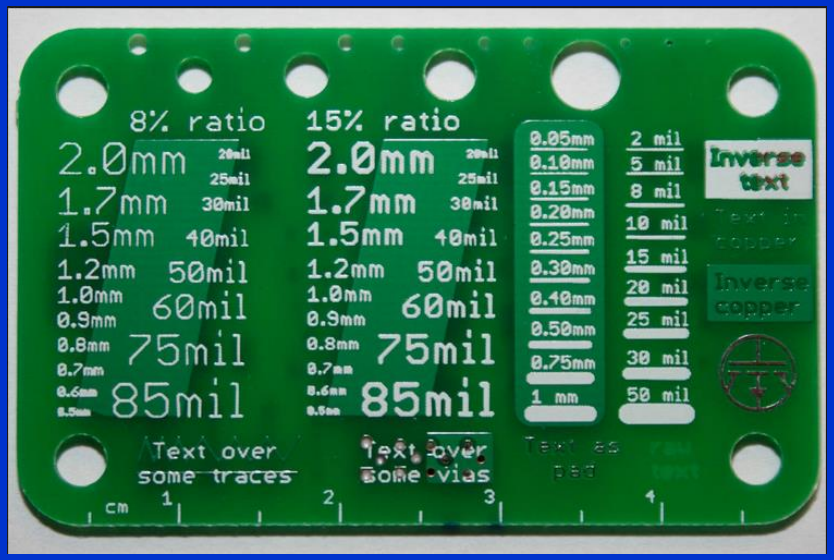
- **Solder mask**
  - **Protects metal from corrosion, short circuits**
  - **Also prevents solder from sticking**
  - **applied as a liquid, then cured with UV**
  - **Many colors available, green most common**





Anatomy of a PCB

- **Silkscreen (legend)**
  - **labels everything: components, notes, warnings, logos**
  - **similar process to making T-shirts**
  - **applied as a liquid, then cured**
  - **several colors, white most common**



PCB Terminology

- **Pin – A plated through hole used to connect the terminal of a part**
- **Pad – A flat conductive surface for connecting the terminal of a part**
- **Via – A plated through hole used for signal routing**
- **Trace – A wire or 1 dimensional electrical connection**
- **Signal Plane – A 2 dimensional electrical connection (commonly used for ground)**

Typical PCB fabrication tolerances

- **Notation: 1 mil = 1 “milli-inch” = 0.001 in.**

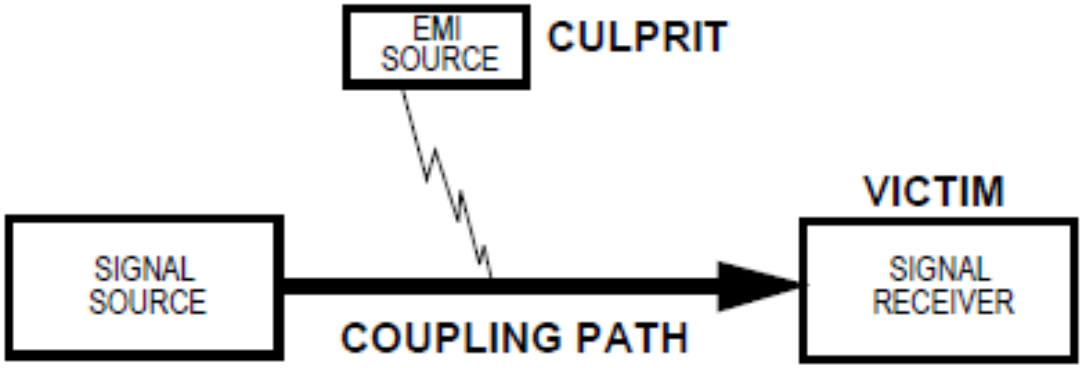
- **Drills: +5/-3 mils diameter, 5 mil center**
  - **smallest drill size 20 mil**
- **Layer-to-layer alignment: +/- 3 mils**
- **Etched feature size: +/- 1 mil**
  - **Trace size (isolate): 6 mil**
  - **≥ 8 mil trace/isolate recommended**
- **Solder mask size: +/- 3 mil**
- **Silkscreen size: +/- 10 mil**

Basic Layout Guidelines

- **Minimum recommended trace/space 10-12 mil**
- **Power and ground traces should be sized for current being passed (width/current charts available online)**
- **Follow all manufacturer layout recommendations**
- **Decoupling capacitors should be placed *as close to each IC as possible***
- **Provide *space* and *mechanical support* for connectors, heat sinks, and standoffs (used for mounting board)**
- **Incorporate *headers* or vias for verification and debugging**

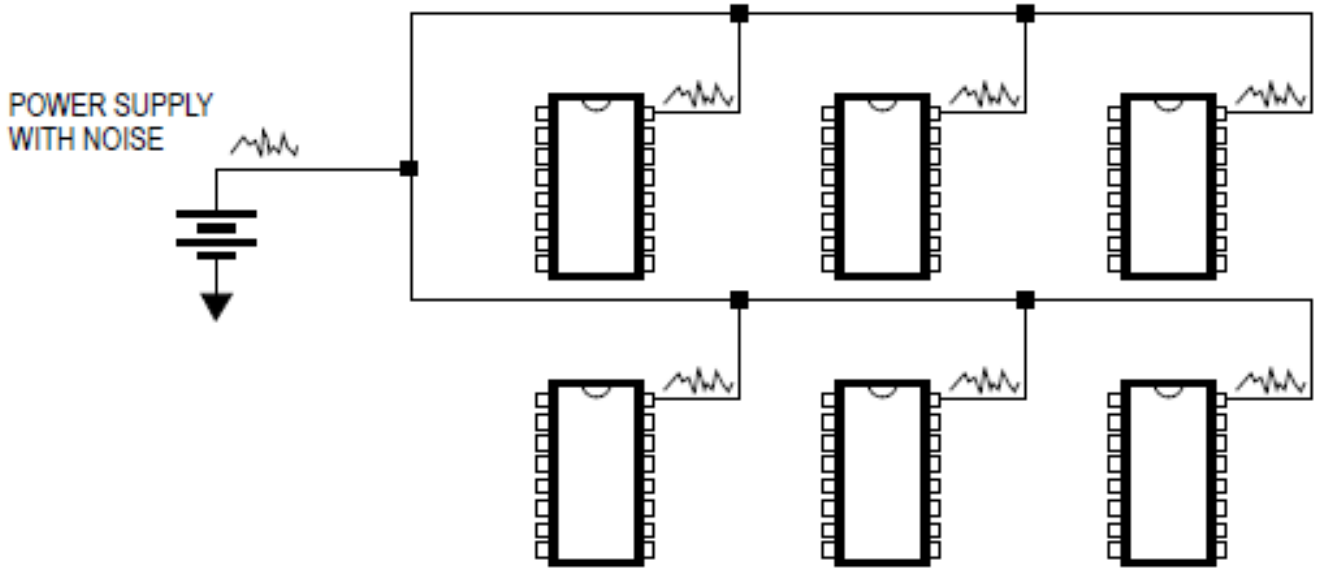
EMI Considerations

- **Source of EMI include microcontrollers, electrostatic discharges, transmitters, transient power components, AC supplies, and lightning**
- **Within a microcontroller system, the digital clock circuitry is usually the biggest generator of wide-band noise**



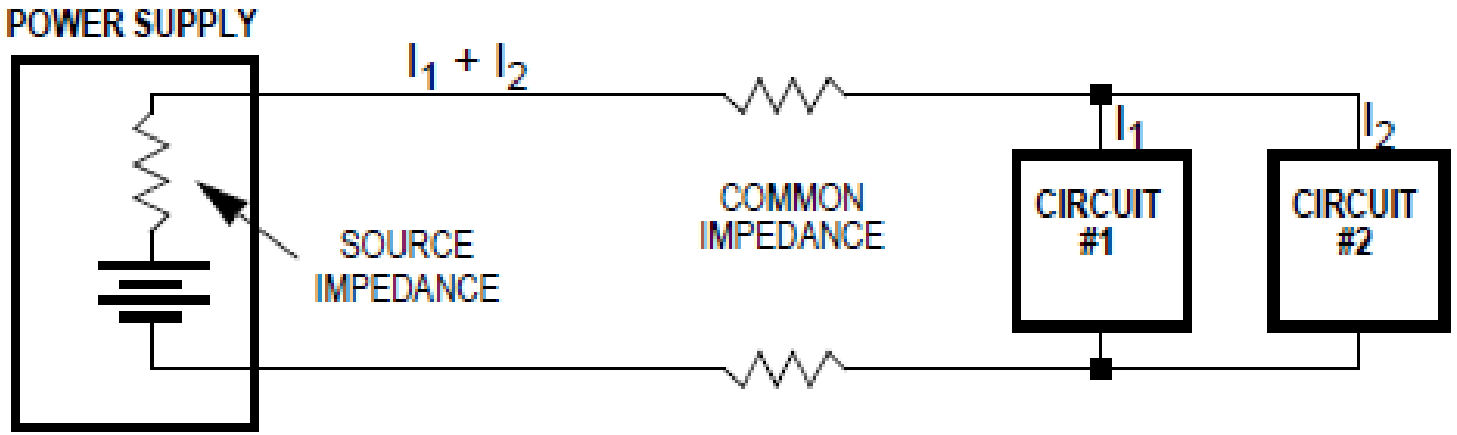
EMI Coupling Paths

- **Through conductors (wire running through a noisy environment)**



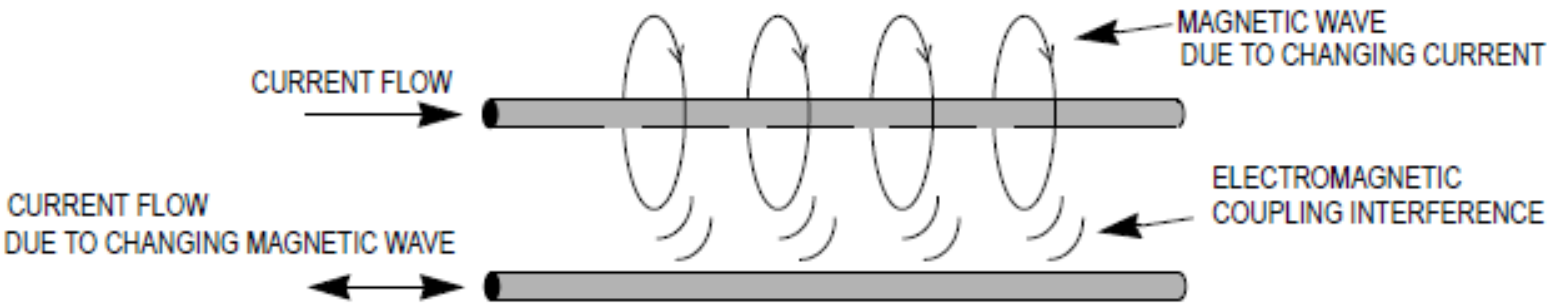
EMI Coupling Paths (2)

- **Through common impedances (shared power supply and ground wires)**



EMI Coupling Paths (3)

- **Through electromagnetic radiation**

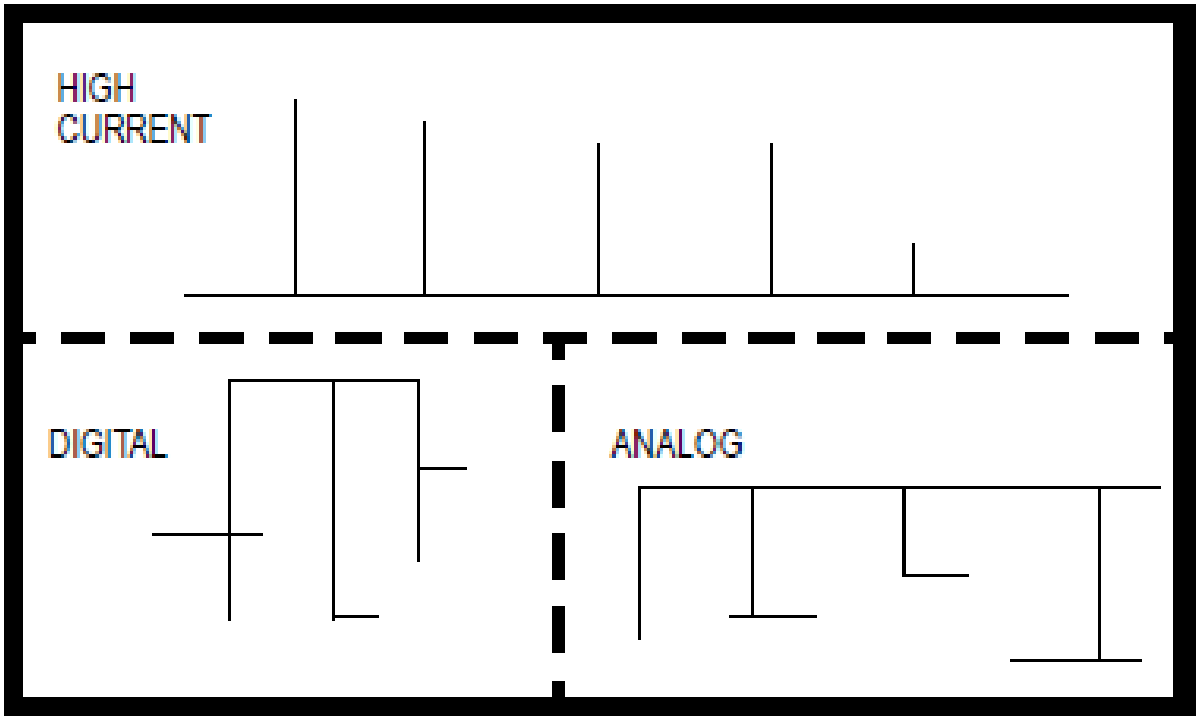


Designing for Electromagnetic Compatibility (EMC)

- **A circuit is electrically compatible if it does not affect and or become affected by its environment**
- **Remedies**
  - **Decrease emissions – can be suppressed at source through proper system design (and possibly adding shielding to contain the emission)**
  - **Increase immunity – susceptibility to noise can be decreased by "hardening" the circuit's design and using shielding to protect the circuit**

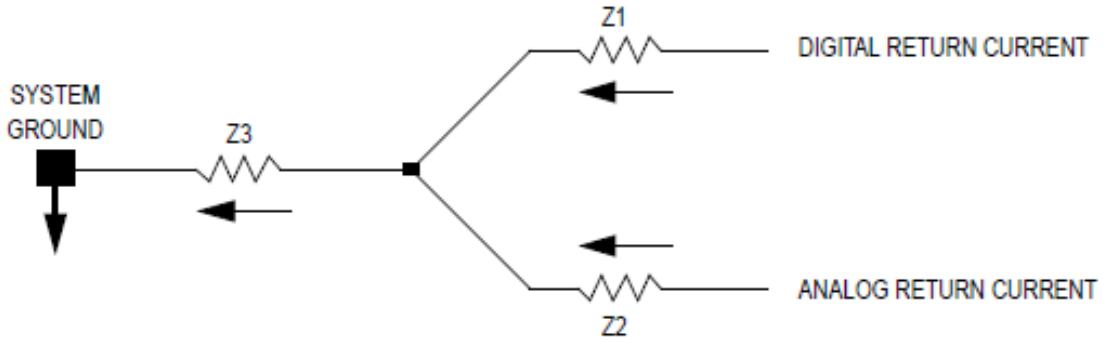
General Layout Guidelines

- **Separation of circuits on a PCB**
  - **pay close attention to the potential routing of circuits between subsystems**



General Layout Guidelines

- **Ground layout is an important PCB layout design consideration – most EMI problems can be resolved using practical and efficient grounding methods**
- **Dynamic DC offset can be created that produces a high-frequency AC component of noise that affects low-level analog circuitry**

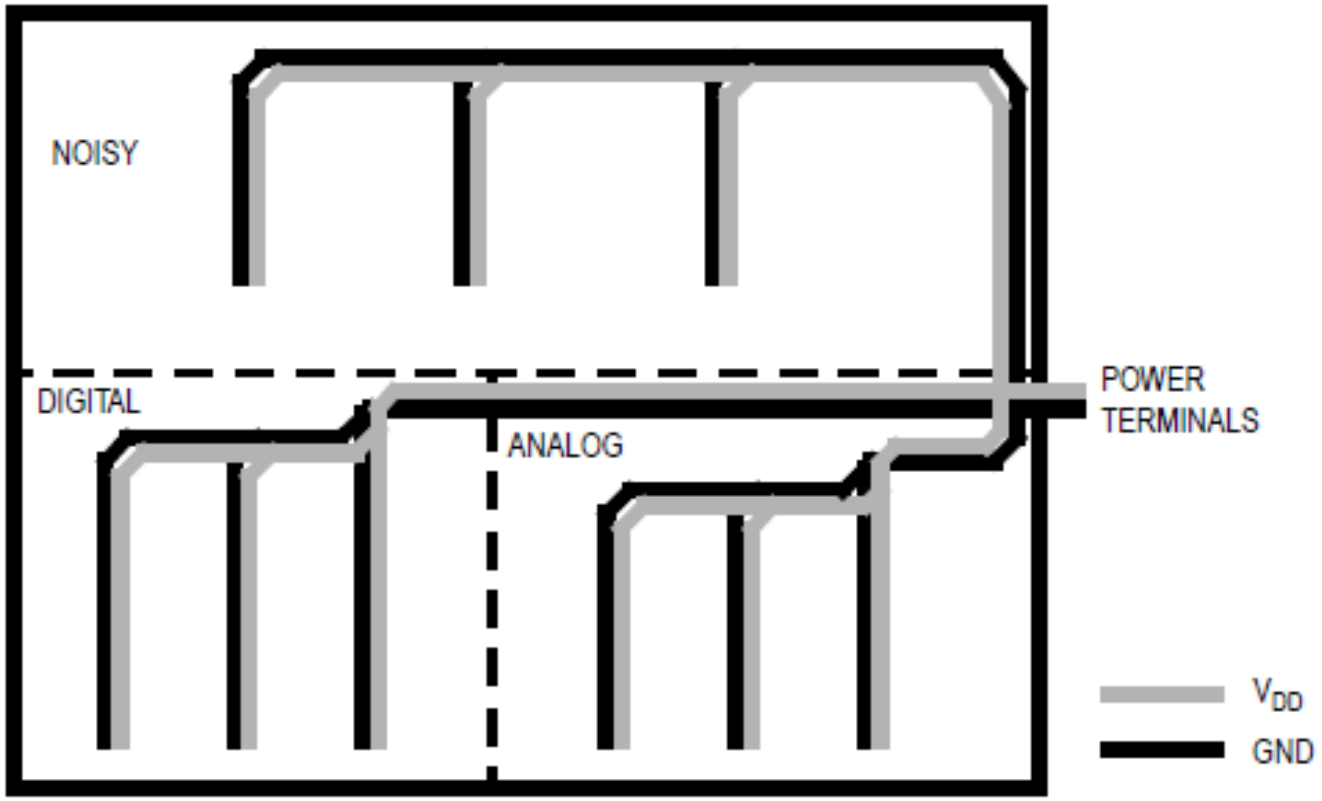


General Layout Guidelines

- **Ground layout design tips**
  - **Separate digital and analog circuits where possible**
  - **Use signal planes, especially ground planes, whenever possible**
  - **If a ground plane is uneconomical, use single-point (star-point) grounding – lowers common impedance coupling among subsystems**
  - **To decrease trace inductance, use short, wide traces**
  - **Use 135-degree turns instead of 90-degree turns to decrease transmission reflections**
  - **Decrease the size of all ground loops as much as possible (e.g., single-point power system)**

General Layout Guidelines

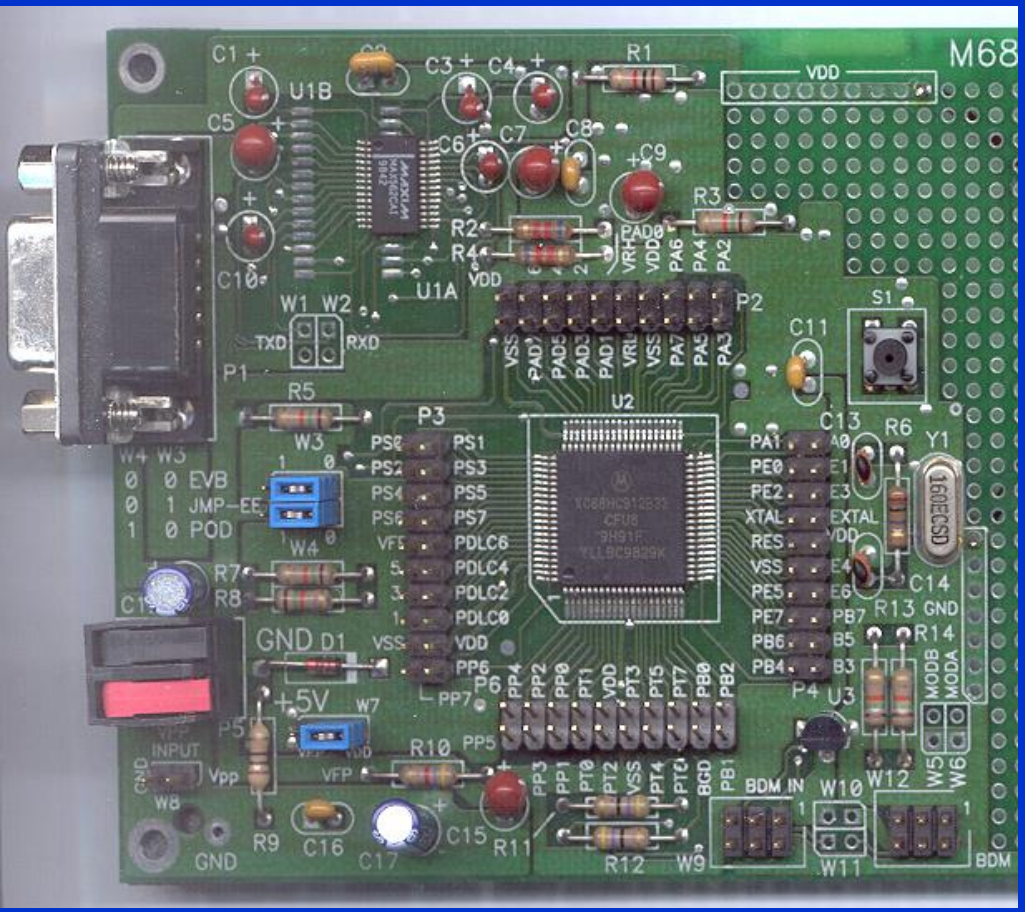
- **Single-point power system for 2-layer PCB**

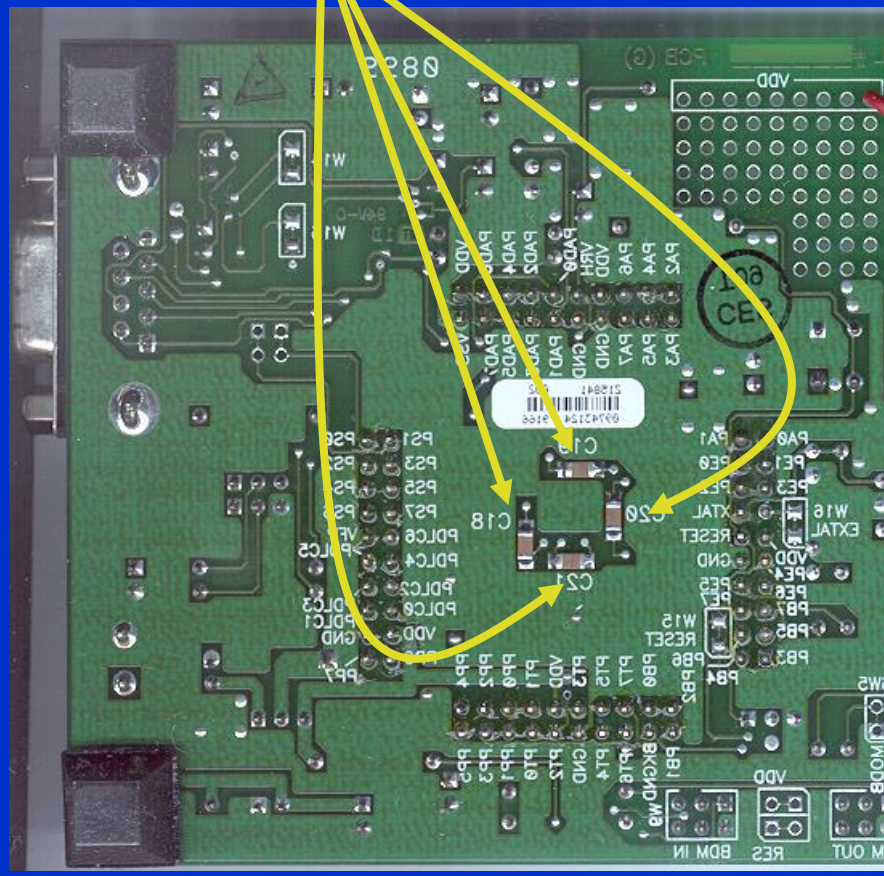


General Layout Guidelines

- **IC decoupling capacitor placement**
  - **should be as physically close to IC as possible (for surface mount components, place capacitor halfway between V_{DD} and GND)**
  - **use 0.1 µF (surface mount, ceramic) decoupling capacitors for system frequencies up to 15 MHz**
  - **above 15 MHz, use 0.01 µF decoupling capacitors**

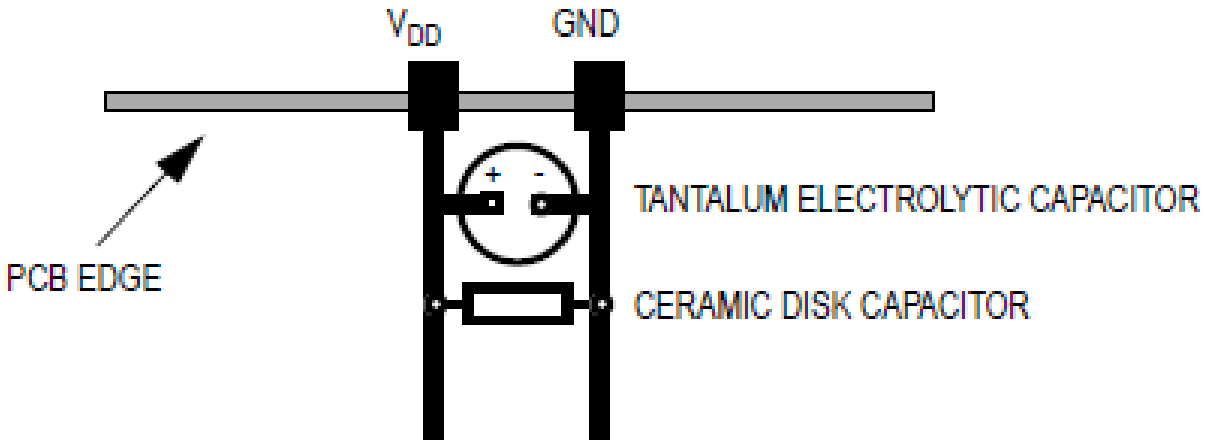
Location of Bypass Capacitors for 68HC12





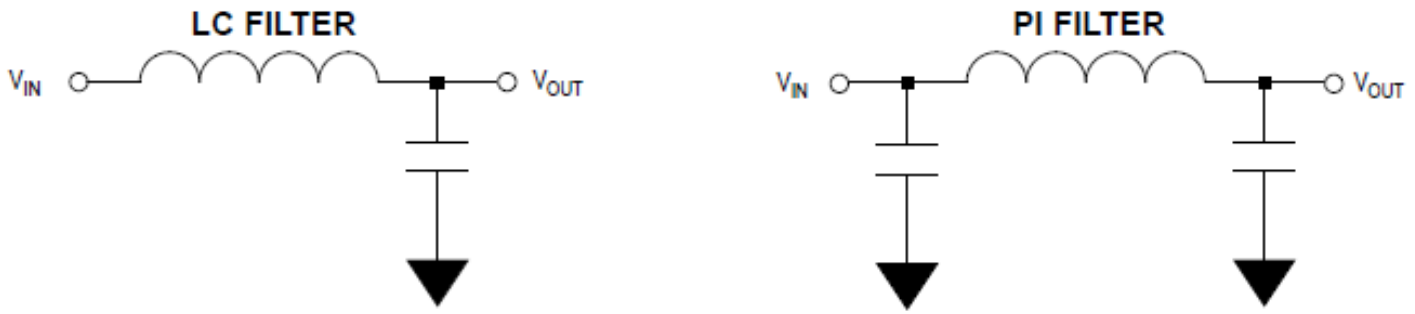
General Layout Guidelines

- **Power terminal decoupling capacitor placement**
  - **Sometimes called a "bulk" capacitor – should be placed as close to the power input terminal (connector) as possible**
  - **A small (0.1 µF capacitor should also be used to decouple high frequency noise at the power input terminal**
  - **Purpose of bulk capacitor is to help recharge the IC decoupling capacitors**
  - **Value is not critical, but should be able to recharge 15-20 ICs (multiple bulk capacitors may be used if there are more than 15-20 ICs)**



General Layout Guidelines

- **High frequency noise filters**
  - **Use if additional filtering needed to isolate a circuit for noise on the power lines (e.g., RF modules)**
  - **Place filter as close to part as possible**
  - **Ferrite beads can also be used to filter out unwanted system noise (especially on cables)**

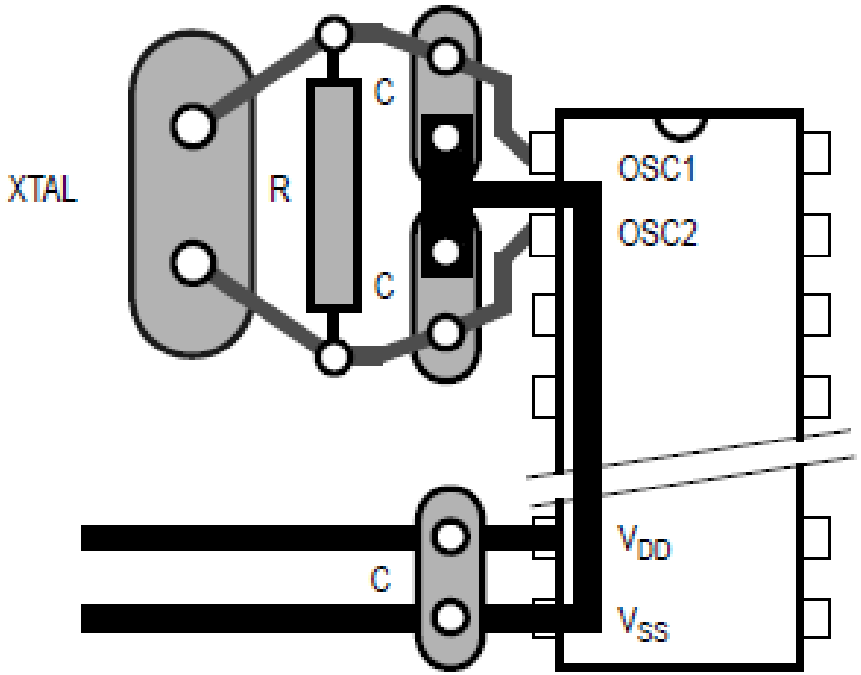


General Layout Guidelines

- **Signal layout**
  - **Most sensitive digital signals usually clock, reset, and interrupt lines**
  - **If analog and digital signals must cross one another, make sure the lines cross each other at 90° angles (reduces cross-coupling)**

General Layout Guidelines

- **Crystal or ceramic resonator circuit layout**



Layout Tips - 1

- **Keep parts that belong close together on layout close together on schematic**
- **Print layout in *1:1 scale* and compare footprints with *your actual parts* before ordering PCBs**
- **Position parts carefully first, route second (“measure twice, cut once”)**
- **Avoid trace angles ≤ 90° in routing whenever possible (PCB layout tool enforces this)**
- **Separate digital/analog grounds, and tie together at a *single point only***

Layout Tips - 2

- **Use larger power traces and orient your power supplies and supply lines near where they are used, and put them in a place where they won’t interfere (e.g., away from GPS or RF modules)**
- **Provide an ample number of *test points* (suggest header that breaks out all significant microcontroller signal pins)**

Layout Tips - 3

- **Be sure to include relevant board information in the silkscreen layer of your board (name, date, board revision, etc.)**
- **Be aware that connector pin-out may differ based on gender (watch out for inadvertent "mirroring" of pin-out)**
- **Start even earlier than you thought you would have to start**