PURDUE
UNIVERSITY

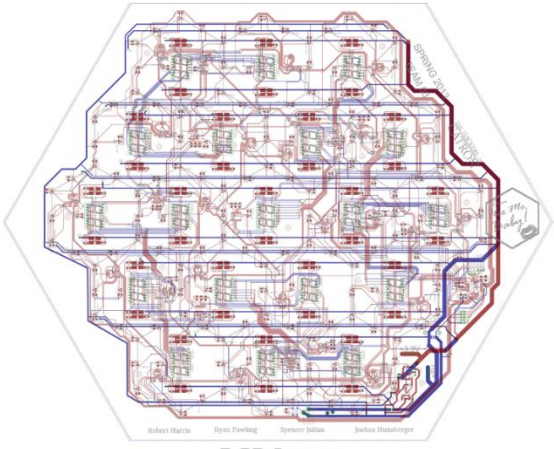
Elmore Family School of Electrical & Computer Engineering

ECE 47700 – Digital Systems Senior Design Project

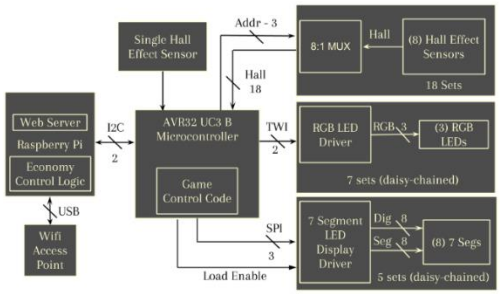
Fall 2023 Course Syllabus

A Game in Progress

Web Application



PCB Layout



Block Diagram

1.0 Course Description

Digital Systems Senior Design Project (ECE 47700) is a structured approach to the development and integration of embedded microcontroller hardware and software that provides senior-level students with significant design experience applying microcontrollers to a wide range of embedded systems (e.g., instrumentation, process control, telecommunications, intelligent devices, etc.). The primary objective is to provide practical experience developing integrated hardware and software for embedded microcontroller systems in an environment that models one which students will most likely encounter in industry.

One of the unique features of this senior design option is that each team gets to choose their own specific project (subject to some general constraints) and define specific success criteria germane to that project. In general, this approach to senior design provides students with a sense of project ownership as well as heightened motivation to achieve functionality.

Course Title: ECE 47700 Digital Systems Senior Project
CRNs: Lecture-37776, Ind. Study-38075, Labs-26019/68480/28699/62147
Lecture: TR - 4:30-5:20 pm in ME 1130
Labs: Section 8: T 9:30-11:20 pm in BHEE 007
Section 5: W 9:30-11:20am in BHEE 007
Section 9: W 12:30-2:20 pm in BHEE 007
Section 4: W 3:30-5:20 pm in BHEE 007
Lecture and Lab: Face-to-Face
4 Credit Hours
Prerequisites: A minimum grade of D- is required in the following courses.
ECE 20100, 20200, 20700, 20800, 25500, 27000, 30100, 30200, 31100, 36200, 36400, 36800
These courses may not be taken concurrently with ECE 47700. (See Course Catalog for more prerequisite details.)

1.1 Course Staff and Office Hours

Name	*Title / Role*	*E-mail Address*
Dr. Phil Walter	Instructor / Project Advisor	philwalter@purdue.edu
Joseph Bougher	Digital Systems Lab Engineer	bougher@purdue.edu
Rohan Sakar	Head Teaching Assistant	sarkarr@purdue.edu
Andjey Ashwill	Teaching Assistant	aashwill@purdue.edu
Xiang Li	Teaching Assistant	li2068@purdue.edu
Adithya Sineesh	Teaching Assistant	asineesh@purdue.edu
Oindrilla Sanyal	Teaching Assistant	osanyal@purdue.edu

Dr. Walter's Office Hours:
Tuesdays: 12:30 – 2:00pm in BHEE 252 or Potter 208b or BHEE 007
Thursdays: 10:30 – 12:00pm in BHEE 252 or Potter 208b or BHEE 007
Fridays: 1:00 - 3:00pm by Appointment Only on https://philwalter.youcanbook.me/
You may stop by my office (BHEE 252) at other times (only knock if door is open or ajar) or email or call 765-494-3454 for an appointment.

TA Office Hours will be posted on Brightspace by the second week of the course.

1.2 Learning Outcomes

1. Apply knowledge obtained in earlier coursework and to obtain new knowledge necessary to design and test a microcontroller-based digital system.
2. Understand the engineering design process.
3. Function on a multidisciplinary team.
4. Be aware of professional and ethical responsibility.
5. Communicate effectively, in both oral and written form.

1.3 Lecture Outline

Week(s)	*Lecture Topics*
1	Course introduction, Defining Requirements
2	Hardware Interfacing
3	Discrete Components
4	Power Considerations
5	Embedded Software, Hardware Design Fundamentals
6	Hardware Design Techniques, PCB Design Verification
7	Hardware and Software Debugging, Design Review Guidelines
8	Formal Design Reviews
9	PCB Verification, Assembly, and Ordering, Soldering Techniques
10	Legal and Regulatory Considerations
11	Reliability and Safety Considerations
12	Ethical and Environmental Considerations
13	Next Steps, Final Presentations Guidelines
14	Project Completion Demonstrations
15	Final Presentations

1.4 General Attendance Policies

This course follows the Academic Regulations: Attendance and Office of the Dean of Students: Class Absences posted in Brightspace under "University Policies and Statements." The policies state that students are expected to be present for every meeting of the classes in which they are enrolled. Attendance will be taken both in the lectures and in the Labs and lateness will be noted. **Note that more than 2 unexcused absences from the Labs or more than 5 unexcused absences from the Lectures will result in failure of the course.** When conflicts or absences can be anticipated, such as for many University-sponsored activities and religious observations, you should inform me of the situation as far in advance as possible. For unanticipated or emergency absences when advance notification to is not possible, contact me as soon as possible by email or phone. For cases that fall under excused absence regulations, you or your representative should contact or go to the Office of the Dean of Students (ODOS) website to complete appropriate forms for instructor notification. Under academic regulations, excused absences may be granted by ODOS for cases of grief/bereavement, military service, jury duty, parenting leave, or emergent medical care.

2.0 Summary of Design Project Specifications / General Requirements

Work on the design project is to be completed in teams of four students. The design project topic is flexible, and each group is encouraged to pick a project that uses the strengths and interest areas of their group members. The design must have the following components:

- **Microcontroller:** To help make the project tractable, recommended microcontroller choices include STM, ESP32, and Nordic variants. Development tools are readily available in lab to support these devices. Further, the devices themselves are relatively low cost and readily available. Optionally, auxiliary processing can be accomplished using a single board computer such as a Raspberry Pi or Jetson Nano.
- **Interface to Something:** The embedded system designed must interface to some other device or devices. It could be a computer, smart phone, tablet, or some other embedded device. Interface standards that can be used include; asynchronous or synchronous serial, parallel, Universal Serial Bus (USB), Bluetooth, Bluetooth Low Energy, Zigbee, Ethernet, Infrared (IR), Radio Frequency (RF), etc. This requirement has a large amount of freedom. To help with some of the more complex interfaces such as Ethernet and USB, dedicated chips which encapsulate the lowest layers of the interface can be utilized. This makes using these interfaces easier to handle but not necessarily trivial. (NOTE: *Interfaces involving A.C. line current require special permission – see the instructor for details.*)
- **Custom printed circuit board:** Through the process of the design, each group will be required to draw a detailed schematic. From the schematic, a two-layer printed circuit board will be designed. Teams are responsible for ordering circuit boards, assembly (soldering parts on the board), and completing the final stages of debugging and testing on their custom boards.
- **Be of personal interest to at least two team members:** It is very difficult to devote the time and energy required to successfully complete a major design project in which you and/or your team members have no personal interest. There are *lots* of possibilities, ranging from toys and games to "useful and socially redeeming" household items, like audio signal processors and security systems.
- **Be tractable:** You should have a "basic idea" of how to implement your project, and the relative hardware/software complexity involved. For example, you should not design an "internet appliance" if you have no idea how TCP/IP works. Also, plan to use parts that are reasonably priced, have reasonable footprints, and are *readily available*. Be cognizant of the prototyping limitations associated with surface mount components.
- **Be neatly packaged:** The finished project should be packaged in a reasonably neat, physical sound, environmentally safe fashion. Complete specification and CAD layout of the packaging represents one of the project design components.
- **Not involve a significant amount of "physical" construction:** The primary objective of the project is to learn more about *digital system* design, not mechanical engineering! Therefore, most of the design work for this project should involve digital hardware and software.

2.1 Project Proposal

Each group should submit a proposal outlining their design project idea. This proposal should be efficient and concise. It should include your design objectives, design/functionality overview, and project success criteria. The five project success criteria common to all projects include the following:

- Create a bill of materials and order/sample all parts needed for the design
- Develop a complete, accurate, readable schematic of the design
- Complete a layout and etch a printed circuit board
- Populate and debug the design on a custom printed circuit board
- Package the finished product and demonstrate its functionality

In addition to the general project success criteria listed above, a set of **five significant** *project-specific Design Requirements* (PSDRs) must be specified. There PSDRs will encompass the team's ECE engineering design efforts for the project (verses other portions of the project which may use off-the-shelf hardware and software components). The degree to which these general success criteria and PSDRs are achieved will constitute several components of your team's grade.

Forms for the preliminary and final versions of your team's project proposal are available on the course web site and Brightspace. Use these skeleton files to create your own proposal. Note that the proposal should also include assignment of each team member to one of the design component reports as well as to one of the professional component reports for the project.

2.2 Group Account and Team Webpage

Each team will be assigned an ECN group account to use as a repository for all their project documentation and for hosting a password-protected team web page. The team web page should contain datasheets for all components utilized, the schematic, board layout, software listings, interim reports, presentation slides, etc. It should also contain the progress reports (prepared in advance of the weekly progress briefings) for each team member. At the end of the semester, each team website will be archived on the course website.

2.3 Design Review

Part way through the design process, there will be a formal design review. This is a critical part of the design process. In industry, this phase of the design process can often make or break your project. A good design review is one where a design is actively discussed, and consensus is reached. The design review is often the last chance to catch errors before the design is "frozen", boards are etched, and hardware is purchased. *A friend is not someone who rubber-stamps a design, but rather one who actively challenges the design to confirm the design is correct.*

Approach the design review from a top-down, bottom-up perspective. First, present a block diagram of your design and explain the functional units. Then drop to the bottom level and explain your design at a schematic level. Be prepared to justify every piece of the design; a perfectly valid answer, however, is applying the recommended circuit from an application note. If you do use a circuit from an application note, have the documentation on hand and be able to produce it. *Your grade for the design review will not be based on the number of errors identified in your design.* The best engineers make mistakes, and the purpose of the design review is to *catch them* rather than spend *hours of debugging later* to find them. The design review will be graded primarily on how well the group understands their design and the professionalism with which they present it.

3.0 Design Project Milestones and Course Schedule

Each group is responsible for setting and adhering to their own schedule; however, there are several important milestones, as listed in the table below. Note, the preliminary project proposals are submitted before the semester begins as part of the enrollment process. As such, students were expected to submit a final proposal in week 1. (See Course Calendar for due dates.)

Week	*Milestone*	*Deliverables*
1	Devise a project budget, schedule, and determine project specific design requirements. Research and select major components, including the family of microcontroller (e.g. STM32, ESP32, etc.) and power supply components (switching regulator, battery management).	Final Project Proposal
2	Check out a microcontroller development board and write code that exercises various on-chip peripherals (e.g., blink an LED at variable rate specified by analog input voltage, debug via RS 232). Order some parts for prototyping purposes. Formulate project description, PSDRs and initial block diagram.	Functional Specification
3	Begin prototyping microcontroller interfaces (work on parts of circuit most complex first). Start prototyping power supply circuitry. Begin selecting secondary components (e.g., voltage level translators, specialty diodes, capacitors, resistors, etc.) – note that an RS 232 level translator chip is required for the microcontroller to communicate with a host PC via RS 232). Continue to order and prototype project components. Continue to formulate project description and PSDRs.	Software Overview
4	Finalize and order major components. Continue prototyping microcontroller. Continue to formulate project description and PSDRs.	Component Analysis and Electrical Overview
5	Create packaging CAD drawings. Continue prototyping interface and support circuitry. Finalize the project description, PSDRs, and any design bonuses.	Mechanical Overview and Bill of Materials
6	Begin schematic and begin PCB layout. Check footprints created for PCB library against actual components. Start developing schematics and create footprints needed for PCB parts library.	Software Formalization and Preliminary Schematic/ PCB footprint/component development
7	Finalize PCB layout for Design Review. Continue software development and testing. Prepare for Design Review.	PCB Layout Design and prepare for Design Review
8	Practice presentation. Continue software development.	Design Review Presentation
9	Incorporate changes/comments from Design Review and order PCBs.	Order PCBs
	Spring Break!	
10	Continue software development and testing.	Legal & Regulatory Analysis Report
11	Begin populating/testing PCB. Test PCB section-by-section as parts are added, porting software as you go – ***add functions one-by-one so you know what it was that "broke" your code or your board when things stop working.***	Reliability and Safety Analysis Report
12	Continue populating and debugging PCBs. Finalize packaging and system integration.	Ethical/ Environmental Impact Analysis Report
13	Complete system integration and packaging.	User Manual

14	Final touches on project. First draft of ABET Sr. Design Report. Project Completion Demo & PSDR Checkoff.	Draft ABET Sr. Design Report, Project Completion!
15	Final Presentations. Spark Challenge. Revised ABET Sr. Design Report. Final Project Archive.	Final Presentations, Revised ABET Sr. Design Report, and Final Project Archive

3.1 Course Calendar

ECE 47700 - Fall 2023 **Weeks 1-8** **Tenative Schedule - Subject to Change**

	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday
Week 1	August 21, 2023	August 22, 2023 Man Lab 8 (9:30-11:20) Lecture 1 Intro to ECE 47700	August 23, 2023 Man Lab 5 (9:30-11:20) Man Lab 9 (12:30-2:20) Man Lab 4 (3:30-5:20)	August 24, 2023 Lecture 2 Defining Requirements	August 25, 2023 Due at 11:59pm (I) Participation Quiz 1 (T) A0 - Revised IPP	August 26, 2023 Due at 11:59pm (T) A1 - Final Project Proposal (T) Create Team Website
Week 2	August 28, 2023	August 29, 2023 Man Lab 8 (9:30-11:20) Lecture 3A Hardware Interfacing	August 30, 2023 Man Lab 5 (9:30-11:20) Man Lab 9 (12:30-2:20) Man Lab 4 (3:30-5:20)	August 31, 2023 Lecture 3B Hardware Interfacing	September 1, 2023 Due at 11:59pm (I) Progress Report - Week 1-2 (I) Participation Quiz 2	September 2, 2023 Due at 11:59pm (T) A2 - Functional Specification
Week 3	September 4, 2023 Labor Day No Classes	September 5, 2023 Man Lab 8 (9:30-11:20) Lecture 4A Discrete Components	September 6, 2023 Man Lab 5 (9:30-11:20) Man Lab 9 (12:30-2:20) Man Lab 4 (3:30-5:20)	September 7, 2023 Lecture 4B Discrete Components	September 8, 2023 Due at 11:59pm (I) Progress Report -Week 3 (I) Participation Quiz 3	September 9, 2023 Due at 11:59pm (I) A3 - Software Overview
Week 4	September 11, 2023	September 12, 2023 Man Lab 8 (9:30-11:20) Lecture 5A Power Design	September 13, 2023 Man Lab 5 (9:30-11:20) Man Lab 9 (12:30-2:20) Man Lab 4 (3:30-5:20)	September 14, 2023 Lecture 5B Power Design	September 15, 2023 Due at 11:59pm (I) Progress Report - Week 4 (I) Participation Quiz 4	September 16, 2023 Due at 11:59pm (I) A4 - Electrical Overview (T) A5 - Component Analysis
Week 5	September 18, 2023	September 19, 2023 Man Lab 8 (9:30-11:20) Lecture 6 Hardware (PCB) Design 1	September 20, 2023 Man Lab 5 (9:30-11:20) Man Lab 9 (12:30-2:20) Man Lab 4 (3:30-5:20)	September 21, 2023 Lecture 7 Hardware (PCB) Design 2	September 22, 2023 Due at 11:59pm (I) Progress Report - Week 5 (T) "Locked Down" PSDRs (I) Participation Quiz 5	September 23, 2023 Due at 11:59pm (I) A6 - Mechanical Overview (T) A7 - Bill of Materials
Week 6	September 25, 2023	September 26, 2023 Man Lab 8 (9:30-11:20) Lecture 8 PCB Design Verification	September 27, 2023 Man Lab 5 (9:30-11:20) Man Lab 9 (12:30-2:20) Man Lab 4 (3:30-5:20)	September 28, 2023 Lecture 9A Firmware Design	September 29, 2023 Due at 11:59pm (I) Progress Report - Week 6 (T) Schematic & PCB Footprints (I) Participation Quiz 6	September 30, 2023 Due at 11:59pm (I) A8 - Software Formalization
Week 7	October 2, 2023	October 3, 2023 Man Lab 8 (9:30-11:20) Lecture 9B PCB Debugging	October 4, 2023 Man Lab 5 (9:30-11:20) Man Lab 9 (12:30-2:20) Man Lab 4 (3:30-5:20)	October 5, 2023 MDR Lecture Design Review Lecture	October 6, 2023 Due at 11:59pm (I) Progress Report Week 7 (T) PCB Layout (I) Participation Quiz 7	October 7, 2023 Work on Midterm Design Review Presentation
Week 8	October 9, 2023 October Break No Classes	October 10, 2023 October Break No Classes	October 11, 2023 Midterm Design Review Presentations Due after Pres. (I) Pres. Peer Reviews	October 12, 2023 Midterm Design Review Presentations Due after Pres. (I) Pres. Peer Reviews	October 13, 2023 Midterm Design Review Presentations Due after Pres. (I) Pres. Peer Reviews	October 14, 2023 Due at 11:59pm (I) Midterm Teammate Reviews
	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday

ECE 47700 - Fall 2023 **Weeks 9-End** **Tenative Schedule - Subject to Change**

	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday
Week 9	October 16, 2023	October 17, 2023 Man Lab 8 (9:30-11:20) Lecture 10 PCB Verification & Assembly	October 18, 2023 Man Lab 5 (9:30-11:20) Man Lab 9 (12:30-2:20) Man Lab 4 (3:30-5:20)	October 19, 2023 Lecture 11 Soldering Techniques	October 20, 2023 Due at 11:59pm (I) Progress Report Week 8-9 (I) Participation Quiz 9	October 21, 2023 Due at 11:59pm (T) PCB Verification & Order
Week 10	October 23, 2023	October 24, 2023 Man Lab 8 (9:30-11:20) Lecture 12A Legal & Regulatory	October 25, 2023 Man Lab 5 (9:30-11:20) Man Lab 9 (12:30-2:20) Man Lab 4 (3:30-5:20)	October 26, 2023 Lecture 12B Legal & Regulatory	October 27, 2023 Due at 11:59pm (I) Progress Report - Week 10 (I) Participation Quiz 10	October 28, 2023 Due at 11:59pm (I) A9 - Legal & Regulatory Analysis
Week 11	October 30, 2023	October 31, 2023 Man Lab 8 (9:30-11:20) Lecture 13A Reliability & Safety	November 1, 2023 Man Lab 5 (9:30-11:20) Man Lab 9 (12:30-2:20) Man Lab 4 (3:30-5:20)	November 2, 2023 Lecture 13B Reliability & Safety	November 3, 2023 Due at 11:59pm (I) Progress Report - Week 11 (I) Participation Quiz 11	November 4, 2023 Due at 11:59pm (I) A10 - Reliability & Safety Analysis
Week 12	November 6, 2023	November 7, 2023 Man Lab 8 (9:30-11:20) Lecture 14 Ethical Considerations	November 8, 2023 Man Lab 5 (9:30-11:20) Man Lab 9 (12:30-2:20) Man Lab 4 (3:30-5:20)	November 9, 2023 Lecture 15 Environmental Concerns	November 10, 2023 Due at 11:59pm (I) Progress Report - Week 12 (I) Participation Quiz 12	November 11, 2023 Reports Due at 11:59pm (I) A11 - Ethical & Environ. Analysis
Week 13	November 13, 2023	November 14, 2023 Man Lab 8 (9:30-11:20) Lecture 16 Final Steps	November 15, 2023 Man Lab 5 (9:30-11:20) Man Lab 9 (12:30-2:20) Man Lab 4 (3:30-5:20)	November 16, 2023	November 17, 2023 Due at 11:59pm (I) Progress Report - Week 13	November 18, 2023 Due at 11:59pm (I) A12 - User Manual
Week 14	November 20, 2023	November 21, 2023	November 22, 2023 Thanksgiving Vacation	November 23, 2023 Thanksgiving Vacation	November 24, 2023 Thanksgiving Vacation	November 25, 2023 Thanksgiving Vacation
Week 15	November 27, 2023	November 28, 2023	November 29, 2023 Due at 11:59pm (T) A13a - Draft Sr. Des. Rep	November 30, 2023	December 1, 2023 Due before 5:00pm (T) Project Demo Deadline Due at 11:59pm (I) Progress Report - Week 14-15	December 2, 2023 Work on Final Presentations
Week 16 Quiet Week	December 4, 2023	December 5, 2023 Final Presentations Due after Pres. (I) Pres. Peer Reviews	December 6, 2023 Final Presentations Due after Pres. (I) Pres. Peer Reviews	December 7, 2023 Final Presentations Due after Pres. (I) Pres. Peer Reviews	December 8, 2023 SPARK CHALLENGE	December 9, 2023 Due at 11:59pm (I) Final Teammate Reviews (T) A14 - Project Archive (T) A13b - Sr. Design Report
Week 17 Finals Week	December 11, 2023	December 12, 2023	December 13, 2023	December 14, 2023	December 15, 2023	December 16, 2023
	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday

4.0 Course Policies

All students and teams are expected to read and adhere to the ECE 47700 course policies that cover hardware restrictions, development environments, outside collaboration, laboratory facilities and equipment, progress reports, PSDRs, and the project completion demonstration. These policies are posted on the course Brightspace.

5.0 Course Grade Determination Policies and Procedures

ECE 47700 is a course that requires both individual and team-based efforts in order for a given student and team to succeed. The ability of a student to pass ECE 47700 and graduate from the Purdue University School of Electrical Engineering undergraduate degree program hinges on the student and team successfully satisfying the evaluation criteria for ECE 47700. The method by which student grades are determined is detailed in this section.

Student grades are based upon individual and team grade components. For the purposes of the course, the individual component of a student's grade is based upon efforts undertaking specifically by the student in question. The team component of a student's grade is based upon efforts undertaken by both the student and other team members that impact the success of the team as a whole.

5.1 Grade Determination

Student course grades will be determined per the breakdown in Table 1, below:

Table 1. Determination of Student Grades

Team Components (40% of total)		**Individual Components (60% of total)**	
PSDRs Satisfaction*	20.0%	Weekly Progress Update Reports*	20.0%
Design Review*	15.0%	Design Component Report*	15.0%
Final Presentation*	10.0%	Professional Component Report*	15.0%
Final Project Archive*	15.0%	Individual Contribution	20.0%
Concept Development Assignments	10.0%	Class Attendance and Participation	10.0%
System Integration and Packaging	20.0%	Mandatory Lab Session Attendance	10.0%
Educational (Senior Design) Report*	5.0%	Confidential Teammate Reviews (2)	5.0%
PCB Completion and Submission*	5.0%	Design Review and Final Presentation Peer Evals	5.0%
Bonus Components (added to grade total)			
Early completion		1.0% per week early (team)	
Design bonus contracts		(variable – negotiated with course staff before Week 6)	
Design Showcase participation		1.0% per individual	
Design Showcase poster		1.0% per team	
Purdue mycourseval Evaluation		0.5% per individual	
Instructor discretion (borderline resolution)		0.5% per individual	

* *items directly related to ABET course outcome assessment*

A description of each component of the grade determination is discussed in sections 5.4, 5.5, and 5.7. Note that some items are directly related to the course outcomes, as detailed in section 5.3.

Student performance on various elements of the course will be used to calculate a student's weighted percentage grade based on the weights in Table 1, above. Letter grades are then assigned on a 90-80-70-60 scale. Letter grades in the upper 30% of each range will receive a "+" designation, and those that fall in the lower 30% of each range will have a "-" designation.

5.1.1 Incompletes and Conditional Failures

A grade of "incomplete" (I) or "conditional failure" (E) will be given *only* for cases in which there are ***documented*** medical or family emergencies that prevent a student from completing required course work by the end of the semester. University regulations stipulate that a student must be passing in order to ***qualify*** for a grade of "I" or "E".

5.1.2 Borderline Cases

A "borderline" is officially defined as a weighted percentage grade within 0.5% of a cutoff when the **final** grade calculation is performed. Before course grades are assigned, the instructor will carefully examine all such cases and determine if the next higher grade is warranted. Grade adjustments are made at the sole discretion of the course staff and are not guaranteed.

5.2 Professionalism, Academic Integrity, and Copyright

Unless otherwise noted, students are expected to do their own work, and not copy the work of any other individual, past or present. Any and all sources used in the completion of ECE 47700 lab activities should be properly referenced, and where appropriate, the level of original work performed by the student should be noted. Any documented case of academic dishonesty will result in a failing grade for the course as well as possible disciplinary action. All cases of academic dishonesty will be reported to the ECE Associate Head as well as to the Dean of Students. ***A professional person does not take credit for the work of somebody else.***

Academic integrity is one of the highest values that Purdue University holds. Individuals are encouraged to alert university officials to potential breaches of this value by either emailing integrity@purdue.edu or by calling 765-494-8778. While information may be submitted anonymously, the more information is submitted the greater the opportunity for the university to investigate the concern. More details are available on our course Brightspace under University Policies and Statements.

See the University Policies and Statements section of Brightspace for guidance on Use of Copyrighted Materials. Effective learning environments provide opportunities for students to reflect, explore new ideas, post opinions openly, and have the freedom to change those opinions over time. Students and instructors are the authors of the works they create in the learning environment. As authors, they own the copyright in their works subject only to the university's right to use those works for educational purposes Students may not copy, reproduce, or post to any other outlet (e.g., YouTube, Facebook, or other open media sources or websites) any work in which they are not the sole or joint author or have not obtained the permission of the author(s).

5.3 Learning Outcome Assessment

In order to satisfy ABET course requirements, each student is expected to successfully demonstrate the set of learning outcomes approved by the ECE Senior Design Committee, listed in Table 2 along with the evaluation instruments used to assess their demonstration.

Table 2. Course Outcome Assessment Instruments

Outcome	*Course Outcome*	*Evaluation Instruments Used*
(i)	An ability to apply engineering design to create a product that meets the specified needs of this engineering design experience with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors.	Design Component Homework
(ii)	An ability to develop and conduct experimentation, analyze and interpret data, and use engineering judgment to draw conclusions related to the development of the product of this engineering design experience.	Individual Progress Reports
(iii)	An ability to identify, formulate, and solve complex engineering problems arising from this engineering design experience by applying principles of engineering, science, and mathematics.	PCB Completion and Submission
(iv)	An ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives associated with this design experience.	Project Success Criteria (general ***and*** PSDRs)
(v)	An ability to communicate effectively with a range of audiences appropriate to this design experience in both a written report and oral presentation.	Professional Component Homework
(vi)	An ability to acquire and apply new knowledge as needed, using appropriate learning strategies to complete the engineering design experience associated with this course.	Educational (Senior Design) Report
(vii)	An ability to recognize ethical and professional responsibilities associated with this engineering design experience and make informed judgments which must consider the impact of the product of this engineering design experience in global, economic, environmental, and societal contexts.	Midterm Design Review, Final Presentation, and Final Project Archive

In order for a student to successfully demonstrate a given course outcome, a minimum score of 60% shall be required on its associated evaluation instrument. An exception to this rule is made for the general success criteria satisfaction, for which 100% of the general success criteria must be passed *in addition to* 60% of the project-specific Design Requirements.

5.4 Description of Team Components

The team component of a student's grade is responsible for 40% of their overall grade. The elements of the team component score are listed out in detail in the subsections below.

5.4.1 Project-Specific Design Requirements Satisfaction

ECE 47700 requires teams to develop a set of 5 Project-Specific Design Requirements (PSDRs). These five PSDRs are the engineering requirements of the project in which the team will focus their engineering design efforts to meet the minimum ECE design criteria for the School and ABET. A team must successfully achieve at least three of these PSDRs in preliminary testing on the final project hardware in order to meet ABET requirements and pass the course. Please note that there are specific course policies that must be observed when selecting the PSDRs and when demonstrating their achievement. More information on these course policies can be found in the "PSDR Policy" document, available on Brightspace. The final PSDRs are evaluated during the Team's Project Completion Demonstration & PSDR Checkoff. Project Completion Demo policy posted on Brightspace for more details on requirements.

5.4.2 System Integration and Packaging

In addition to a team's ability to satisfy project success criteria, the system integration score is a measure on the part of the course staff of how successfully the team was able to produce a refined final prototype of the proposed senior design project. This score includes things such as the difficulty level of the project, whether or not the senior design project was packaged, and how successfully and professionally it was done, as well as the extent to which electronic systems were combined together to produce a complete, working design. These are evaluated at the team's Project Completion Demonstration & PSDRs Checkoff. System integration and packaging is worth 20% of the student's team component grade, or 8% of the student's overall grade.

5.4.3 Midterm Design Review

During the middle of the semester, all ECE 47700 teams are expected to present their projects in the form of a midterm design review. The midterm design review allows course staff to assess students' presentation skills as well as their preparation and progress at the middle of the semester. A score of 60% on the midterm design review is required to partially satisfy an ABET course outcome (this is further described in section 5.3). The midterm design review is worth 15% of the student's team component grade, or 6% of the student's overall grade. See section 2.3 for additional details on grading of the design review presentations.

5.4.4 Final Presentation

ECE 47700 student teams are required to conduct a final presentation summarizing their development activities and progress on their senior design projects over the course of the semester. The final presentation allows course staff to assess students' presentation and communication skills. A score of 60% on the final presentation is required to partially satisfy an ABET course outcome (this is further described in section 5.3). The final presentation is worth 10% of the student's team component grade, or 4% of the student's overall grade.

5.4.5 Final Project Archive

At the end of the semester, student teams are required to compile revised assignments and source code and submit a final project archive for their respective senior design projects. The final archive provides the course staff with the opportunity to assess the student teams' abilities to

communicate technical information in written form. A minimum score of 60% on the final archive is required to partially satisfy an ABET course outcome (this is further described in section 5.3). The final archive is subject to the late assignment policy defined in section 5.6. The archive is worth 15% of the student's team component grade, or 6% of the student's overall grade.

5.4.6 Concept Development Assignments

During the earlier stages of the design process, ECE 47700 student teams are expected to complete a number of concept development assignments. These assignments are listed below:

- Functional Specification (#2)
- Component Analysis (#5)
- Bill of Materials (#7)

The purpose of these assignments is to help the team determine global design aspects and requirements of their projects, and these assignments are to be completed by and with input from the entire team. Assignments 5 and 7, though separate items, are graded as a single item. Completion of the functional specification is worth 5% of the student's team grade and completion of the component analysis and bill of materials is worth 5% of the student's team grade, for a total of 10% of the student's team grade or 4% of their overall grade.

5.4.7 Educational (“Senior Design”) Report

To satisfy educational requirements of ECE 47700, student teams are expected to complete a senior design educational summary at the end of the senior design semester. This report is used to describe the educational development of student teams over the course of their ECE 47700 senior design semester. The senior design educational summary is subject to the late assignment policy defined in section 5.6. The senior design educational summary is worth 5% of the student's team component grade, or 2% of the student's overall grade.

5.4.8 PCB Completion and Submission

ECE 47700 requires the design and fabrication of a printed circuit board (PCB); students are responsible for ordering their own individual PCBs. PCB Submission and Completion is a gradable item which assesses the ability of student teams to submit their printed circuit board for fabrication in a timely manner, to ensure completion of hardware integration and course objectives. PCB completion and submission is worth 5% of the student's team component grade, or 2% of the student's overall grade.

5.5 Description of Individual Components

The individual component of a student's grade is responsible for 60% of their overall grade. The elements of the individual component score are listed out in detail in the subsections below.

5.5.1 Progress Reports

Students are expected to maintain a progress report (engineering journal) over the course of their semester within ECE 47700. The weekly project reports should give a detailed description (using images and graphics to reduce the word count) of the work an individual completed that week on their team project. These progress reports are less formal than the other reports and will be evaluated by course staff frequently throughout the semester. A 60% or better average score on progress reports is required to satisfy an ABET outcome; this is described in further detail in section 5.3. Course policies regarding progress reports are detailed further in the Progress Report

Policy, available on Brightspace. Performance on progress reports is worth 20% of the student's individual component grade, or 12% of the student's overall grade.

5.5.2 Individual Contribution

ECE 47700 is a team-based course in which individual student efforts contribute to the overall success or failure of an ECE 47700 student team. The individual contribution score is an assessment by the course staff of how much a student contributed and helped or hindered their ECE 47700 team in the completion of their project. Many metrics are included in this assessment including the student's individual progress reports, other individual reports, team member feedback, observation from course staff over the course of the semester, and the level of project difficulty. The individual contribution grade is worth 20% of the student's individual component grade, or 12% of the student's overall grade.

5.5.3 Design Component Report

The following ECE 47700 assignments are considered design component reports for the purposes of the class:

- Software Overview (#3)
- Electrical Overview (#4)
- Mechanical Overview (#6)
- Software Formalization (#8)

Each ECE 47700 student team is required to complete one copy of each of these assignments, and each assignment is to be completed by a different member of the ECE 47700 team. A score of 60% or better score on the design component report is required to satisfy an ABET outcome; this is described in further detail in section 5.3. The design component reports are subject to the late assignment policy defined in section 5.6. The design component report is worth 15% of the student's individual component grade, or 9% of the student's overall grade.

5.5.4 Professional Component Report

The following ECE 47700 assignments are considered professional component reports for the purposes of this class:

- Legal Analysis (#9)
- Reliability and Safety Analysis (#10)
- Ethical/Environmental Impact Analysis (#11)
- User Manual (#12)

Each ECE 47700 student team is required to complete one copy of each of these assignments, and each assignment is to be completed by a different member of the ECE 47700 team. A score of 60% or better score on the professional component report is required to satisfy an ABET outcome; this is described in further detail in section 5.3. The professional component reports are subject to the late assignment policy defined in section 5.6. The professional component report is worth 15% of the student's individual component grade, or 9% of the student's overall grade.

5.5.5 Class Attendance and Participation

Attendance is required at the lectures. **More than 5 unexcused absences from the lectures will result in a course failure.** Online quizzes will be routinely used to encourage attendance and

attention in ECE 47700 lectures. Lecture attendance and participation as well as the scores on the quizzes are used to determine the Class Attendance and Participation grade which is worth 10% of the individual component grade, or 6% of the student's overall grade.

5.5.6 Mandatory Lab Session Attendance

In the interest of ensuring students are held accountable for project work and staff are up to date on student project issues and progress, weekly mandatory lab sessions are held in which ECE 47700 course staff meet with each student team. During these sessions, students are expected to detail their progress concerning their projects and homework assignments. Students are expected to attend their mandatory lab sessions and attendance is taken; failure to attend a minimum of 80% of these mandatory sessions may result in course failure **(i.e., Don't Miss More Than Two Labs!)**. Mandatory lab session attendance is worth 10% of a student's individual grade, or 6% of the student's overall grade.

5.5.7 Confidential Teammate Reviews

During the midterm and final portions of an ECE 47700 semester, feedback on student performance is provided in the form of confidential teammate reviews filled out by student team members. The midterm and final confidential peer reviews are cumulatively worth 5% of the student's individual component grade, or 3% of the student's overall grade.

5.5.8 Design Review and Final Presentation Peer Evaluations

During the midterm design review and final presentations, feedback on student presentation performance is provided in the form of peer evaluations. The midterm design review and final presentation peer evaluations are cumulatively worth 5% of the student's individual component grade, or 3% of the student's overall grade.

5.6 Late Assignment Penalty

Homework assignments are due by the deadlines described in the course calendar (typically Fridays or Saturdays) at 11:59 PM (midnight). In the event of late assignments, the following penalties are assessed:

a) -10% for every day the assignment is submitted late (rounded up)

b) If an assignment is more than 3 days late, the ECE 47700 course staff may grade it at their discretion.

5.7 Description of Bonus Components

In addition to the project and team components, opportunities exist for additional bonus credit. These bonus credit opportunities are elaborated on in the subsections below.

5.7.1 Early Completion Bonus Credit

Student teams who successfully complete their ECE 47700 senior design project early may qualify for early completion bonus credit. This is to inspire student teams to work hard and be proactive by working ahead in their senior design course. For each week prior Project Completion Demonstration & PSDR Checkoff deadline week that a team completes their project, they will receive an additional +1% bonus credit to their overall grade. This bonus credit is subject to certain conditions and is awarded at the sole discretion of the ECE 47700 course staff.

5.7.2 Poster and Design Showcase Participation

At the end of the senior design semester, ECE 47700 student teams may have the option of participating in a symposium known as the Spark Challenge. Student teams approved by course instructional staff will become eligible for bonus credit. If selected and agreed upon, the team is then required to produce a poster detailing their senior design projects. The senior design posters are used to present ECE 47700 to the general public, as well as for promotional materials for ECE 47700 used by the course staff and Purdue School of Electrical Engineering. Spark Challenge participation, along with a completed poster, is worth an additional 2% bonus credit to participating students' grades.

5.7.3 Design Bonus Contract Credit

ECE 47700 requires students to design and build a preliminary hardware prototype of a project. Depending on the particulars of a student project, students may have the opportunity to receive bonus credit for going above and beyond standard hardware design requirements for ECE 47700. Please contact course staff to see if a design bonus contract may be assessed.

6.0 General Course and University Policies

6.1 Communication:

For questions, first ask your teammates on the Team communication app you have chosen (slack, WeChat, Team section in Piazza, etc.). Next ask your assigned TA if they are included in your Team communication group. Next post on the course Piazza. Finally, if you still do not have an acceptable answer, send an email to ECE477@ecn.purdue.edu. You also may attend any of the in person or virtual office hours offered for this course (see schedule on Brightspace).

6.2 Campus Emergencies

In the event of a major campus emergency, course requirements, deadlines and grading percentages are subject to changes that may be necessitated by a revised semester calendar or other circumstances beyond the instructor's control. Relevant changes to this course will be posted onto the course website or can be obtained by contacting the instructors or TAs via email or phone. You are expected to read your @purdue.edu email on a frequent basis.

A link to Purdue's Information on Emergency Preparation and Planning is located on our Brightspace under "University Policies and Statements." This website covers topics such as Severe Weather Guidance, Emergency Plans, and a place to sign up for the Emergency Warning Notification System. I encourage you to download and review the *Emergency Preparedness for Classrooms document (**PDF**) or (**Word**).*

The first day of class, I will review the **Emergency Preparedness plan for our specific classroom**, following Purdue's required Emergency Preparedness Briefing. Please make note of items like:

- The location to where we will proceed after evacuating the building if we hear a fire alarm.
- The location of our Shelter in Place in the event of a tornado warning.
- The location of our Shelter in Place in the event of an active threat such as a shooting.

6.3 Nondiscrimination:

Purdue University is committed to maintaining a community that recognizes and values the inherent worth and dignity of every person; fosters tolerance, sensitivity, understanding, and mutual respect among its members; and encourages each individual to strive to reach his or her potential. In pursuit of its goal of academic excellence, the University seeks to develop and nurture diversity. The University believes that diversity among its many members strengthens the institution, stimulates creativity, promotes the exchange of ideas, and enriches campus life. A hyperlink to Purdue's full Nondiscrimination Policy Statement is included in our course Brightspace under University Policies and Statements.

6.4 Accessibility:

Purdue University is committed to making learning experiences accessible. If you anticipate or experience physical or academic barriers based on disability, you are welcome to let me know so that we can discuss options. You are also encouraged to contact the Disability Resource Center at: drc@purdue.edu or by phone: 765-494-1247.

6.5 Mental health / Wellness:

If you find yourself beginning to feel some stress, anxiety and/or feeling slightly overwhelmed, try WellTrack**.** Sign in and find information and tools at your fingertips, available to you at any time.

If you need support and information about options and resources, please contact or see the Office of the Dean of Students. Call 765-494-1747. Hours of operation are M-F, 8 am- 5 pm.

If you find yourself struggling to find a healthy balance between academics, social life, stress, etc., sign up for free one-on-one virtual or in-person sessions with a Purdue Wellness Coach at RecWell. Student coaches can help you navigate through barriers and challenges toward your goals throughout the semester. Sign up is free and can be done on BoilerConnect.

If you're struggling and need mental health services: Purdue University is committed to advancing the mental health and well-being of its students. If you or someone you know is feeling overwhelmed, depressed, and/or in need of mental health support, services are available. For help, such individuals should contact Counseling and Psychological Services (CAPS) at 765-494-6995 during and after hours, on weekends and holidays, or by going to the CAPS office on the second floor of the Purdue University Student Health Center (PUSH) during business hours. The CAPS website also offers resources specific to situations such as COVID-19.

6.6 Basic needs:

Any student who faces challenges securing their food or housing and believes this may affect their performance in the course is urged to contact the Dean of Students for support. There is no appointment needed and Student Support Services is available to serve students 8 a.m.-5 p.m. Monday through Friday.