# 10. Configuring Cyclone III Devices

CIII51010-2.1

## Introduction

Cyclone® III devices use SRAM cells to store configuration data. Because SRAM memory is volatile, configuration data must be downloaded to Cyclone III devices each time the device powers up.

Depending on device densities or package options, Cyclone III devices can be configured using one of five configuration schemes:

- Active serial (AS)
- Active parallel (AP)
- Passive serial (PS)
- Fast passive parallel (FPP)
- Joint Test Action Group (JTAG)

AS and AP schemes use an external flash memory, such as a serial configuration device or a supported flash memory, respectively. PS, FPP, and JTAG schemes use either an external controller (for example, a MAX® II device or microprocessor), or a download cable. When used in a multi-device configuration scheme for PS and FPP, the external controller for the slave Cyclone III device is a master Cyclone III device set in the AS and AP modes, respectively (for more information, refer to the "Configuration Features").

In some applications, it may be necessary for a device to wake up very quickly to begin operation. Cyclone III devices offer the Fast-On feature for fast power-on reset (POR) time to support fast wake-up time applications such as those used in the automotive market. Cyclone III devices support a new configuration scheme, such as the AP scheme, which uses commodity parallel flash as configuration memory without the need for an external host. This lowers system costs and offers fast configuration time. Additionally, Cyclone III devices can receive a compressed configuration bitstream and decompress the data in real-time, reducing storage requirements and configuration time. Furthermore, Cyclone III devices support remote system upgrade in active configuration modes. Remote system upgrades help deliver feature enhancements and bug fixes without costly recalls, reduce time-to-market, and extend product life.

This chapter explains Cyclone III device configuration features and describes how to configure Cyclone III devices using supported configuration schemes. This chapter also includes configuration pin descriptions and Cyclone III device configuration file formats. In this chapter, the generic term "device" includes all Cyclone III devices.

This chapter contains the following sections:

- "Configuration Features"
- "Configuration Requirements"
- "Active Serial Configuration (Serial Configuration Devices)"
- "Active Parallel Configuration (Supported Flash Memories)"

- "Passive Serial Configuration"
- "Fast Passive Parallel Configuration"
- "JTAG Configuration"
- "Cyclone III JTAG Instructions"
- "Device Configuration Pins"

## Configuration Devices

Altera® serial configuration devices (EPCS128, EPCS64, EPCS16, and EPCS4) are used in the AS configuration scheme for Cyclone III devices. Serial configuration devices offer a low-cost, low-pin count configuration solution.

For information about serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS16, EPCS64, and EPCS128) Data Sheet* chapter in volume 2 of the *Configuration Handbook*.

In the AP configuration scheme, the commodity parallel flash is used as configuration memory (for information about the supported families for the commodity parallel flash, refer to Table 10–10).

## Configuration Schemes

A configuration scheme with different configuration voltage standards is selected by driving the Cyclone III device's MSEL pins either high or low as shown in Table 10–1. The MSEL pins are powered by the $V_{CCINT}$ power supply of the bank in which they reside. The `MSEL[3..0]` pins have 9-kΩ internal pull-down resistors that are always active.

To avoid problems in detecting an incorrect configuration scheme, hardwire the MSEL pins to $V_{CCA}$ or GND without pull-up or pull-down resistors. Do not drive the MSEL pins with a microprocessor or another device.

**Table 10–1.** Cyclone III Configuration Schemes *(Note 13)* (Part 1 of 2)

| Configuration Scheme | MSEL3 *(10)* | MSEL2 | MSEL1 | MSEL0 | Configuration Voltage Standard *(9)* |
|---|---|---|---|---|---|
| Passive Serial Standard (PS Standard POR) *(6)* | 0 | 0 | 0 | 0 | 3.3/3.0/2.5 V *(11)* |
| Active Serial Standard (AS Standard POR) *(1)*, *(5)*, *(6)* | 0 | 0 | 1 | 0 | 3.3 V *(11)* |
| Active Serial Standard (AS Standard POR) *(1)*, *(5)*, *(6)* | 0 | 0 | 1 | 1 | 3.0/2.5 V *(11)* |
| Active Serial Fast (AS Fast POR) *(1)*, *(5)*, *(6)*, *(12)* | 0 | 1 | 0 | 0 | 3.0/2.5 V *(11)* |
| Active Parallel ×16 Fast (AP Fast POR) *(1)*, *(2)*, *(3)* | 0 | 1 | 0 | 1 | 3.3 V *(11)* |
| Active Parallel ×16 Fast (AP Fast POR) *(1)*, *(2)*, *(3)* | 0 | 1 | 1 | 0 | 1.8 V |
| Active Parallel ×16 (AP Standard POR) *(1)*, *(2)*, *(3)* | 0 | 1 | 1 | 1 | 3.3 V *(11)* |
| Active Parallel ×16 (AP Standard POR) *(1)*, *(2)*, *(3)* | 1 | 0 | 0 | 0 | 1.8 V |
| Active Parallel ×16 (AP Standard POR) *(1)*, *(2)*, *(3)* | 1 | 0 | 1 | 1 | 3.0/2.5 V *(11)* |

**Table 10–1.** Cyclone III Configuration Schemes *(Note 13)* (Part 2 of 2)

| Configuration Scheme | MSEL3 *(10)* | MSEL2 | MSEL1 | MSEL0 | Configuration Voltage Standard *(9)* |
|---|---|---|---|---|---|
| Passive Serial Fast (PS Fast POR) *(6)* | 1 | 1 | 0 | 0 | 3.3/3.0/2.5 V *(11)* |
| Active Serial Fast (AS Fast POR) *(1)*, *(5)*, *(6)* | 1 | 1 | 0 | 1 | 3.3 V *(11)* |
| Fast Passive Parallel Fast (FPP Fast POR) *(4)* | 1 | 1 | 1 | 0 | 3.3/3.0/2.5 V *(11)* |
| Fast Passive Parallel Fast (FPP Fast POR) *(4)* | 1 | 1 | 1 | 1 | 1.8/1.5 V |
| JTAG-based configuration *(8)* | *(7)* | *(7)* | *(7)* | *(7)* | — |

**Notes to Table 10–1:**

(1) These schemes support the remote system upgrade feature. Remote update mode is supported when using the remote system upgrade feature. You can enable or disable remote update mode with an option setting in the Quartus® II software. For more information about the remote system upgrade feature, refer to the *Remote System Upgrade with Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

(2) Some of the smaller Cyclone III devices or package options do not support the AP configuration scheme (for more information, refer to Table 10–2).

(3) In the AP configuration scheme, the commodity parallel flash is used as configuration memory (for information about the supported families for the commodity parallel flash, refer to Table 10–10).

(4) Some of the smaller Cyclone III devices or package options do not support the FPP configuration scheme (for more information, refer to Table 10–2).

(5) EPCS16, EPCS64, and EPCS128 support up to 40 MHz DCLK and are supported in Cyclone III devices. Existing batches of EPCS4 manufactured on 0.15 µ process geometry support up to 40 MHz DCLK and are supported in Cyclone III devices. However, batches of EPCS4 manufactured on 0.18 µ process geometry do not support AS configuration in Cyclone III devices. For information about product traceability and transition date to differentiate between supported and non-supported EPCS4 serial configuration devices, refer to *PCN 0514 Manufacturing Changes on EPCS Family*. For more information about serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS16, EPCS64, and EPCS128) Data Sheet* chapter in volume 2 of the *Configuration Handbook*.

(6) These schemes support data decompression.

(7) Do not leave the MSEL pins floating. Connect them to $V_{CCA}$ or GND. These pins support the non-JTAG configuration scheme used in production. If you only use JTAG configuration connect the MSEL pins to GND.

(8) JTAG-based configuration takes precedence over other configuration schemes, which means MSEL pin settings are ignored.

(9) Configuration voltage standard is applied to the $V_{CCIO}$ supply of the bank in which the configuration pins reside.

(10) Some of the smaller Cyclone III devices or package options do not support the AP configuration scheme and do not have the MSEL[3] pin (for more information about the supported configuration schemes across device densities and package options, refer to Table 10–2).

(11) You must follow specific requirements when interfacing Cyclone III devices with 2.5-, 3.0-, and 3.3-V configuration voltage standards (for information about the requirements, refer to "Configuration and JTAG Pin I/O Requirements").

(12) AS Fast POR with 2.5-, and 3.0-V configuration voltage standard is not available for devices that do not have the MSEL[3] pin (for devices that support AS Fast POR, refer Table 10–2).

(13) Connect the MSEL pins to $V_{CCA}$ or GND depending on the MSEL pin settings.

In Cyclone III devices, supported configuration schemes differ for different device densities and package options.

Table 10–2 shows the supported configuration schemes across device densities and package options.

**Table 10–2.** Cyclone III Devices Supported Configuration Schemes Across Device Densities and Package Options *(Note 1)*

| Device | Package Options *(4)* | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | **E144** | **M164** | **Q240** | **F256** | **F324** | **F484** | **F780** | **U256** | **U484** |
| EP3C5 | AS, PS, JTAG *(2)* | AS, PS, FPP, JTAG *(2)* | — | AS, PS, FPP, JTAG *(2)* | — | — | — | AS, PS, FPP, JTAG *(2)* | — |
| EP3C10 | AS, PS, JTAG *(2)* | AS, PS, FPP, JTAG *(2)* | — | AS, PS, FPP, JTAG *(2)* | — | — | — | AS, PS, FPP, JTAG *(2)* | — |
| EP3C16 | AS, PS, JTAG *(2)* | AS, PS, FPP, JTAG *(2)* | AS, PS, FPP, JTAG *(2)* | AS, PS, FPP, JTAG *(2)* | — | AS, PS, FPP, AP, JTAG *(3)* | — | AS, PS, FPP, JTAG *(2)* | AS, PS, FPP, AP, JTAG *(3)* |
| EP3C25 | AS, PS, JTAG *(2)* | — | AS, PS, FPP, JTAG *(2)* | AS, PS, FPP, JTAG *(2)* | AS, PS, FPP, AP, JTAG *(3)* | — | — | AS, PS, FPP, JTAG *(2)* | — |
| EP3C40 | — | — | AS, PS, FPP, JTAG *(2)* | — | AS, PS, FPP, AP, JTAG *(3)* | AS, PS, FPP, AP, JTAG *(3)* | AS, PS, FPP, AP, JTAG *(3)*, *(5)* | — | AS, PS, FPP, AP, JTAG *(3)* |
| EP3C55 | — | — | — | — | — | AS, PS, FPP, AP, JTAG *(3)* | AS, PS, FPP, AP, JTAG *(3)* | — | AS, PS, FPP, AP, JTAG *(3)* |
| EP3C80 | — | — | — | — | — | AS, PS, FPP, AP, JTAG *(3)* | AS, PS, FPP, AP, JTAG *(3)* | — | AS, PS, FPP, AP, JTAG *(3)* |
| EP3C120 | — | — | — | — | — | AS, PS, FPP, AP, JTAG *(3)* | AS, PS, FPP, AP, JTAG *(3)* | — | — |

**Notes to Table 10–2:**

(1) AS is active serial, PS is passive serial, FPP is fast passive parallel, and AP is active parallel.

(2) These packages do not support AP configuration scheme and AS Fast POR with 2.5-, and 3.0-V configuration voltage standard. These packages do not have the `MSEL[3]` pin.

(3) These packages support all the configuration schemes shown in Table 10–10.

(4) For more information about vertical package migration and package options for Cyclone III devices, refer to the *Cyclone III Device Family Overview* chapter and the *Package Information for Cyclone III Devices* chapter in volume 1 of the Cyclone III Device Handbook.

(5) The EP3C40 package option F780 only partially supports vertical package migration to other F780 package options.

For more information about vertical package migration and package options for Cyclone III devices, refer to the *Cyclone III Device Family Overview* chapter and the *Package Information for Cyclone III Devices* chapter in volume 1 the *Cyclone III Device Handbook*.

Cyclone III devices offer decompression and remote system upgrade features. Cyclone III devices can receive a compressed configuration bitstream and decompress this data in real-time, thus reducing storage requirements and configuration time. Data decompression is supported in AS and PS configuration schemes. You can make real-time system upgrades from remote locations of your Cyclone III designs with the remote system upgrade mode feature. Remote update is supported in AS and AP configuration schemes.

## Configuration File Format

Table 10–3 shows the approximate uncompressed configuration file sizes for Cyclone III devices. To calculate the amount of storage space required for multiple device configurations, add the file size of each device together.

**Table 10–3.** Cyclone III Uncompressed Raw Binary File Sizes *(Note 1)*

| Device | Data Size (Mbits) |
|---|---|
| EP3C5 | 3.0 |
| EP3C10 | 3.0 |
| EP3C16 | 4.1 |
| EP3C25 | 5.8 |
| EP3C40 | 9.6 |
| EP3C55 | 14.9 |
| EP3C80 | 20.0 |
| EP3C120 | 28.6 |

**Note to Table 10–3:**

(1) Raw Binary File (**.rbf**)

Use the data in Table 10–3 only to estimate the file size before design compilation. Different configuration file formats, such as a Hexadecimal (**.hex**) or Tabular Text File (**.ttf**) formats, have different file sizes. However, for any specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio is dependent on the design.

For more information about setting device configuration options or creating configuration files, refer to the *Software Settings* section in volume 2 of the *Configuration Handbook*.

# Configuration Features

Cyclone III devices offer configuration data decompression to reduce configuration file storage and provide remote system upgrade to allow you to remotely update your Cyclone III designs.

Table 10–4 summarizes which configuration features you can use in each configuration scheme.

**Table 10–4.** Cyclone III Configuration Features *(Note 2)*

| Configuration Scheme | Configuration Method | Decompression | Remote System Upgrade *(2)* |
|---|---|---|---|
| Active Serial Fast (AS Fast POR) | Serial Configuration Device | ✓ | ✓ |
| Active Serial Standard (AS Standard POR) | Serial Configuration Device | ✓ | ✓ |
| Active Parallel ×16 Fast (AP Fast POR) | Supported flash memory *(1)* | — | ✓ |
| Active Parallel ×16 (AP Standard POR) | Supported flash memory *(1)* | — | ✓ |
| Passive Serial Fast (PS Fast POR) | MAX II device or a Microprocessor with flash memory | ✓ | — |
| | Download cable | ✓ | — |
| Passive Serial Standard (PS Standard POR) | MAX II device or a Microprocessor with flash memory | ✓ | — |
| | Download cable | ✓ | — |
| Fast Passive Parallel Fast (FPP Fast POR) | MAX II device or a Microprocessor with flash memory | — | — |
| JTAG-based configuration | MAX II device or a Microprocessor with flash memory | — | — |
| | Download cable | — | — |

**Notes to Table 10–4:**

(1) For more information about the supported families for the Numonyx commodity parallel flash, refer to Table 10–10.

(2) Remote update mode is supported when using remote system upgrade feature. You can enable or disable the remote update mode with an option setting in the Quartus II software. For more information about the remote system upgrade feature, refer to the *Remote System Upgrade with Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

## Configuration Data Decompression

Cyclone III devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and transmit this compressed bitstream to Cyclone III devices. During configuration, Cyclone III devices decompress the bitstream in real time and programs their SRAM cells.

Preliminary data indicates that compression typically reduces configuration bitstream size by 35 to 55%.

Cyclone III devices support decompression in the AS and PS configuration schemes. Decompression is not supported in the AP configuration scheme, FPP configuration scheme, or JTAG-based configuration scheme.

In PS mode, use the Cyclone III decompression feature to reduce configuration time. You should also use the Cyclone III decompression feature during AS configuration if you need to save configuration memory space in the serial configuration device.

When you enable compression, the Quartus II software generates configuration files with compressed configuration data. This compressed file reduces the storage requirements in the configuration device or flash memory and decreases the time needed to transmit the bitstream to the Cyclone III device. The time needed by a Cyclone III device to decompress a configuration file is less than the time needed to transmit the configuration data to the device.

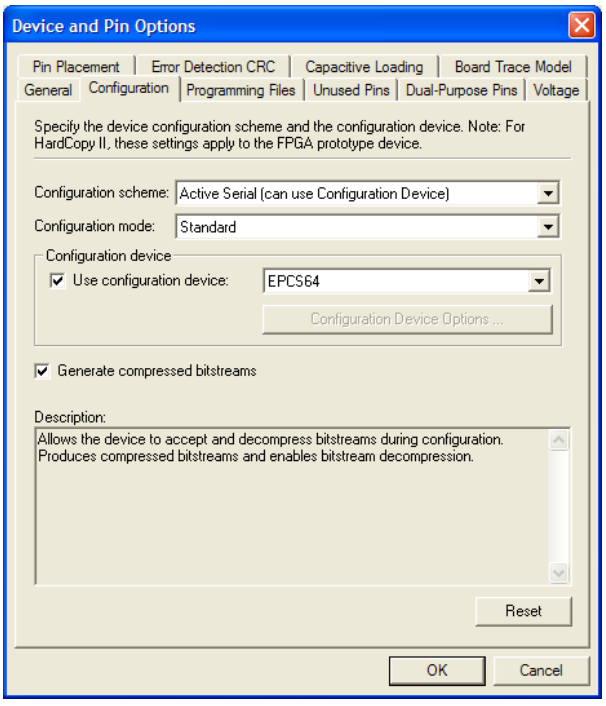
There two methods for enabling compression for Cyclone III bitstreams in the Quartus II software are:

- Before design compilation (via the Compiler Settings menu)
- After design compilation (via the **Convert Programming Files** window)

To enable compression in the project's compiler settings, perform the following steps in the Quartus II software:

1. On the Assignments menu, click **Device**. The **Settings** dialog box appears.
2. Click **Device and Pin Options**. The **Device and Pin Options** dialog box appears.
3. Click the **Configuration** tab.
4. Turn on **Generate compressed bitstreams** (Figure 10–1).
5. Click **OK**.
6. In the **Settings** dialog box, click **OK**.

**Figure 10–1.** Enabling Compression for Cyclone III Bitstreams in Compiler Settings




You can also enable compression when creating programming files from the **Convert Programming Files** window.

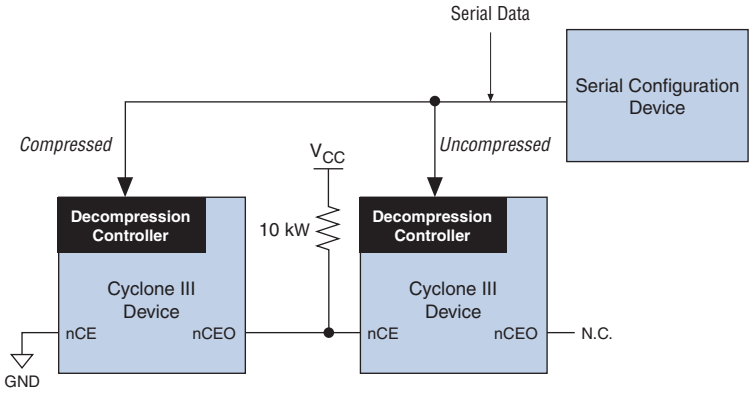
1. On the File menu, click **Convert Programming Files**.

2. Under **Output programming file**, from the drop-down menu, select your desired file type.
3. If you select Programmer Object File (**.pof**), you must specify a configuration device, directly under the file type.
4. In the **Input files to convert** box, select **SOF Data**.
5. Click **Add File** to browse to the Cyclone III device SRAM Object file (**.sof**) or files.
6. On the **Convert Programming Files** window, select the **.pof** file you added to SOF Data and click **Properties**.
7. On the **SOF File Properties** dialog box, turn on **Compression**.

When multiple Cyclone III devices are cascaded, you can selectively enable the compression feature for each device in the chain.

Figure 10–2 shows a chain of two Cyclone III devices. The first Cyclone III device has compression enabled and receives a compressed bitstream from the configuration device. The second Cyclone III device has the compression feature disabled and receives uncompressed data.

**Figure 10–2.** Compressed and Uncompressed Configuration Data in the Same Configuration File




You can generate programming files for this setup from the **Convert Programming Files** dialog box in the Quartus II software, from the File menu.

## Remote System Upgrade

Cyclone III devices support remote update mode when using the remote system upgrade feature. You can enable or disable remote update mode with an option setting in the Quartus II software. Remote system upgrades help deliver feature enhancements and bug fixes without costly recalls, reduce time-to-market, and extend product life.

Cyclone III devices support remote update in the AS and AP configuration schemes. You can implement remote update in conjunction with real-time decompression of configuration data if you need to save configuration memory space in the serial configuration device with the AS configuration scheme.

For more information about the remote system upgrade feature, refer to the *Remote System Upgrade with Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

# Configuration Requirements

## Power-On Reset Circuit

The POR circuit keeps the device in reset state until the power supply voltage levels have stabilized on power-up. Upon power-up, the device does not release nSTATUS until $V_{CCINT}$, $V_{CCA}$, and $V_{CCIO}$ of banks 1, 6, 7, and 8 are above the device's POR trip point. On power-up, $V_{CCINT}$ and $V_{CCA}$ are monitored for brown-out conditions.

$V_{CCA}$ is the analog power to the phase-locked loop (PLL).

In Cyclone III devices, you can select between a fast POR time or standard POR time depending on the MSEL pin settings. The fast POR time is 3 ms < $T_{POR}$ < 9 ms for fast configuration time. The standard POR time is 50 ms < $T_{POR}$ < 200 ms, which has a lower power-ramp rate. In both cases, you can extend the POR time by using an external component to assert the nSTATUS pin low.

Table 10–5 shows the supported POR times for each configuration scheme.

**Table 10–5.** Cyclone III Supported Power-On Reset Times Across Configuration Schemes *(Note 3)*

| Configuration Scheme | Fast POR Time (3 ms < $T_{POR}$ < 9 ms) | Standard POR Time (50 ms < $T_{POR}$ < 200 ms) | Configuration Voltage Standard *(1)* |
|---|---|---|---|
| Passive Serial Standard (PS Standard POR) | — | ✓ | 3.3/3.0/2.5 V |
| Active Serial Standard (AS Standard POR) | — | ✓ | 3.3 V |
| Active Serial Standard (AS Standard POR) | — | ✓ | 3.0/2.5 V |
| Active Serial Fast (AS Fast POR) | ✓ | — | 3.0/2.5 V |
| Active Parallel ×16 Fast (AP Fast POR) | ✓ | — | 3.3 V |
| Active Parallel ×16 Fast (AP Fast POR) | ✓ | — | 1.8 V |
| Active Parallel ×16 (AP Standard POR) | — | ✓ | 3.3 V |
| Active Parallel ×16 (AP Standard POR) | — | ✓ | 1.8 V |
| Active Parallel ×16 (AP Standard POR) | — | ✓ | 3.0/2.5 V |
| Passive Serial Fast (PS Fast POR) | ✓ | — | 3.3/3.0/2.5 V |
| Active Serial Fast (AS Fast POR) | ✓ | — | 3.3 V |
| Fast Passive Parallel Fast (FPP Fast POR) | ✓ | — | 3.3/3.0/2.5 V |
| Fast Passive Parallel Fast (FPP Fast POR) | ✓ | — | 1.8/1.5 V |
| JTAG-based configuration | *(2)* | *(2)* | — |

**Notes to Table 10–5:**

(1) Configuration voltage standard is applied to the $V_{CCIO}$ supply of the bank in which the configuration pins reside.

(2) JTAG-based configuration takes precedence over other configuration schemes, which means MSEL pin settings are ignored. However, the POR time is dependent on the MSEL pin settings.

(3) Connect the MSEL pins to $V_{CCA}$ or GND depending on the MSEL pin settings.

In some applications, it may be necessary for a device to wake up very quickly to begin operation. The Cyclone III device family offers the fast POR time option to support fast wake-up time applications. The fast POR time option has stricter power-up requirements compared to the standard POR time option. You can select either the fast POR option or the standard POR option using the MSEL pin settings.

The fast POR time feature in Cyclone III devices is similar to the Fast-On feature in Cyclone II devices designated with an "A" in the ordering code.

The Cyclone III devices' fast wake-up time meets the requirement of common bus standards in automotive applications, such as Media Orientated Systems Transport (MOST) and Controller Area Network (CAN).

For more information about wake-up time and POR circuit, refer to the *Hot Socketing and Power-On Reset* chapter in volume 1 of the *Cyclone III Device Handbook*.

## Configuration and JTAG Pin I/O Requirements

Cyclone III devices are manufactured using TSMC's 65-nm low-k dielectric process. Although Cyclone III devices use TSMC 2.5-V transistor technology in I/O buffers, the devices are compatible and able to interface with 2.5-, 3.0-, and 3.3-V configuration voltage standards. However, you must follow specific requirements when interfacing Cyclone III devices with 2.5-, 3.0-, and 3.3-V configuration voltage standards.

All I/O inputs must maintain a maximum AC voltage of 4.1 V. When using a serial configuration device in the AS configuration scheme, you must connect a 25-Ω series resistor at the near end of the serial configuration device for DATA[0]. When cascading Cyclone III devices in a multi-device configuration, you must connect repeater buffers between the Cyclone III master and slave device or the devices for DATA and DCLK. The output resistance of the repeater buffers must fit the maximum overshoot equation given by:

**Equation 10–1.**

$$0.8Z_O \leq R_E \leq 1.8Z_O$$

In this Equation 10–1, $Z_O$ is the transmission line impedance and $R_E$ is the equivalent resistance of the output buffer.

# Active Serial Configuration (Serial Configuration Devices)

In the AS configuration scheme, Cyclone III devices are configured using a serial configuration device. These configuration devices are low-cost devices with non-volatile memories that feature a simple four-pin interface and a small form factor. These features make serial configuration devices an ideal low-cost configuration solution.

For more information about serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS16, EPCS64, and EPCS128) Data Sheet* in volume 2 of the *Configuration Handbook*.

In Cyclone III devices, the active master clock frequency runs at a maximum of 40 MHz, and typically at 30 MHz. Cyclone III devices only work with serial configuration devices that support up to 40 MHz. Existing batches of EPCS4 manufactured on 0.15 µ process geometry support AS configuration in Cyclone III devices up to 40 MHz. However, batches of EPCS4 manufactured on 0.18 µ process geometry support only up to 20 MHz. EPCS16, EPCS64, and EPCS128 are not affected.

For more information about product traceability and transition date to differentiate between 0.15 µ process geometry and 0.18 µ process geometry EPCS4 serial configuration devices, refer to *PCN 0514 Manufacturing Changes on EPCS Family*.

Serial configuration devices provide a serial interface to access configuration data. During device configuration, Cyclone III devices read configuration data via the serial interface, decompress data if necessary, and configures their SRAM cells. This scheme is referred to as the AS configuration scheme because the device controls the configuration interface. This scheme contrasts with the PS configuration scheme, where the external host controls the interface.

The Cyclone III decompression and remote system upgrade features are available when configuring your Cyclone III device using the AS configuration scheme.

Table 10–6 shows the MSEL pin settings when using the AS configuration scheme with different configuration voltage standards.

**Table 10–6.** Cyclone III MSEL Pin Settings for AS Configuration Schemes *(Note 7)*

| Configuration Scheme | MSEL3 *(5)* | MSEL2 | MSEL1 | MSEL0 | Configuration Voltage Standard *(3)* |
|---|---|---|---|---|---|
| Active Serial Standard (AS Standard POR) *(1)*, *(2)* | 0 | 0 | 1 | 0 | 3.3 V *(4)* |
| Active Serial Standard (AS Standard POR) *(1)*, *(2)* | 0 | 0 | 1 | 1 | 3.0/2.5 V *(4)* |
| Active Serial Fast (AS Fast POR) *(1)*, *(2)*, *(6)* | 0 | 1 | 0 | 0 | 3.0/2.5 V *(4)* |
| Active Serial Fast (AS Fast POR) *(1)*, *(2)* | 1 | 1 | 0 | 1 | 3.3 V *(4)* |

**Notes to Table 10–6:**

(1) These schemes support the remote system upgrade feature. Remote update mode is supported when using the remote system upgrade feature. You can enable or disable remote update mode with an option setting in the Quartus II software. For more information about the remote system upgrade feature, refer to the *Remote System Upgrade with Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

(2) These schemes support data decompression.

(3) The configuration voltage standard is applied to the $V_{CCIO}$ supply of the bank in which the configuration pins reside.

(4) You must follow specific requirements when interfacing Cyclone III devices with 2.5-, 3.0-, and 3.3-V configuration voltage standards (for more information about the requirements, refer to "Configuration and JTAG Pin I/O Requirements").

(5) Some of the smaller Cyclone III devices or package options do not support the AP configuration scheme and do not have the `MSEL[3]` pin (for more information about the supported configuration schemes across device densities and package options, refer to Table 10–2).

(6) AS Fast POR with a 2.5- or 3.0-V configuration voltage standard is not available for devices that do not have the `MSEL[3]` pin (for more information about devices that support AS Fast POR, refer to Table 10–2).

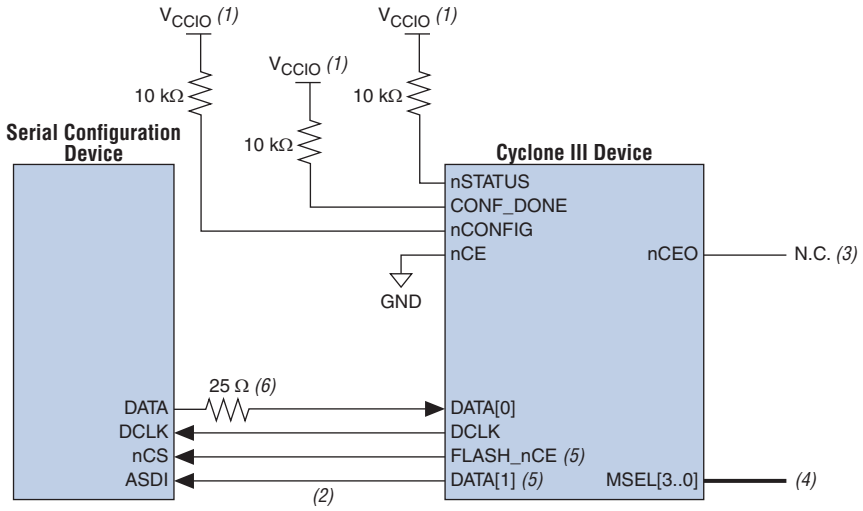
(7) Connect the MSEL pins to $V_{CCA}$ or GND depending on the MSEL pin settings.

## Single-Device AS Configuration

The four-pin interface of serial configuration devices consists of a serial clock input (DCLK), serial data output (DATA), AS data input (ASDI), and an active-low chip select (nCS).

This four-pin interface connects to Cyclone III device pins, as shown in Figure 10–3.

**Figure 10–3.** Single-Device AS Configuration




**Notes to Figure 10–3:**

(1) Connect the pull-up resistors to the $V_{CCIO}$ supply of the bank in which the pin resides.

(2) Cyclone III devices use the DATA[1] -to-ASDI path to control the configuration device.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 10–6. Connect the MSEL pins directly to $V_{CCA}$ or GND.

(5) These are dual-purpose I/O pins. The FLASH_nCE pin functions as the nCSO pin in the AS configuration scheme. The DATA[1] pin functions as the ASDO pin in the AS configuration scheme.

(6) Connect the series resistor at the near end of the serial configuration device.

When connecting a serial configuration device to the Cyclone III device in a single-device AS configuration, you must connect a 25-Ω series resistor at the near end of the serial configuration device for DATA[0]. The 25-Ω resistor in the series works to minimize the driver impedance mismatch with the board trace and reduce the overshoot seen at the Cyclone III DATA[0] input pin.

In a single-device AS configuration, the maximum board loading and board trace length between the supported serial configuration device and the Cyclone III device must follow the recommendations in Table 10–8.

If you use the AS configuration scheme for Cyclone III devices, the $V_{CCIO}$ of I/O bank 1 must be 3.3, 3.0, or 2.5 V. Altera does not recommend using the level shifter between a serial configuration device and the Cyclone III device in the AS configuration scheme.

For information about electrical specification compatibility between the Cyclone III and the EPCS device at various configuration voltage levels, refer to *AN 523: Cyclone III Configuration Interface Guidelines with EPCS Devices* application note.

Upon power-up, Cyclone III devices go through a POR. POR delay depends on the MSEL pin settings, which corresponds to the configuration scheme that you selected. Depending on the configuration scheme, either a fast or standard POR time is available. The fast POR time is 3 ms < $T_{POR}$ < 9 ms for a fast configuration time. The standard POR time is 50 ms < $T_{POR}$ < 200 ms, which has a lower power-ramp rate. During POR, the device resets, holds nSTATUS and CONF_DONE low, and tri-states all user I/O pins. When the device successfully exits POR, all user I/O pins continue to be tri-stated. The user I/O pins and dual-purpose I/O pins have weak pull-up resistors, which are always enabled (after POR) before and during configuration.

The value of the weak pull-up resistors on the I/O pins that are on before and during configuration can be found in the *DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*.

The three stages of the configuration cycle are reset, configuration, and initialization. When nCONFIG or nSTATUS are low, the device is in reset. After POR, the Cyclone III device releases nSTATUS, which is pulled high by an external 10-kΩ pull-up resistor and enters configuration mode.

To begin configuration, power $V_{CCINT}$, $V_{CCA}$, and $V_{CCIO}$ voltages (for the banks in which the configuration and JTAG pins reside) to the appropriate voltage levels.

The serial clock (DCLK) generated by the Cyclone III device controls the entire configuration cycle and provides timing for the serial interface. Cyclone III devices use an 40-MHz internal oscillator to generate DCLK. There is some variation in the internal oscillator frequency because of the process, voltage, and temperature conditions in Cyclone III devices. The internal oscillator is designed such that its maximum frequency is guaranteed to meet EPCS device specifications.

EPCS1 does not support Cyclone III devices because of its insufficient memory capacity.

For information about serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS16, EPCS64, and EPCS128) Data Sheet* chapter in volume 2 of the *Configuration Handbook*.

Table 10–7 shows active serial DCLK output frequency.

**Table 10–7.** Active Serial DCLK Output Frequency

| Oscillator | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|
| 40 MHz | 20 | 30 | 40 | MHz |

In the AS configuration scheme, the serial configuration device latches input and control signals on the rising edge of DCLK and drives out configuration data on the falling edge. Cyclone III devices drive out control signals on the falling edge of DCLK and latch configuration data on the falling edge of DCLK.

The FLASH_nCE and DATA[1] pins are dual-purpose I/O pins. The FLASH_nCE pin functions as the nCSO pin in the AS configuration scheme. The DATA[1] pin functions as the ASDO pin in the AS configuration scheme.

In configuration mode, the Cyclone III device enables the serial configuration device by driving the FLASH_nCE output pin low, which connects to the chip select (nCS) pin of the configuration device. The Cyclone III device uses the serial clock (DCLK) and serial data output (DATA[1]) pins to send operation commands and/or read address signals to the serial configuration device. The configuration device provides data on its serial data output (DATA) pin, which connects to the DATA[0] input of the Cyclone III device.

After all configuration bits are received by the Cyclone III device, it releases the open-drain CONF_DONE pin, which is pulled high by an external 10-kΩ resistor. Initialization begins only after the CONF_DONE signal reaches a logic-high level. All AS configuration pins (DATA[0], DCLK, FLASH_nCE, and DATA[1]) have weak internal pull-up resistors that are always active. After configuration, these pins are set as input tri-stated and are driven high by weak internal pull-up resistors. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize.

In Cyclone III devices, the initialization clock source is either the 10-MHz (typical) internal oscillator (separate from the active serial internal oscillator) or the optional CLKUSR pin. By default, the internal oscillator is the clock source for initialization. If you use the internal oscillator, the Cyclone III device provides itself with enough clock cycles for proper initialization. The advantage of using the internal oscillator is that you do not need to send additional clock cycles from an external source to the CLKUSR pin during the initialization stage. Additionally, you can use the CLKUSR pin as a user I/O pin. The timing parameters $t_{CF2CD}$, $t_{CF2ST0}$, $t_{CFG}$, $t_{STATUS}$, $t_{CF2ST1}$, and $t_{CD2UM}$ are identical to the one for PS mode which are shown in Table 10–13.

You also have the flexibility to synchronize initialization of multiple devices or to delay initialization with the CLKUSR option. Using the CLKUSR pin allows you to control when your device enters user mode. You can delay the device from entering user mode for an indefinite amount of time. Turn on the **Enable user-supplied start-up clock** (**CLKUSR**) option in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. When you **enable** the **user supplied start-up clock** option, the CLKUSR pin is the initialization clock source. Supplying a clock on CLKUSR does not affect the configuration process. After all configuration data is accepted and CONF_DONE goes high, Cyclone III devices require 3,185 clock cycles to initialize properly and enter user mode. Cyclone III devices support a CLKUSR $f_{MAX}$ of 133 MHz.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user mode with a low-to-high transition. The **Enable INIT_DONE Output** option is available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. If the INIT_DONE pin is used, it will be high due to an external 10-kΩ pull-up resistor when nCONFIG is low and during the beginning of configuration. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and pulled high. This low-to-high transition signals that the device has entered user mode. When initialization is complete, the device enters user mode. In user mode, the user I/O pins no longer have weak pull-up resistors and function as assigned in your design.

If an error occurs during configuration, Cyclone III devices assert the nSTATUS signal low, indicating a data frame error, and the CONF_DONE signal stays low. If the **Auto-restart configuration after error** option (available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box) is turned on, the Cyclone III device resets the configuration device by pulsing FLASH_nCE, releases nSTATUS after a reset time-out period (maximum of 230 µs), and retries configuration. If this option is turned off, the system must monitor nSTATUS for errors and then pulse nCONFIG low for at least 500 ns to restart configuration.

When the Cyclone III device is in user mode, you can initiate reconfiguration by pulling the nCONFIG pin low. The nCONFIG pin needs to be low for at least 500 ns. When nCONFIG is pulled low, the Cyclone III device resets. The Cyclone III device also pulls nSTATUS and CONF_DONE low and all I/O pins are tri-stated. When nCONFIG returns to a logic-high level and nSTATUS is released by the Cyclone III device, reconfiguration begins.

If you use the optional CLKUSR pin, and the nCONFIG pin is pulled low to restart configuration during device initialization, ensure the CLKUSR pin continues to toggle during the time nSTATUS is low (a maximum of 230 µs).

For more information about configuration issues, refer to the *Debugging Configuration Problems* chapter in volume 2 of the *Configuration Handbook* and the FPGA Configuration Troubleshooter on the Altera website (www.altera.com).

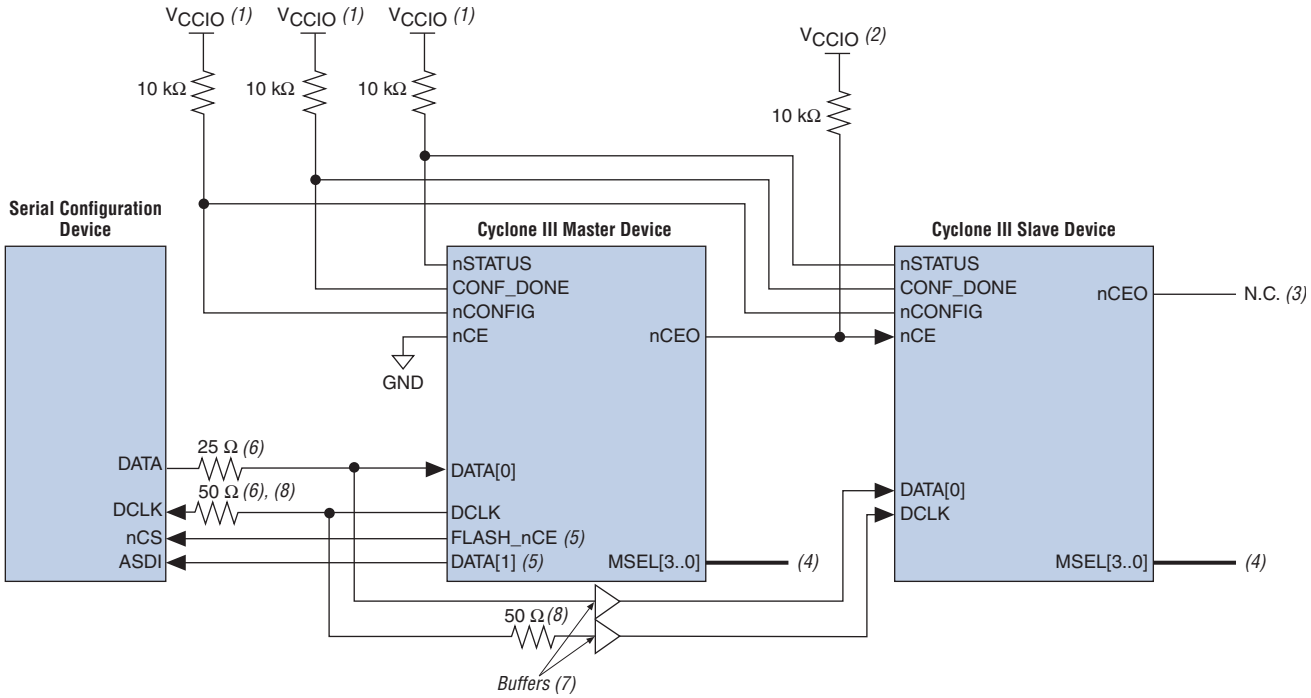
## Multi-Device AS Configuration

You can configure multiple Cyclone III devices using a single-serial configuration device. You can cascade multiple Cyclone III devices using the chip-enable (nCE) and chip-enable-out (nCEO) pins. The first device in the chain must have its nCE pin connected to GND. You must connect its nCEO pin to the nCE pin of the next device in the chain. Use an external 10-kΩ pull-up resistor to pull the nCEO signal high to its $V_{CCIO}$ level to help the internal weak pull-up resistor. When the first device captures all of its configuration data from the bitstream, it drives the nCEO pin low, enabling the next device in the chain. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration if the last device in the chain is a Cyclone III device. The nCONFIG, nSTATUS, CONF_DONE, DCLK, and DATA[0] pins of each device in the chain are connected (refer to Figure 10–4).

The first Cyclone III device in the chain is the configuration master and controls configuration of the entire chain. You must connect its MSEL pins to select the AS configuration scheme. The remaining Cyclone III devices are configuration slaves; you must connect their MSEL pins to select the PS configuration scheme. Any other Altera device that supports PS configuration can also be part of the chain as a configuration slave.

Figure 10–4 shows the pin connections for this setup.

**Figure 10–4.** Multi-Device AS Configuration




**Notes to Figure 10–4:**

(1) Connect the pull-up resistors to the $V_{CCIO}$ supply of the bank in which the pin resides.

(2) Connect the pull-up resistor to the $V_{CCIO}$ supply voltage of I/O bank in which the `nCE` pin resides.

(3) You can leave the `nCEO` pin unconnected or use it as a user I/O pin when it does not feed another device's `nCE` pin.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. You must set the Cyclone III master device in AS mode and the slave devices in PS mode. To connect `MSEL[3..0]` for the master device in AS mode, refer to Table 10–6. To connect `MSEL[3..0]` for the slave devices in PS mode, refer to Table 10–12. Connect the MSEL pins directly to $V_{CCA}$ or GND.

(5) These are dual-purpose I/O pins. The `FLASH_nCE` pin functions as the `nCSO` pin in the AS configuration scheme. The `DATA[1]` pin functions as the `ASDO` pin in the AS configuration scheme.

(6) Connect the series resistor at the near end of the serial configuration device.

(7) Connect the repeater buffers between the Cyclone III master and slave device or devices for `DATA[0]` and `DCLK`. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

(8) The 50-Ω series resistors are optional if the 3.3-V configuration voltage standard is applied. For optimal signal integrity, connect these 50-Ω series resistors if the 2.5- or 3.0-V configuration voltage standard is applied.

When connecting a serial configuration device to the Cyclone III device in a multi-device AS configuration, you must connect a 25-Ω series resistor at the near end of the serial configuration device for `DATA[0]`.

In a multi-device AS configuration, the board trace length between the serial configuration device to the master Cyclone III device needs to follow the recommendations in Table 10–8. Additionally, you must connect the repeater buffers between the Cyclone III master and slave device or devices for `DATA[0]` and `DCLK`. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

As shown in Figure 10–4, the nSTATUS and CONF_DONE pins on all target devices are connected together with external pull-up resistors. These pins are open-drain bidirectional pins on the devices. When the first device asserts nCEO (after receiving all of its configuration data), it releases its CONF_DONE pin. However, the subsequent devices in the chain keep this shared CONF_DONE line low until they have received their configuration data. When all target devices in the chain have received their configuration data and have released CONF_DONE, the pull-up resistor drives a high level on this line and all devices simultaneously enter initialization mode.

If an error occurs at any point during configuration, the nSTATUS line is driven low by the failing device. If you enable the **Auto-restart configuration after error** option, reconfiguration of the entire chain begins after a reset time-out period (a maximum of 230 µs). If you turn off the **Auto-restart configuration after error** option, the external system must monitor nSTATUS for errors and then pulse nCONFIG low to restart the configuration. The external system can pulse nCONFIG if it is under system control rather than tied to $V_{CCIO}$.

While you can cascade Cyclone III devices, serial configuration devices cannot be cascaded or chained together.

If the configuration bitstream size exceeds the capacity of a serial configuration device, you must select a larger configuration device, enable the compression feature, or both. When configuring multiple devices, the size of the bitstream is the sum of the individual devices' configuration bitstreams.

## Configuring Multiple Cyclone III Devices with the Same Design

Certain designs require you to configure multiple Cyclone III devices with the same design through a configuration bitstream or a **.sof** file. You can do this through one of two methods, as described in this section. For both methods, serial configuration devices cannot be cascaded or chained together.

### Multiple SRAM Object Files

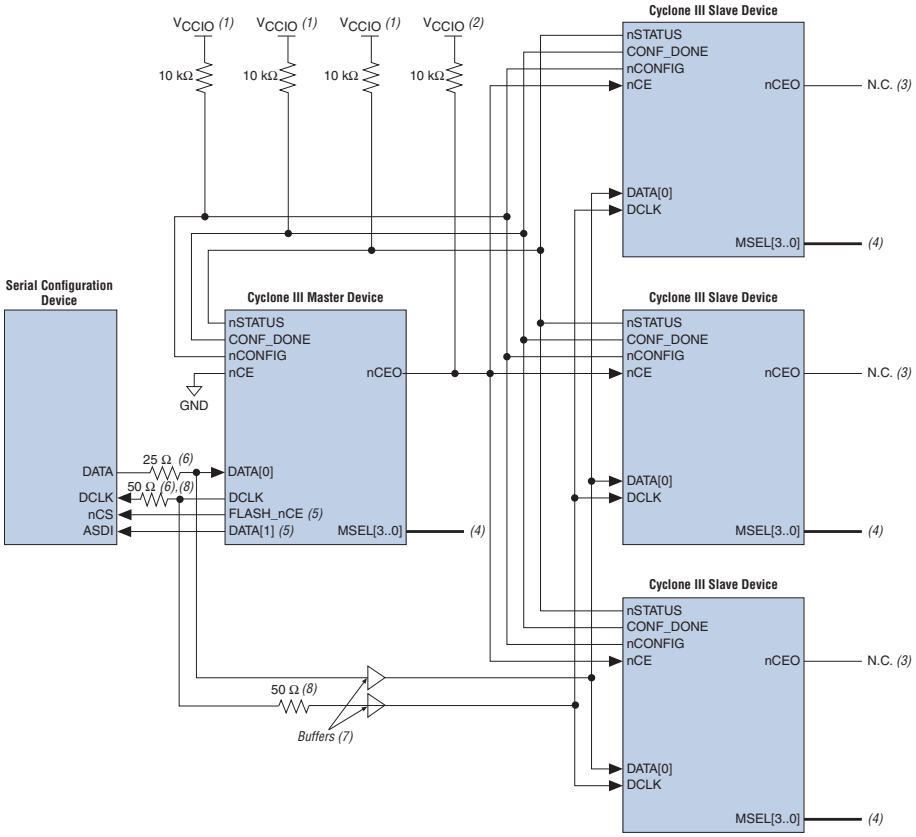
In the first method, two copies of the **.sof** files are stored in the serial configuration device. Use the first copy to configure the master Cyclone III device and the second copy to configure all remaining slave devices concurrently. All slave devices must be the same density and package. The setup is similar to Figure 10–4, in which the master is set up in active serial mode and the slave devices are set up in passive serial mode.

To configure four identical Cyclone III devices with the same **.sof** files, you must set up the chain similar to the example shown in Figure 10–5. The first device is the master device and its MSEL pins need to be set to select AS configuration. The other three slave devices are set up for concurrent configuration and their MSEL pins need to be set to select PS configuration. The nCEO pin from the master device drives the nCE input pins on all three slave devices. The DATA and DCLK pins connect in parallel to all four devices. During the first configuration cycle, the master device reads its configuration data from the serial configuration device while holding nCEO high. After completing its configuration cycle, the master drives nCE low and transmits the second copy of the configuration data to all three slave devices, configuring them simultaneously.

The advantage of using the setup in Figure 10–5 is that you can have a different **.sof** file for the Cyclone III master device. However, all the Cyclone III slave devices must be configured with the same **.sof** file. You can either compress or uncompress the **.sof** files in this configuration method.

You can still use this method if the master and slave Cyclone III devices use the same **.sof** file.

**Figure 10–5.** Multi-Device AS Configuration in which Devices Receive the Same Data with Multiple SRAM Object Files




**Notes to Figure 10–5:**

(1) Connect the pull-up resistors to the $V_{CCIO}$ supply of the bank in which the pin resides.

(2) Connect the pull-up resistor to the $V_{CCIO}$ supply voltage of I/O bank in which the `nCE` pin resides.

(3) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed another device's `nCE` pin.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. You must set the Cyclone III master device in AS mode and the slave devices in PS mode. To connect `MSEL[3..0]` for the master device in AS mode, refer to Table 10–6. To connect `MSEL[3..0]` for the slave devices in PS mode, refer to Table 10–12. Connect the MSEL pins directly to $V_{CCA}$ or GND.

(5) These are dual-purpose I/O pins. The `FLASH_nCE` pin functions as the `nCSO` pin in the AS configuration scheme. The `DATA[1]` pin functions as the `ASDO` pin in the AS configuration scheme.

(6) Connect the series resistor at the near end of the serial configuration device.

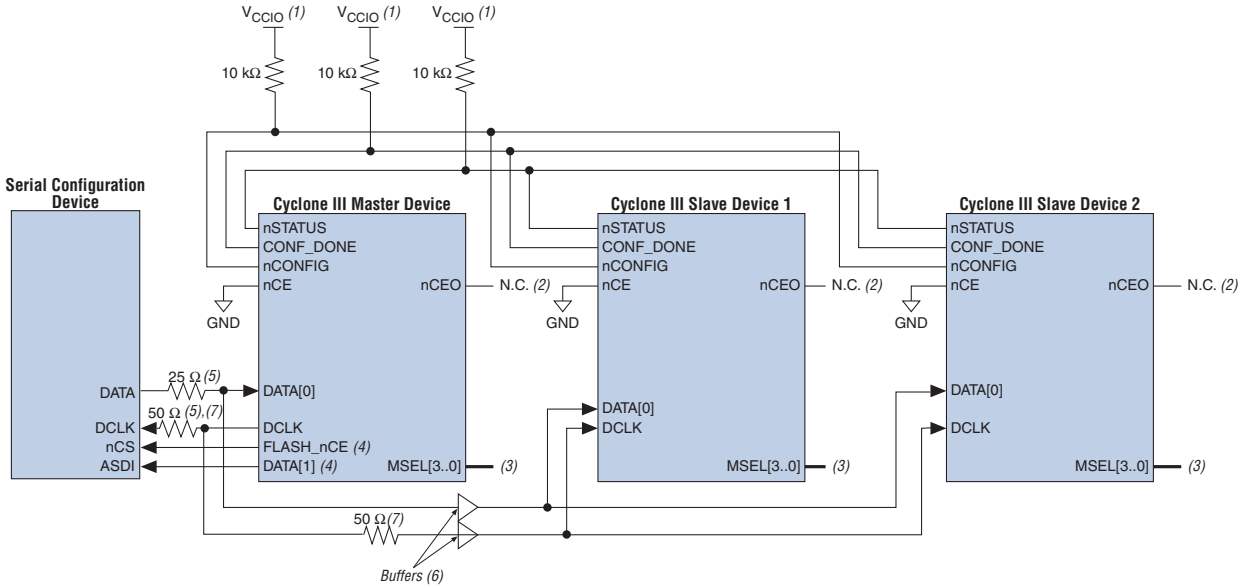
(7) Connect the repeater buffers between the Cyclone III master and slave device or devices for `DATA[0]` and `DCLK`. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

(8) The 50-Ω series resistors are optional if the 3.3-V configuration voltage standard is applied. For optimal signal integrity, connect these 50-Ω series resistors if the 2.5- or 3.0-V configuration voltage standard is applied.

## Single SRAM Object File

The second method configures both the master and slave Cyclone III devices with the same **.sof** file. The serial configuration device stores one copy of the **.sof** file. This setup is shown in Figure 10–6 where the master is setup in AS mode and the slave devices are setup in PS mode. You must setup one or more slave devices in the chain. All the slave devices must be setup in the same way as shown in Figure 10–6.

**Figure 10–6.** Multi-Device AS Configuration in which Devices Receive the Same Data with a Single SRAM Object File




**Notes to Figure 10–6:**

(1) Connect the pull-up resistors to the $V_{CCIO}$ supply of the bank in which the pin resides.

(2) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

(3) The MSEL pin settings vary for different configuration voltage standards and POR time. You must set the Cyclone III master device in AS mode and the slave devices in PS mode. To connect MSEL[3..0] for the master device in AS mode, refer to Table 10–6. To connect MSEL[3..0] for the slave devices in PS mode, refer to Table 10–12. Connect the MSEL pins directly to $V_{CCA}$ or GND.

(4) These are dual-purpose I/O pins. The FLASH_nCE pin functions as the nCSO pin in the AS configuration scheme. The DATA[1] pin functions as the ASDO pin in the AS configuration scheme.

(5) Connect the series resistor at the near end of the serial configuration device.

(6) Connect the repeater buffers between the Cyclone III master and slave device or devices for DATA[0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

(7) The 50-Ω series resistors are optional if the 3.3-V configuration voltage standard is applied. For optimal signal integrity, connect these 50-Ω series resistors if the 2.5- or 3.0-V configuration voltage standard is applied.

In this setup, all the Cyclone III devices in the chain are connected for concurrent configuration. This can reduce the AS configuration time because all the Cyclone III devices are configured in one configuration cycle. Connect the nCE input pins of all the Cyclone III devices to ground. You can either leave the nCEO output pins on all the Cyclone III devices unconnected or use the nCEO output pins as normal user I/O pins. The DATA and DCLK pins are connected in parallel to all the Cyclone III devices.

You need to put a buffer before the DATA and DCLK output from the master Cyclone III device to avoid signal strength and signal integrity issues. The buffer should not significantly change the DATA-to-DCLK relationships or delay them with respect to other AS signals (ASDI and nCS). Also, the buffer should only drive the slave Cyclone III devices, so that the timing between the master Cyclone III device and serial configuration device is unaffected.

This configuration method supports both compressed and uncompressed **.sof** files. Therefore, if the configuration bitstream size exceeds the capacity of a serial configuration device, you can enable the compression feature in the **.sof** file used or you can select a larger serial configuration device.

## Guidelines for Connecting Serial Configuration Device to Cyclone III Device on AS Interface

For single- and multi-device AS configurations, the board trace length and loading between the supported serial configuration device and Cyclone III device must follow the recommendations in Table 10–8.

**Table 10–8.** Maximum Trace Length and Loading for AS Configuration

| Cyclone III AS Pins | Maximum Board Trace Length from Cyclone III Device to Serial Configuration Device (Inches) | Maximum Board Load (pF) |
|---|---|---|
| DCLK | 10 | 15 |
| DATA[0] | 10 | 30 |
| FLASH_nCE | 10 | 30 |
| DATA[1] | 10 | 30 |

## Estimating AS Configuration Time

Active serial configuration time is dominated by the time it takes to transfer data from the serial configuration device to the Cyclone III device. This serial interface is clocked by the Cyclone III DCLK output (generated from an internal oscillator).

As listed in Table 10–7, the DCLK minimum frequency when using the 40-MHz oscillator is 20 MHz (50 ns). Therefore, the maximum configuration time estimate for EP3C10 (3,000,000 bits of uncompressed data) is:

**Equation 10–2.**

$$\text{RBF Size} \times \left(\frac{\text{maximum DCLK period}}{1 \text{ bit}}\right) = \text{estimated maximum configuration time}$$

**Equation 10–3.**

$$3{,}000{,}000 \text{ bits} \times \left(\frac{50 \text{ ns}}{1 \text{ bit}}\right) = 150 \text{ ms}$$

To estimate the typical configuration time, use the typical DCLK period as listed in Figure 10–7. With a typical DCLK period of 33.33 ns, the typical configuration time is 116.7 ms. Enabling compression reduces the amount of configuration data that is transmitted to the Cyclone III device, which also reduces configuration time. On average, compression reduces configuration time by 50%.

## Programming Serial Configuration Devices

Serial configuration devices are non-volatile, flash-memory-based devices. You can program these devices in-system using the USB-Blaster™or ByteBlaster II™ download cable. Alternatively, you can program them using the Altera Programming Unit (APU), supported third-party programmers, or a microprocessor with the SRunner software driver.

You can perform in-system programming of serial configuration devices via the AS programming interface. During in-system programming, the download cable disables device access to the AS interface by driving the nCE pin high. Cyclone III devices are also held in reset by a low level on nCONFIG. After programming is complete, the download cable releases nCE and nCONFIG, allowing the pull-down and pull-up resistors to drive GND and $V_{CC}$, respectively.

To perform in-system programming of a serial configuration device via the AS programming interface, the diodes and capacitors must be placed as close as possible to the Cyclone III device. Ensure the diodes and capacitors maintain a maximum AC voltage of 4.1 V (refer to Figure 10–7).

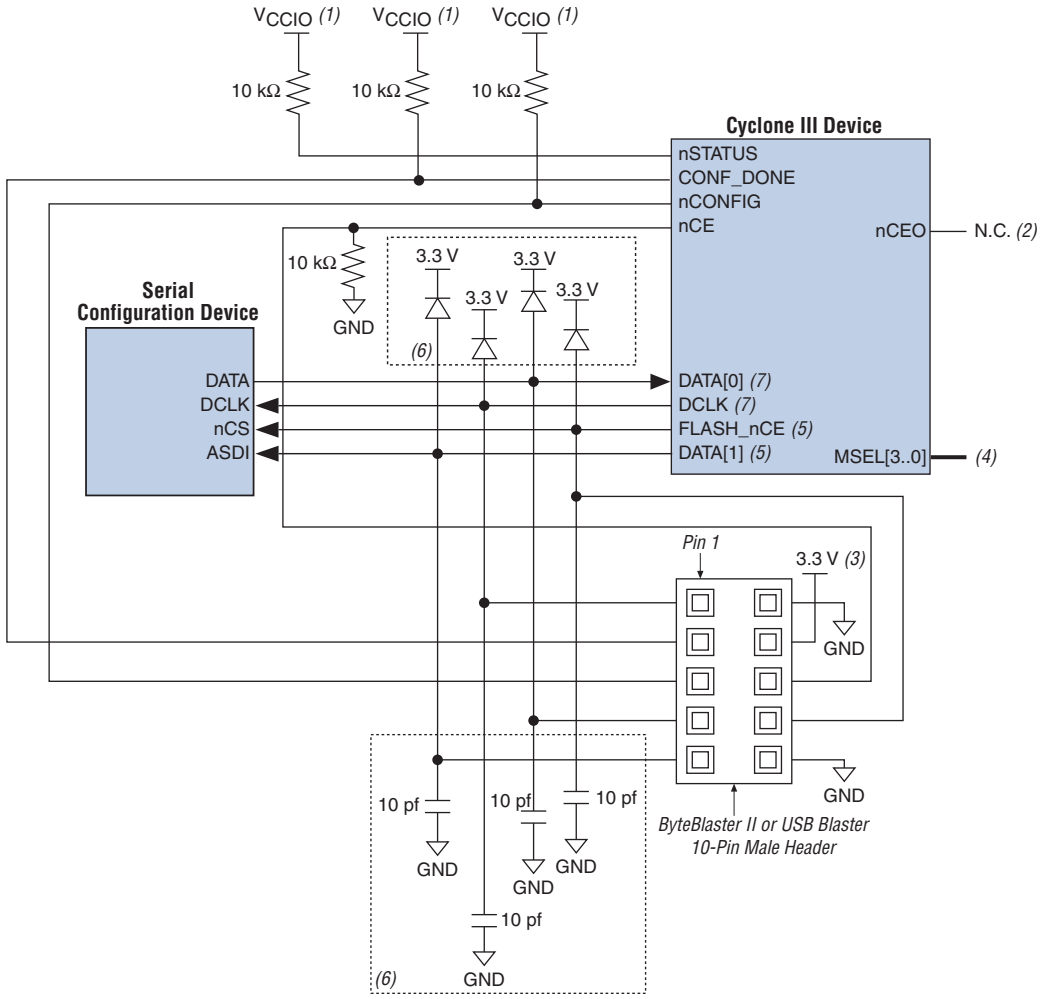
If you wish to use the same setup shown in Figure 10–7 to perform in-system programming of a serial configuration device and single- or multi-device AS configuration, you do not need a series resistor on the DATA line at the near end of the serial configuration device. The existing diodes and capacitors are sufficient.

Altera has developed the Serial FlashLoader (SFL), a JTAG-based in-system programming solution for Altera serial configuration devices. The SFL is a bridge design for the Cyclone III device that uses its JTAG interface to access the EPCS JTAG Indirect Configuration Device Programming (**.jic**) file and then uses the AS interface to program the EPCS device. Both the JTAG interface and AS interface are bridged together inside the SFL design (for more information about implementing the SFL with Cyclone III devices, refer to "Programming Serial Configuration Devices In-System Using the JTAG Interface").

For more information about the USB-Blaster download cable, refer to the *USB-Blaster Download Cable User Guide*. For more information about the ByteBlaster II cable, refer to the *ByteBlaster II Download Cable User Guide*.

Figure 10–7 shows the download cable connections to the serial configuration device.

**Figure 10–7.** In-System Programming of Serial Configuration Devices




**Notes to Figure 10–7:**

(1) Connect these pull-up resistors to the $V_{CCIO}$ supply of the bank in which the pin resides.

(2) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed other device's `nCE` pin.

(3) Power up the ByteBlaster II or USB-Blaster cable's $V_{CC}$ with the 3.3-V supply.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect `MSEL[3..0]`, refer to Table 10–6. Connect the MSEL pins directly to $V_{CCA}$ or ground.

(5) These are dual-purpose I/O pins. The `FLASH_nCE` pin functions as the `nCSO` pin in the AS configuration scheme. The `DATA[1]` pin functions as the `ASDO` pin in the AS configuration scheme.

(6) The diodes and capacitors must be placed as close as possible to the Cyclone III device. You must ensure the diodes and capacitors maintain a maximum AC voltage of 4.1 V. The external diodes and capacitors are required to prevent damage to the Cyclone III AS configuration input pins due to possible overshoot when programming the serial configuration device using a download cable. Altera recommends using the Schottky diode, which has a relatively lower forward diode voltage (VF) than the switching and Zener diodes, for effective voltage clamping.

(7) When cascading Cyclone III devices in a multi-device AS configuration, connect the repeater buffers between the Cyclone III master and slave device or devices for `DATA[0]` and `DCLK`. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

You can use the Quartus II software with the APU and appropriate configuration device programming adapter to program serial configuration devices. All serial configuration devices are offered in an 8- or 16-pin small outline integrated circuit (SOIC) package.

In production environments, serial configuration devices using multiple methods. You can use Altera programming hardware or other third-party programming hardware to program blank serial configuration devices before they are mounted onto PCBs. Alternatively, you can use an on-board microprocessor to program the serial configuration device in-system by porting the reference C-based software driver provided by Altera (that is, the SRunner software driver).

You can program a serial configuration device in-system by an external microprocessor using SRunner. SRunner is a software driver developed for embedded serial configuration device programming, which can be easily customized to fit in different embedded systems. SRunner is able to read a raw programming data (.**rpd**) file and write to the serial configuration devices. The serial configuration device programming time using SRunner is comparable to the programming time with the Quartus II software.

For more information about SRunner, refer to the *AN 418: SRunner: An Embedded Solution for Serial Configuration Device Programming* and the source code on the Altera website (www.altera.com).

For more information about programming serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS16, EPCS64, and EPCS128) Data Sheet* chapter in volume 2 of the *Configuration Handbook*.

## Active Parallel Configuration (Supported Flash Memories)

Cyclone III devices offer the AP configuration scheme for Altera's devices. In the AP configuration scheme, Cyclone III devices are configured using commodity 16-bit parallel flash memory. These external non-volatile configuration devices are industry standard microprocessor flash memories. The flash memories provide a fast interface to access configuration data. The speed-up in configuration time is mainly due to the 16-bit wide parallel data bus, which is used to retrieve data from the flash.

Some of the smaller Cyclone III devices or package options do not support the AP configuration scheme and do not have the `MSEL[3]` pin (for more information, refer to Table 10–2).

During device configuration, Cyclone III devices read configuration data via the parallel interface, and configure their SRAM cells. This scheme is referred to as the AP configuration scheme because the device controls the configuration interface. This scheme contrasts with the FPP configuration scheme, where an external host controls the interface.

The Cyclone III remote system upgrade feature is available when you configure your Cyclone III device using the AP configuration scheme.

Table 10–9 shows the MSEL pin settings when using the AP configuration scheme with different configuration voltage standard.

**Table 10–9.** Cyclone III MSEL Pin Settings for AP Configuration Schemes *(Note 7)*

| Configuration Scheme | MSEL3 *(5)* | MSEL2 | MSEL1 | MSEL0 | Configuration Voltage Standard *(4)* |
|---|---|---|---|---|---|
| Active Parallel ×16 Fast (AP Fast POR) *(1)*, *(2)*, *(3)* | 0 | 1 | 0 | 1 | 3.3 V *(6)* |
| Active Parallel ×16 Fast (AP Fast POR) *(1)*, *(2)*, *(3)* | 0 | 1 | 1 | 0 | 1.8 V |
| Active Parallel ×16 (AP Standard POR) *(1)*, *(2)*, *(3)* | 0 | 1 | 1 | 1 | 3.3 V *(6)* |
| Active Parallel ×16 (AP Standard POR) *(1)*, *(2)*, *(3)* | 1 | 0 | 0 | 0 | 1.8 V |
| Active Parallel ×16 (AP Standard POR) *(1)*, *(2)*, *(3)* | 1 | 0 | 1 | 1 | 3.0/2.5 V *(6)* |

**Notes to Table 10–9:**

(1) These schemes support the remote system upgrade feature. Remote update mode is supported when using remote system upgrade feature. You can enable or disable remote update mode with an option setting in the Quartus II software. For more information about the remote system upgrade feature, refer to the *Remote System Upgrade With Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

(2) Some of the smaller Cyclone III devices or package options do not support the AP configuration scheme (for more information, refer to Table 10–2).

(3) In the AP configuration scheme, the commodity parallel flash is used as configuration memory (for information about the supported families for the commodity parallel flash, refer to Table 10–10).

(4) Configuration voltage standard is applied to the $V_{CCIO}$ supply of the bank in which the configuration pins reside.

(5) Some of the smaller Cyclone III devices or package options do not support the AP configuration scheme and do not have the `MSEL[3]` pin (for more information about the supported configuration schemes across device densities and package options, refer to Table 10–2).

(6) You must follow specific requirements when interfacing Cyclone III devices with 2.5-, 3.0-, and 3.3-V configuration voltage standards (for more information about these requirements, refer to "Configuration and JTAG Pin I/O Requirements").

(7) You must connect the MSEL pins to $V_{CCA}$ or GND depending on the MSEL pin settings.

## AP Configuration Supported Flash Memories

The AP configuration controller in Cyclone III devices is designed to interface with the Numonyx StrataFlash® Embedded Memory P30 flash family and the Numonyx StrataFlash Embedded Memory P33 flash family, which are two industry standard flash families. Unlike serial configuration devices, both of the flash families supported in AP configuration scheme are designed to interface with microprocessors. By configuring from an industry standard microprocessor flash which allows access to the flash once in user mode, the AP configuration scheme allows you to combine configuration data and user data (microprocessor boot code) on the same flash memory.

The Numonyx P30 flash family and the P33 flash family are similar because both support a continuous synchronous burst read mode at 40 MHz `DCLK` frequency for reading data from the flash. Additionally, the Numonyx P30 and P33 flash families have identical pin-out and adopt similar protocols for data access.

☞ Cyclone III devices use a 40-MHz oscillator for the AP configuration scheme.

Table 10–10 shows the supported families of the commodity parallel flash for the AP configuration scheme.

**Table 10–10.** Cyclone III Supported Commodity Flash for AP Configuration Scheme *(Note 1)*

| Flash Memory Density | Numonyx P30 Flash Family *(2)* | Numonyx P33 Flash Family *(3)* |
|---|---|---|
| 64 Mbit | ✓ | ✓ |
| 128 Mbit | ✓ | ✓ |
| 256 Mbit | ✓ | ✓ |

**Notes to Table 10–10:**

(1) The AP configuration scheme only supports flash memory speed grades of 40 MHz and above. You must refer to the respective flash datasheets to check for supported speed grades and package options.

(2) 3.3- , 3.0-, 2.5-, and 1.8-V I/O options are supported for Numonyx P30 flash family.

(3) 3.3-, 3.0- and 2.5-V I/O options are supported for Numonyx P33 flash family.

The AP configuration of Cyclone III devices supports the Numonyx P30 and P33 family 64-Mbit, 128-Mbit, and 256-Mbit flash memories. Configuring Cyclone III devices from the Numonyx P30 and P33 family 512-Mbit flash memory is possible, but you need to properly drive the extra address and chip select pins as required by these flash memories.

You must refer to the respective flash datasheets to check for supported speed grades and package options. For example, the Numonyx P30 and P33 families have only a single speed grade at 40 MHz. The synchronous burst read operation is permitted with all options of the P30 and P33 256-Mbit Thin Small Outline Package (TSOP) package when the clock frequency does not exceed 40 MHz and the P30 device does not operate below a minimum $V_{CC}$ of 1.85 V. Therefore, the P30 and P33 FBGA packages and only 256-Mbit TSOP devices are supported for the AP configuration scheme at this time.

However, they do not support 40 MHz on the TSOP packages. Therefore, the P30 and P33 FBGA packages are supported for the AP configuration scheme while the TSOP packages are not supported.

The AP configuration scheme in Cyclone III devices support flash speed grades of 40 MHz and above. However, AP configuration for all these speed grades must be capped at 40 MHz. The advantage of the faster speed grades is realized when your design in the Cyclone III devices accesses flash memory in user mode.

For information about the operation of the Numonyx StrataFlash Embedded Memory P30 flash memories, search for the keyword "P30" on the Numonyx website (www.numonyx.com) to obtain the P30 family datasheet.

For information about the operation of the Numonyx StrataFlash Embedded Memory P33 flash memories, search for the keyword "P33" on the Numonyx website (www.numonyx.com) to obtain the P33 family datasheet.

## Single-Device AP Configuration

The three groups of interface pins supported in Numonyx P30 and P33 flash memories are the control pins, address pins, and data pins. In the AP configuration scheme, both of the supported parallel flash memories accept:

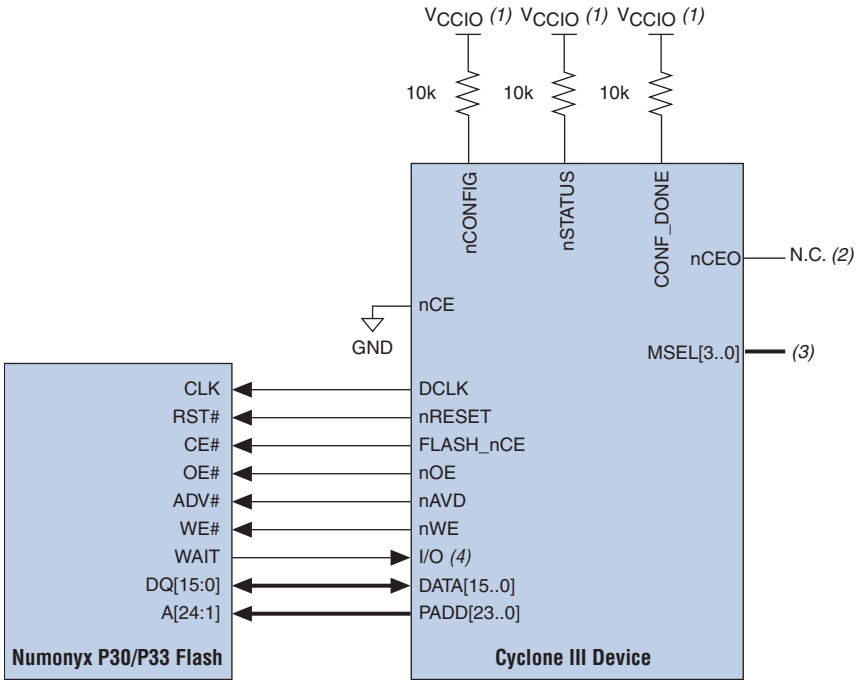
- DCLK, active-low reset (RST#)

- active-low chip enable (CE#)
- active-low output enable (OE#)
- active-low address valid (ADV#), and
- active-low write enable (WE#)

as control signals from the Cyclone III device. The supported parallel flash memories output a control signal (WAIT) to the Cyclone III device to indicate when synchronous data is ready on the data bus. The Cyclone III device has a 24-bit address bus which connects to the address bus (A[24:1]) of the flash memory. A 16-bit bidirectional data bus (DATA[15..0]) provides data transfer between the Cyclone III device and the flash memory.

The control signals from the Cyclone III device to flash memory include DCLK, nRESET, FLASH_nCE, nOE, nAVD, and nWE. The interface for the Numonyx P30 flash memory and P33 flash memory connects to Cyclone III device pins, as shown in Figure 10–8.

**Figure 10–8.** Single-Device AP Configuration Using Numonyx P30 and P33 Flash Memory




**Notes to Figure 10–8:**

(1) Connect the pull-up resistors to the $V_{CCIO}$ supply of the bank in which the pin resides.

(2) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

(3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 10–9. Connect the MSEL pins directly to $V_{CCA}$ or GND.

(4) AP configuration ignores the WAIT signal during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use normal I/O to monitor the WAIT signal from the Numonyx P30 or P33 flash.

In a single-device AP configuration, the maximum board loading and board trace length between supported parallel flash and the Cyclone III device must follow the recommendation in Table 10–11.

If you use the AP configuration scheme for Cyclone III devices, the $V_{CCIO}$ of I/O banks 1, 6, 7, and 8, must be 3.3, 3.0, 2.5, or 1.8-V. Altera does not recommend using the level shifter between the Numonyx P30/P33 flash and the Cyclone III device in the AP configuration scheme.

There is no series resistors required in Cyclone III AP configuration mode when using the Numonyx Flash at 2.5-V/3.0-V/3.3-V I/O standard. According to Numonyx's P30 IBIS model, the output buffer will not overshoot above 4.1-V. Thus, series resistors are not required for 2.5-V/3.0-V/3.3-V active parallel configuration option. However, if there are any other devices sharing same flash I/Os with the Cyclone III device, all shared pins are still subject to the 4.1-V limit and may require series resistors.

The default read mode of the supported parallel flash memory is asynchronous, and all writes to the parallel flash memory are asynchronous. Both the parallel flash families support a synchronous read mode, with data supplied on the positive edge of DCLK.

- nRESET is an active-low hard reset
- FLASH_nCE is an active-low chip enable
- nOE is an active-low output enable for the DATA[15..0] bus and WAIT pin
- nAVD is an active-low address valid signal and is used to write addresses into the flash
- nWE is an active-low write enable and is used to write data into the flash
- PADD[23..0] bus is the address bus supplied to the flash
- DATA[15..0] bus is a bidirectional bus used to supply and read data to and from the flash, with the flash output controlled by nOE

Upon power-up, Cyclone III devices go through a POR. The POR delay depends, on the MSEL pin settings which correspond to the configuration scheme that you select. Depending on the configuration scheme, either a fast POR time or a standard POR time is available. The fast POR time is 3 ms < $T_{POR}$ < 9 ms for fast configuration time. The standard POR time is 50 ms < $T_{POR}$ < 200 ms, which has a lower power-ramp rate. During POR, the device resets, holds nSTATUS and CONF_DONE low, and tri-states all user I/O pins. Once the device successfully exits POR, all user I/O pins continue to be tri-stated. The user I/O pins and dual-purpose I/O pins have weak pull-up resistors, which are always enabled (after POR) before and during configuration.

You can find the value of the weak pull-up resistors on the I/O pins that are on before and during configuration in the *DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*.

The three stages of the configuration cycle are reset, configuration, and initialization. When nCONFIG or nSTATUS is low, the device is in reset. After POR, Cyclone III devices release nSTATUS, which is pulled high by an external 10-kΩ pull-up resistor and enters configuration mode.

To begin configuration, power the $V_{CCINT}$, $V_{CCA}$, and $V_{CCIO}$ voltages (for the banks in which the configuration and JTAG pins reside) to the appropriate voltage levels.

The serial clock (DCLK) generated by the Cyclone III device controls the entire configuration cycle and provides timing for the parallel interface. Cyclone III devices use a 40-Mhz internal oscillator to generate DCLK. The oscillator is the same oscillator used in the AS configuration scheme. The active DCLK output frequency is shown in Table 10–7.

After all configuration bits are received by the Cyclone III device, it releases the open-drain CONF_DONE pin, which is pulled high by an external 10-kΩ resistor. Initialization begins only after the CONF_DONE signal reaches a logic-high level. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize.

In Cyclone III devices, the initialization clock source is either the 10-MHz (typical) internal oscillator (separate from the active serial internal oscillator) or the optional CLKUSR pin. By default, the internal oscillator is the clock source for initialization. If you use the internal oscillator, the Cyclone III device provides itself with enough clock cycles for proper initialization. You do not need to send additional clock cycles from an external source to the CLKUSR pin during the initialization stage. You can also use the CLKUSR pin as a user I/O pin.

You also have the flexibility to synchronize initialization of multiple devices or to delay initialization with the CLKUSR option. Using the CLKUSR pin allows you to control when your device enters user mode. You can delay the device from entering user mode for an indefinite period of time. You can turn on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. When you click **Enable user-supplied start-up clock (CLKUSR)**, the CLKUSR pin is the initialization clock source. Supplying a clock on CLKUSR does not affect the configuration process. After all the configuration data has been accepted and CONF_DONE goes high, Cyclone III devices require 3,185 clock cycles to initialize properly and enter user mode. Cyclone III devices support a CLKUSR $f_{MAX}$ of 133 MHz.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user mode with a low-to-high transition. The **Enable INIT_DONE Output** option is available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. If you use the INIT_DONE pin, it will be high due to an external 10-kΩ pull-up resistor when nCONFIG is low and during the beginning of configuration. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and is pulled high. This low-to-high transition signals that the device has entered user mode. When initialization is complete, the device enters user mode. In user mode, the user I/O pins no longer have weak pull-up resistors and function as assigned in your design.

If an error occurs during configuration, Cyclone III devices assert the nSTATUS signal low, indicating a data frame error and the CONF_DONE signal stays low. If you turn on the **Auto-restart configuration after error** option (available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box), the Cyclone III device resets the configuration device by pulsing FLASH_nCE, releases nSTATUS after a reset time-out period (maximum of 230 ms), and retries configuration. If this option is turned off, the system must monitors nSTATUS for errors and then pulses nCONFIG low for at least 500 ns to restart configuration.

When the Cyclone III device is in user mode, you can initiate reconfiguration by pulling the nCONFIG pin low. The nCONFIG pin needs to be low for at least 500 ns. When nCONFIG is pulled low, the Cyclone III device is reset. The Cyclone III device also pulls nSTATUS and CONF_DONE low and all I/O pins are tri-stated. When nCONFIG returns to a logic-high level and nSTATUS is released by the Cyclone III device, reconfiguration begins.

If you use the optional CLKUSR pin and the nCONFIG pin is pulled low to restart configuration during device initialization, ensure CLKUSR continues to toggle during the time nSTATUS is low (a maximum of 230 ms).

For more information about configuration issues, refer to the *Debugging Configuration Problems* chapter in volume 2 of the *Configuration Handbook* and the FPGA Configuration Troubleshooter on the Altera website (www.altera.com).

## Multi-Device AP Configuration

You can configure multiple Cyclone III devices using a single parallel flash. You can cascade multiple Cyclone III devices using the chip-enable (nCE) and chip-enable-out (nCEO) pins. The first device in the chain must have its nCE pin connected to GND. You must connect its nCEO pin to the nCE pin of the next device in the chain. Use an external 10-kΩ pull-up resistor to pull the nCEO signal high to its $V_{CCIO}$ level to help the internal weak pull-up resistor. When the first device captures all of its configuration data from the bitstream, it drives the nCEO pin low, enabling the next device in the chain. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration if the last device in the chain is a Cyclone III device. The nCONFIG, nSTATUS, CONF_DONE, DCLK, DATA[15..8], and DATA[7..0] pins of each device in the chain are connected (refer to Figure 10–9 and Figure 10–10).

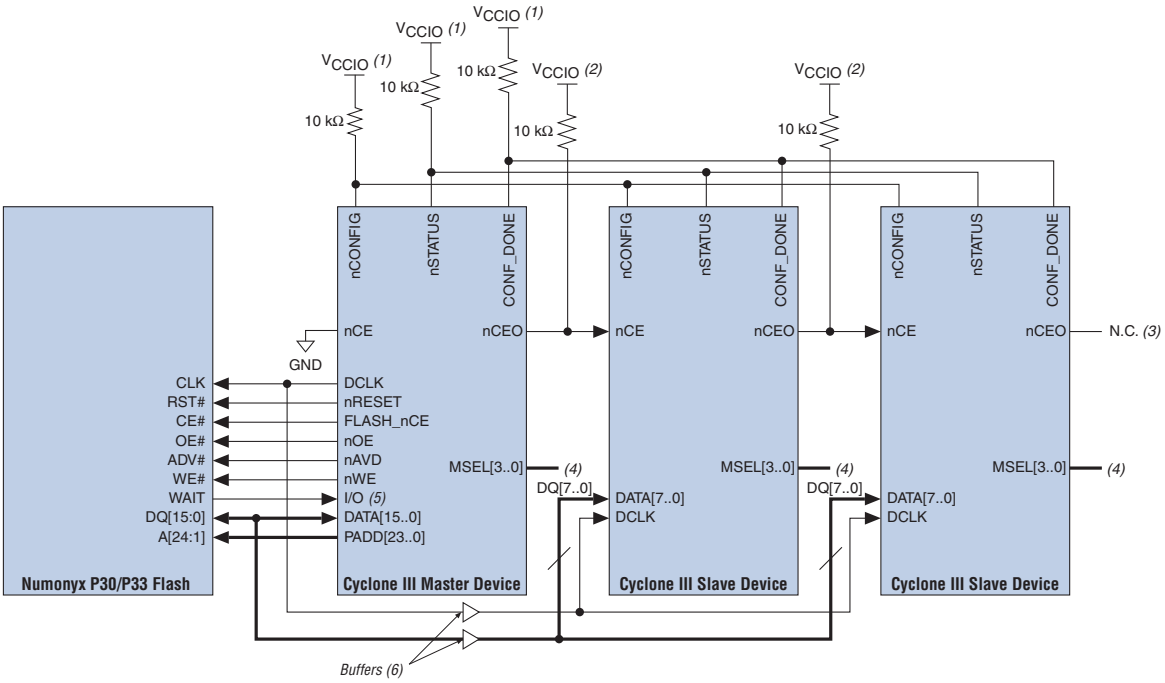
This first Cyclone III device in the chain, as shown in Figure 10–9 and Figure 10–10, is the configuration master and controls the configuration of the entire chain. You must connect its MSEL pins to select the AP configuration scheme. The remaining Cyclone III devices are configuration slaves period. You must connect their MSEL pins to select the FPP configuration scheme. Any other Altera device that supports FPP configuration can also be part of the chain as a configuration slave.

The two configurations for the DATA[15..0] bus in a multi-device AP configuration the byte-wide multi-device AP configuration and word-wide multi-device AP configuration.

### Byte-Wide Multi-Device AP Configuration

The first method is the byte-wide multi-device AP configuration and is the simpler form. In the byte-wide multi-device AP configuration, the least significant byte DATA[7..0] from the flash and master device (set to the AP configuration scheme) is connected to each of the slave devices set to FPP configuration scheme, as shown in Figure 10–9.

**Figure 10–9.** Byte-Wide Multi-Device AP Configuration




**Notes to Figure 10–9:**

(1) Connect the pull-up resistors to the $V_{CCIO}$ supply of the bank in which the pin resides.

(2) Connect the pull-up resistor to the $V_{CCIO}$ supply voltage of the I/O bank in which the nCE pin resides.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. You must set the Cyclone III master device in AP mode and the slave devices in FPP mode. To connect MSEL[3..0] for the master device in AP mode, refer to Table 10–9. To connect MSEL[3..0] for the slave devices in FPP mode, refer to Table 10–14. Connect the MSEL pins directly to $V_{CCA}$ or GND.

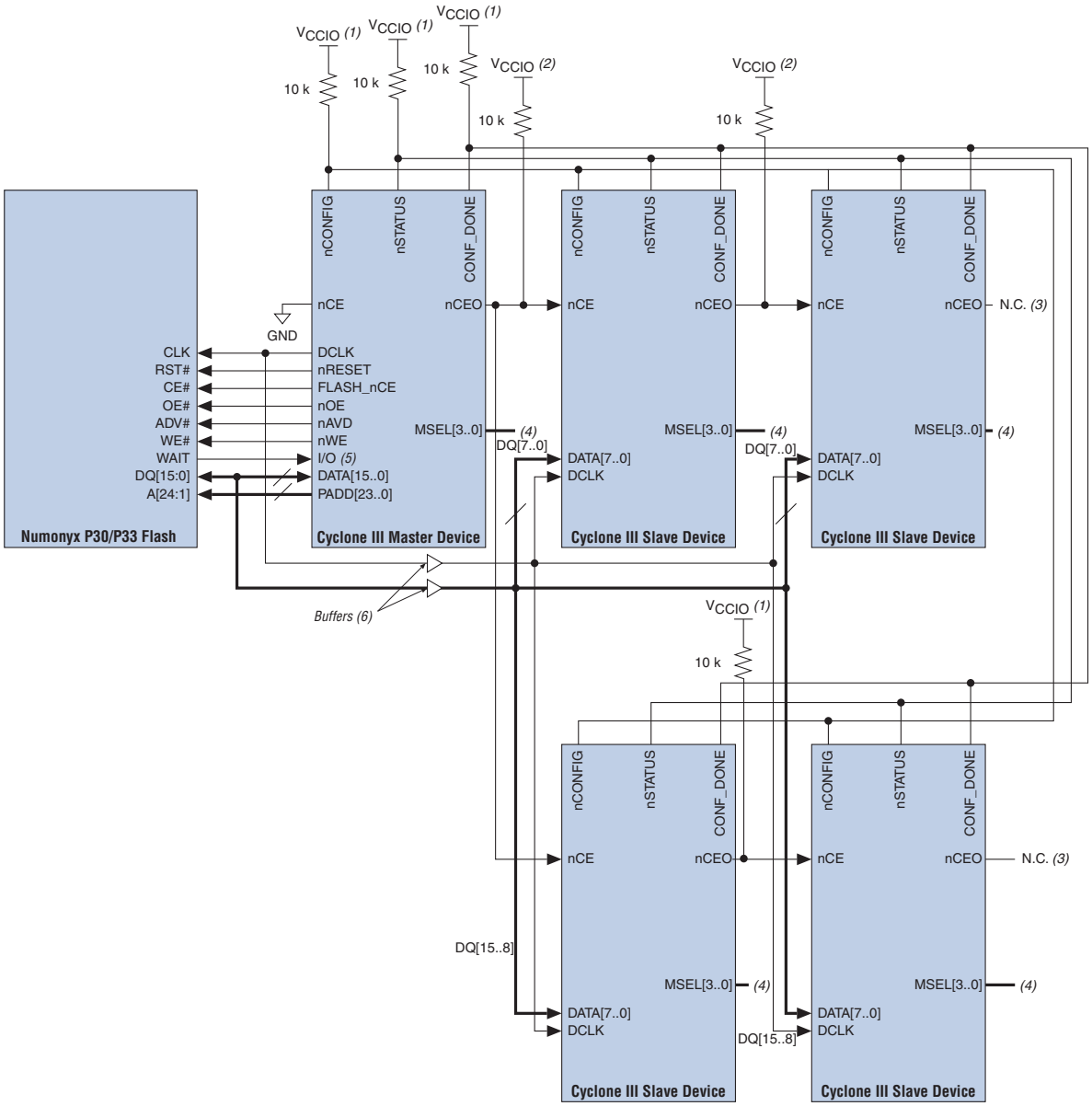
(5) The AP configuration ignores the WAIT signal during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O to monitor the WAIT signal from the Numonyx P30 or P33 flash.

(6) Connect the repeater buffers between the Cyclone III master and slave device or devices for DATA[15..0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

## Word-Wide Multi-Device AP Configuration

The more efficient setup is one in which some of the slave devices are connected to the least significant byte DATA[7..0] and the remaining slave devices are connected to the most significant byte DATA[15..8]. In the word-wide multi-device AP configuration, the nCEO pin of the master device enables two separate daisy-chains of slave devices, allowing both chains to be programmed concurrently, as shown in Figure 10–10.

**Figure 10–10.** Word-Wide Multi-Device AP Configuration




**Notes to Figure 10–10:**

(1) Connect the pull-up resistors to the $V_{CCIO}$ supply of the bank in which the pin resides.

(2) Connect the pull-up resistor to the $V_{CCIO}$ supply voltage of the I/O bank in which the nCE pin resides.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. You must set the Cyclone III master device in AP mode and the slave devices in FPP mode. To connect MSEL[3..0] for the master device in AP mode, refer to Table 10–9. To connect MSEL[3..0] for the slave devices in FPP mode, refer to Table 10–14. Connect the MSEL pins directly to $V_{CCA}$ or GND.

(5) The AP configuration ignores the WAIT signal during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O pin to monitor the WAIT signal from the Numonyx P30 or P33 flash.

(6) Connect the repeater buffers between the Cyclone III master and slave device or devices for DATA[15..0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

In a multi-device AP configuration, the board trace length between the parallel flash and the master Cyclone III device must follow the recommendations in Table 10–11. Additionally, you must connect the repeater buffers between the Cyclone III master and slave device or devices for DATA[15..0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

As shown in Figure 10–9 and Figure 10–10, the nSTATUS and CONF_DONE pins on all target devices are connected together with external pull-up resistors. These pins are open-drain bidirectional pins on the devices. When the first device asserts nCEO (after receiving all of its configuration data), it releases its CONF_DONE pin. However, the subsequent devices in the chain keep this shared CONF_DONE line low until they have received their configuration data. When all target devices in the chain have received their configuration data and have released CONF_DONE, the pull-up resistor drives a high level on this line and all devices simultaneously enter initialization mode.

If an error occurs at any point during configuration, the nSTATUS line is driven low by the failing device. If you enable the **Auto-restart configuration after error** option, reconfiguration of the entire chain begins after a reset time-out period (a maximum of 230 ms). If you turn off the **Auto-restart configuration after error** option, the external system must monitor nSTATUS for errors and then pulse nCONFIG low to restart the configuration. The external system can pulse nCONFIG if it is under system control rather than tied to $V_{CCIO}$.

## Guidelines for Connecting Parallel Flash to Cyclone III for AP Interface

For single- and multi-device AP configuration, the board trace length and loading between the supported parallel flash and the Cyclone III device must follow the recommendations shown in Table 10–11. These recommendations also apply to an AP configuration with multiple bus masters.

**Table 10–11.** Maximum Trace Length and Loading for AP Configuration

| Cyclone III AP Pins | Maximum Board Trace Length from Cyclone III Device to Flash Device (inches) | Maximum Board Load (pF) |
|---|---|---|
| DCLK | 6 | 15 |
| DATA[15..0] | 6 | 30 |
| PADD[23..0] | 6 | 30 |
| nRESET | 6 | 30 |
| Flash_nCE | 6 | 30 |
| nOE | 6 | 30 |
| nAVD | 6 | 30 |
| nWE | 6 | 30 |
| I/O *(1)* | 6 | 30 |

**Note to Table 10–11:**

(1) The AP configuration ignores the WAIT signal from the flash during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O to monitor the WAIT signal from the Numonyx P30 or P33 flash.

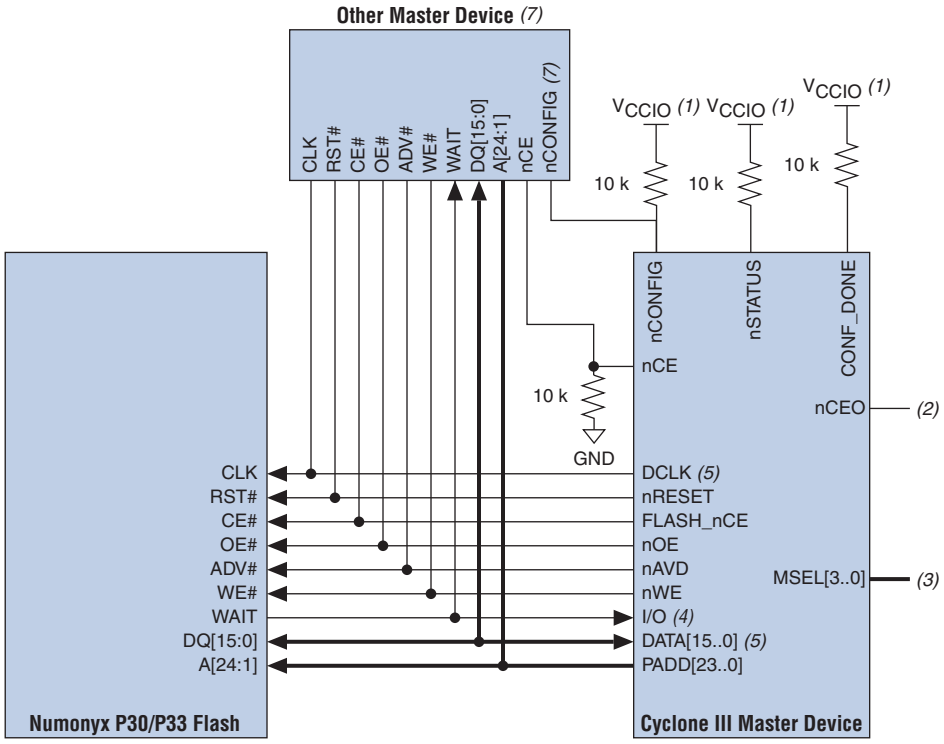
## Configuring With Multiple Bus Masters

Similar to the AS configuration scheme, the AP configuration scheme supports multiple bus masters for the parallel flash. For another master to take control of the AP configuration bus, it must assert nCONFIG low for at least 500 ns to reset the master Cyclone III device and override the weak 10 kΩ pull-down resistor on the nCE pin. This resets the master Cyclone III device and causes it to tri-state its AP configuration bus. The other master then takes control of the AP configuration bus. Once the other master is done, it must release the AP configuration bus, then release the nCE pin, and finally pulse nCONFIG low to restart the configuration.

In the AP configuration scheme, multiple masters can share the parallel flash. Similar to the AS configuration scheme, the bus control is negotiated by the nCE pin.

The AP configuration with multiple bus masters is shown in Figure 10–11.

**Figure 10–11.** AP Configuration with Multiple Bus Masters




**Notes to Figure 10–11:**

(1) Connect the pull-up resistors to the $V_{CCIO}$ supply of the bank in which the pin resides.

(2) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.

(3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 10–9. Connect the MSEL pins directly to $V_{CCA}$ or GND.

(4) The AP configuration ignores the WAIT signal during configuration mode. However, if you are accessing flash during user mode with user logic, you can optionally use the normal I/O to monitor the WAIT signal from the Numonyx P30 or P33 flash.

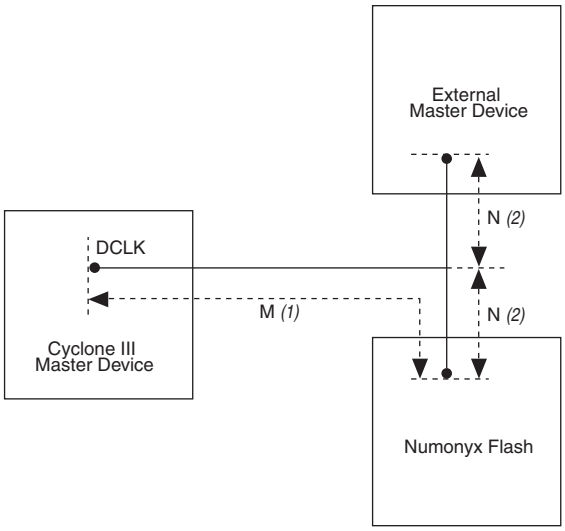
(5) When cascading Cyclone III devices in a multi-device AP configuration, connect the repeater buffers between the Cyclone III master and slave device or devices for DATA[15..0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

(6) The other master device must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

(7) The other master device can pulse nCONFIG if it is under system control rather than tied to $V_{CCIO}$.

For multiple bus master interfaces, refer to Figure 10–12 for the recommended routing to minimize signal integrity issue.

**Figure 10–12.** Balanced Star Routing




**Notes to Figure 10–12:**

(1) Altera does not recommend *M* to exceed 6 inches as per Table 10–11.

(2) Altera recommends using a balanced star routing. Try to keep the *N* length equal and as short as possible to minimize reflection noise from the transmission line. The *M* length is applicable to this setup.

## Estimating AP Configuration Time

Active parallel configuration time is dominated by the time it takes to transfer data from the parallel flash to the Cyclone III device. This parallel interface is clocked by the Cyclone III DCLK output (generated from an internal oscillator). As listed in Table 10–7, the DCLK minimum frequency when using the 40-MHz oscillator is 20 MHz (50 ns). In word-wide cascade programming, the DATA[15..0] bus transfers a 16-bit word and essentially cuts configuration time to approximately 1/16 that of the AS configuration time. Therefore, the maximum configuration time estimation for an EP3C40 device (9,600,000 bits of uncompressed data) is:

**Equation 10–4.**

$$\text{RBF Size} \times \left(\frac{\text{maximum DCLK period}}{\text{16 bits per DCLK cycle}}\right) = \text{estimated maximum configuration time}$$

**Equation 10–5.**

$$9{,}600{,}000 \text{ bits} \times \left(\frac{50 \text{ ns}}{16 \text{ bits}}\right) = 30 \text{ ms}$$

To estimate the typical configuration time, use the typical DCLK period listed in Table 10–7. With a typical DCLK period of 33.33 ns, the typical configuration time is 20 ms.

## Programming Parallel Flash Memories

Supported parallel flash memories are external non-volatile configuration devices. They are industry standard microprocessor flash memories (for more information about the supported families for the commodity parallel flash, refer to Table 10–10).

Cyclone III devices in a single device chain or in a multiple device chain support in-system programming of a parallel flash using the JTAG interface via the flash loader megafunction. The board's intelligent host or download cable can use the four JTAG pins on the Cyclone III device to program the parallel flash in system, even if the host or download cable cannot access the parallel flash's configuration pins.

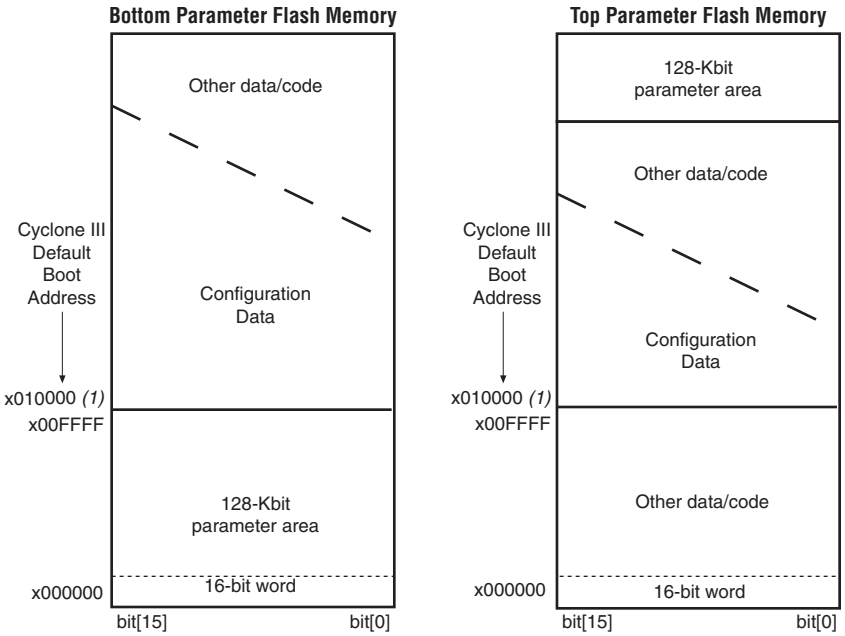
For more information about using the JTAG pins on the Cyclone III device to program the parallel flash in-system, refer to *AN 478: Using FPGA-Based Parallel Flash Loader (PFL) with the Quartus II Software*.

In the AP configuration scheme, the default configuration boot address is 0×010000 when represented in 16-bit word addressing in the supported parallel flash memory (refer to Figure 10–13). In the Quartus II software, the default configuration boot address is 0x020000 because it is represented in 8-bit byte addressing. Cyclone III devices configure from word address 0x010000, which is equivalent to byte address 0x020000.

The Quartus II software uses byte addressing for the default configuration boot address. You must set the **Start address** field to 0x020000.

The default configuration boot address allows the system to use special parameter blocks within the flash memory map. Parameter blocks can be at the top or bottom of the memory map. The configuration boot address in the AP configuration scheme is shown in Figure 10–13. You can change the default configuration default boot address 0x010000 to any desired address using the JTAG instruction `APFC_BOOT_ADDR` (for more information about the JTAG instruction `APFC_BOOT_ADDR`, refer to "Cyclone III JTAG Instructions").

**Figure 10–13.** Configuration Boot Address in AP Flash Memory Map




**Note to Figure 10–13:**

(1) The default configuration boot address is x010000 when represented in 16-bit word addressing.

# Passive Serial Configuration

You can perform PS configuration on Cyclone III devices with an external intelligent host, such as a MAX II device, microprocessor with flash memory, or a download cable. In the PS scheme, an external host controls configuration. Configuration data is clocked into the target Cyclone III device via the DATA[0] pin at each rising edge of DCLK.

The Cyclone III decompression feature is available when configuring your Cyclone III device with the PS configuration scheme.

Table 10–12 shows the MSEL pin settings when using the PS configuration scheme with different configuration voltage standards.

**Table 10–12.** Cyclone III MSEL Pin Settings for PS Configuration Schemes *(Note 5)*

| Configuration Scheme | MSEL3 *(4)* | MSEL2 | MSEL1 | MSEL0 | Configuration Voltage Standard *(2)* |
|---|---|---|---|---|---|
| Passive Serial Standard (PS Standard POR) *(1)* | 0 | 0 | 0 | 0 | 3.3/3.0/2.5 V *(3)* |

**Table 10–12.** Cyclone III MSEL Pin Settings for PS Configuration Schemes *(Note 5)*

| Configuration Scheme | MSEL3 *(4)* | MSEL2 | MSEL1 | MSEL0 | Configuration Voltage Standard *(2)* |
|---|---|---|---|---|---|
| Passive Serial Fast (PS Fast POR) *(1)* | 1 | 1 | 0 | 0 | 3.3/3.0/2.5 V *(3)* |

**Notes to Table 10–12:**

(1) These schemes support data decompression.

(2) The configuration voltage standard is applied to the $V_{CCIO}$ supply of the bank in which the configuration pins reside.

(3) You must follow specific requirements when interfacing Cyclone III devices with 2.5-, 3.0-, and 3.3- V configuration voltage standards (for more information about the requirements, refer to "Configuration and JTAG Pin I/O Requirements").

(4) Some of the smaller Cyclone III devices or package options do not support the AP configuration scheme and do not have the `MSEL[3]` pin. For information about the supported configuration schemes across device densities and package options, refer to Table 10–2.

(5) You should connect the MSEL pins to $V_{CCA}$ or GND depending on the MSEL pin settings.

If your system already contains a common flash interface (CFI) flash memory, you can use it for the Cyclone III device configuration storage as well. The MAX II PFL feature provides an efficient method to program CFI flash memory devices through the JTAG interface and the logic to control configuration from the flash memory device to the Cyclone III device. Both PS and FPP configuration schemes are supported using this PFL feature.

For more information about PFL, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software*.

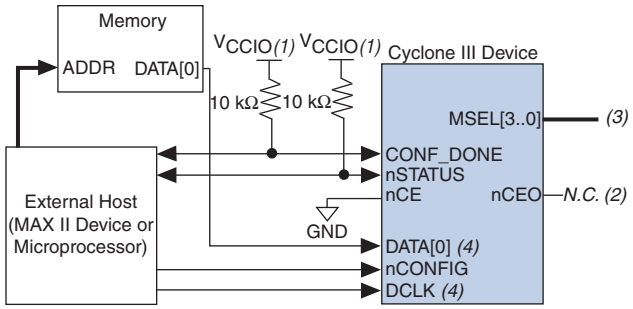
Cyclone III devices do not support enhanced configuration devices for PS or FPP configuration.

## PS Configuration Using a MAX II Device as an External Host

In the PS configuration scheme, you can use a MAX II device as an intelligent host that controls the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone III device. You can store configuration data in either a **.rbf**, **.hex**, or **.ttf** file format.

Figure 10–14 shows the configuration interface connections between a Cyclone III device and a MAX II device for single-device configuration.

**Figure 10–14.** Single-Device PS Configuration Using an External Host




**Notes to Figure 10–14:**

(1) Connect the pull-up resistor to a supply that provides an acceptable input signal for the device. $V_{CC}$ should be high enough to meet the $V_{IH}$ specification of the I/O on the device and the external host.

(2) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

(3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 10–12. Connect the MSEL pins directly to $V_{CCA}$ or ground.

(4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. DATA[0] and DCLK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

All I/O inputs must maintain a maximum AC voltage of 4.1 V. In a single-device PS configuration, DATA[0] and DCLK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

Upon power-up, Cyclone III devices go through a POR. The POR delay is dependent on the MSEL pin settings which correspond to the configuration scheme that you select. Depending on the configuration scheme, either a fast POR time or a standard POR time is available. The fast POR time is 3 ms < $T_{POR}$ < 9 ms for fast configuration time. The standard POR time is 50 ms < $T_{POR}$ < 200 ms, which has a lower power-ramp rate. During POR, the device resets, holds nSTATUS low, and tri-states all user I/O pins. Once the device successfully exits POR, all user I/O pins continue to be tri-stated. The user I/O pins and dual-purpose I/O pins have weak pull-up resistors which are always enabled (after POR) before and during configuration.

For information about the value of the weak pull-up resistors on the I/O pins that are on before and during configuration, refer to the *DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*.

The three stages of the configuration cycle are reset, configuration, and initialization. When nCONFIG or nSTATUS is low, the device is in reset. To initiate configuration, the MAX II device must generate a low-to-high transition on the nCONFIG pin.

To begin configuration, power the $V_{CCINT}$, $V_{CCA}$, and $V_{CCIO}$ voltages (for the banks in which the configuration and JTAG pins reside) to the appropriate voltage levels.

When nCONFIG goes high, the device comes out of reset and releases the open-drain nSTATUS pin, which is then pulled high by an external 10-kΩ pull-up resistor. Once nSTATUS is released, the device is ready to receive configuration data and the configuration stage begins. When nSTATUS is pulled high, the MAX II device needs to place the configuration data one bit at a time on the DATA[0] pin. If you are using configuration data in either a **.rbf**, **.ttf**, or **.hex** file, you must send the least significant bit of each data byte first. For example, if the **.rbf** file contains the byte sequence 02 1B EE 01 FA, the serial bitstream you needs to transmit to the device is:

```
0100-0000 1101-1000 0111-0111 1000-0000 0101-1111
```

Cyclone III devices receive configuration data on the DATA[0] pin; the clock is received on the DCLK pin. Data is latched into the device on the rising edge of DCLK. Data is continuously clocked into the target device until CONF_DONE goes high. After the device has received all the configuration data successfully, it releases the open-drain CONF_DONE pin, which is pulled high by an external 10-kΩ pull-up resistor. A low-to-high transition on CONF_DONE indicates configuration is complete and initialization of the device can begin. The CONF_DONE pin must have an external 10-kΩ pull-up resistor for the device to initialize.

Two DCLK falling edges are required after CONF_DONE goes high to begin the initialization of the device.

In Cyclone III devices, the initialization clock source is either the internal oscillator (typically 10 MHz) or the optional CLKUSR pin. By default, the internal oscillator is the clock source for initialization. If you use the internal oscillator, the Cyclone III device provides itself with enough clock cycles for proper initialization. Therefore, if the internal oscillator is the initialization clock source, sending the entire configuration file to the device is sufficient to configure and initialize the device. Driving DCLK to the device after configuration is complete does not affect device operation. Additionally, if you use the internal oscillator as the clock source, you can use the CLKUSR pin as a user I/O pin.

You also have the flexibility to synchronize initialization of multiple devices or to delay initialization with the CLKUSR option. You can turn on the **Enable user-supplied start-up clock** (**CLKUSR**) option in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. Supplying a clock on CLKUSR does not affect the configuration process. After all the configuration data is accepted and CONF_DONE goes high, CLKUSR is enabled after the time specified as $t_{CD2CU}$. After this time period elapses, Cyclone III devices require 3,187 clock cycles to initialize properly and enter user mode. Cyclone III devices support a CLKUSR $f_{MAX}$ of 133 MHz.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user-mode with a low-to-high transition. The **Enable INIT_DONE Output** option is available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. If you use the INIT_DONE pin, it will be high due to an external 10-kΩ pull-up resistor when nCONFIG is low and during the beginning of configuration. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and pulled high. The MAX II device must be able to detect this low-to-high transition, which signals the device has entered user mode. When initialization is complete, the device enters user mode. In user mode, the user I/O pins no longer have weak pull-up resistors and function as assigned in your design.

To ensure DCLK and DATA[0] are not left floating at the end of configuration, the MAX II device must drive them either high or low, whichever is convenient on your board. The DATA[0] pin is available as a user I/O pin after configuration. When you choose the PS scheme in the Quartus II software, the DATA[0] pin is tri-stated, by default, in user mode and needs to be driven by the MAX II device. To change this default option in the Quartus II software, select the **Dual-Purpose Pins** tab of the **Device and Pin Options** dialog box.

The configuration clock (DCLK) speed must be below the specified system frequency to ensure correct configuration (refer to Table 10–13). No maximum DCLK period exists, which means you can pause configuration by halting DCLK for an indefinite amount of time.

If an error occurs during configuration, the device drives its nSTATUS pin low, resetting itself internally. The low signal on the nSTATUS pin also alerts the MAX II device that there is an error. If you turn on the **Auto-restart configuration after error** option (available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box), the Cyclone III device releases nSTATUS after a reset time-out period (maximum of 230 µs). After nSTATUS is released and pulled high by a pull-up resistor, the MAX II device can try to reconfigure the target device without needing to pulse nCONFIG low. If you turn off this option, the MAX II device must generate a low-to-high transition (with a low pulse of at least 500 ns) on nCONFIG to restart the configuration process.

The MAX II device can also monitor the CONF_DONE and INIT_DONE pins to ensure successful configuration. The CONF_DONE pin must be monitored by the MAX II device to detect errors and determine when programming completes. If all configuration data is sent, but CONF_DONE or INIT_DONE has not gone high, the MAX II device must reconfigure the target device.

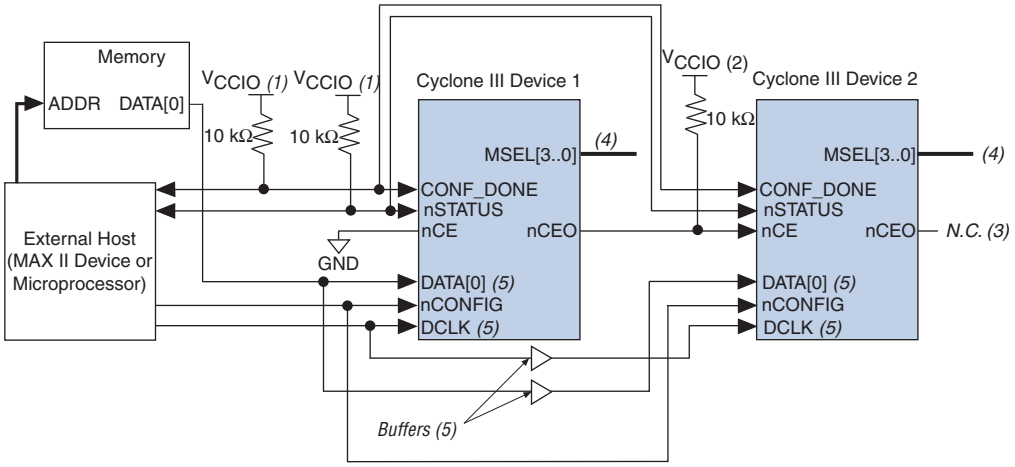
If you are using the optional CLKUSR pin and nCONFIG is pulled low to restart configuration during device initialization, ensure that CLKUSR continues toggling during the time nSTATUS is low (a maximum of 230 µs).

When the device is in user mode, you can initiate a reconfiguration by transitioning the nCONFIG pin low-to-high. The nCONFIG pin must be low for at least 500 ns. When nCONFIG is pulled low, the device also pulls nSTATUS and CONF_DONE low and tri-states all I/O pins. Once nCONFIG returns to a logic-high level and nSTATUS is released by the device, reconfiguration begins.

For more information about configuration issues, refer to *Debugging Configuration Problems* chapter in volume 2 of the *Configuration Handbook* and the FPGA Configuration Troubleshooter on the Altera website (www.altera.com).

Figure 10–15 shows how to configure multiple devices using a MAX II device. This circuit is similar to the PS configuration circuit for a single device, except Cyclone III devices are cascaded for multi-device configuration.

**Figure 10–15.** Multi-Device PS Configuration Using an External Host




**Notes to Figure 10–15:**

(1) The pull-up resistor needs to be connected to a supply that provides an acceptable input signal for all devices in the chain. $V_{CC}$ needs to be high enough to meet the $V_{IH}$ specification of the I/O on the device and the external host.

(2) Connect the pull-up resistor to the $V_{CCIO}$ supply voltage of the I/O bank in which the nCE pin resides.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 10–12. Connect the MSEL pins directly to $V_{CCA}$ or ground.

(5) All I/O inputs must maintain a maximum AC voltage of 4.1 V. DATA[0] and DCLK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

All I/O inputs must maintain a maximum AC voltage of 4.1 V. In a multi-device PS configuration, DATA[0] and DCLK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements". You must connect the repeater buffers between the Cyclone III master and slave device or devices for DATA[0] and DCLK.

In a multi-device PS configuration, the first device's nCE pin is connected to GND while its nCEO pin is connected to nCE of the next device in the chain. The last device's nCE input comes from the previous device, while its nCEO pin is left floating. After the first device completes configuration in a multi-device configuration chain, its nCEO pin drives low to activate the second device's nCE pin, which prompts the second device to begin configuration. The second device in the chain begins configuration within one clock cycle. Therefore, the transfer of data destinations is transparent to the MAX II device. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA[0], and CONF_DONE) are connected to every device in the chain. Configuration signals can require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered. Because all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

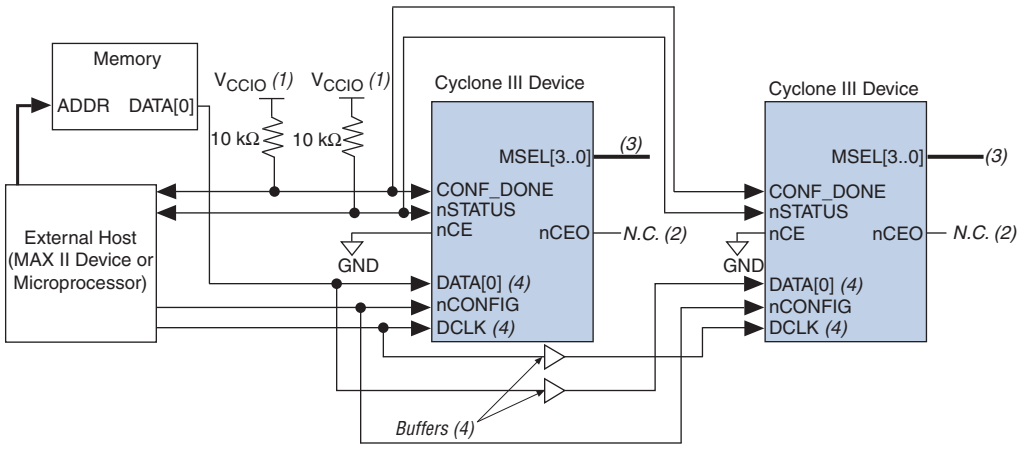
If any device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured because all nSTATUS and CONF_DONE pins are tied together. For example, if the first device flags an error on nSTATUS, it resets the chain by pulling its nSTATUS pin low. This behavior is similar to a single device detecting an error.

If the **Auto-restart configuration after error** option is turned on, the devices release their nSTATUS pins after a reset time-out period (a maximum of 230 µs). After all nSTATUS pins are released and pulled high, the MAX II device can try to reconfigure the chain without needing to pulse nCONFIG low. If this option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 500 ns) on nCONFIG to restart the configuration process.

In your system, you can have multiple devices that contain the same configuration data. To support this configuration scheme, all device nCE inputs are tied to GND, while nCEO pins are left floating. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA[0], and CONF_DONE) are connected to every device in the chain. Configuration signals can require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered. Devices must be the same density and package. All devices will start and complete configuration at the same time.

Figure 10–16 shows a multi-device PS configuration when both Cyclone III devices are receiving the same configuration data.

**Figure 10–16.** Multi-Device PS Configuration When Both Devices Receive the Same Data




**Notes to Figure 10–16:**

(1) The pull-up resistor needs to be connected to a supply that provides an acceptable input signal for all devices in the chain. $V_{CC}$ needs to be high enough to meet the $V_{IH}$ specification of the I/O on the device and the external host.

(2) The nCEO pins of both devices can be left unconnected or used as user I/O pins when configuring the same configuration data into multiple devices.

(3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 10–12. Connect the MSEL pins directly to $V_{CCA}$ or ground.

(4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. DATA[0] and DCLK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

You can use a single configuration chain to configure Cyclone III devices with other Altera devices. To ensure that all devices in the chain complete configuration at the same time or that an error flagged by one device initiates reconfiguration in all devices, all of the device CONF_DONE and nSTATUS pins must be tied together.

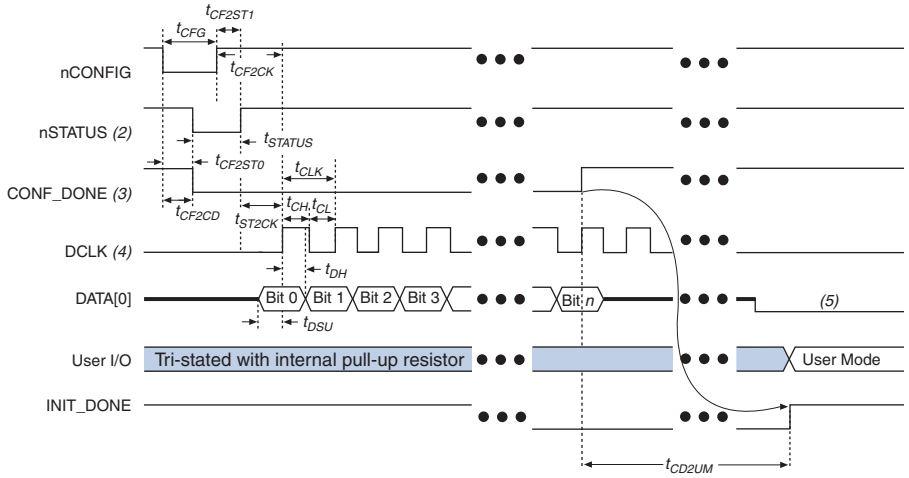
For more information about configuring multiple Altera devices in the same configuration chain, refer to *Configuring Mixed Altera FPGA Chains* in volume 2 of the *Configuration Handbook*.

## PS Configuration Timing

A PS configuration must meet the setup and hold timing parameters and the maximum clock frequency. When using a microprocessor or another intelligent host to control the PS interface, ensure that you meet these timing requirements.

Figure 10–17 shows the timing waveform for a PS configuration when using a MAX II device as an external host.

**Figure 10–17.** PS Configuration Timing Waveform *(Note 1)*




**Notes to Figure 10–17:**

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) Upon power-up, the Cyclone III device holds nSTATUS low for the time of the POR delay.

(3) Upon power-up, before and during configuration, CONF_DONE is low.

(4) In user mode, drive DCLK either high or low when using the PS configuration scheme, whichever is more convenient. When using the AS configuration scheme, DCLK is a Cyclone III output pin and should not be driven externally.

(5) Do not leave the DATA[0] pin floating after configuration. Drive it high or low, whichever is more convenient.

Table 10–13 defines the timing parameters for Cyclone III devices for a PS configuration.

**Table 10–13.** PS Timing Parameters for Cyclone III Devices *(Note 1)* (Part 1 of 2)

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 500 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 500 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 500 | — | ns |
| $t_{STATUS}$ | nSTATUS low pulse width | 45 | 230 *(2)* | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 230 *(2)* | µs |
| $t_{CF2CK}$ | nCONFIG high to first rising edge on DCLK | 230 *(2)* | — | µs |

**Table 10–13.** PS Timing Parameters for Cyclone III Devices *(Note 1)* (Part 2 of 2)

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{ST2CK}$ | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | Data setup time before rising edge on DCLK | 5 | — | ns |
| $t_{DH}$ | Data hold time after rising edge on DCLK | 0 | — | ns |
| $t_{CH}$ | DCLK high time | 3.2 | — | ns |
| $t_{CL}$ | DCLK low time | 3.2 | — | ns |
| $t_{CLK}$ | DCLK period | 7.5 | — | ns |
| $f_{MAX}$ | DCLK frequency | — | 133 | MHz |
| $t_{CD2UM}$ | CONF_DONE high to user mode *(3)* | 300 | 650 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (3,187 × CLKUSR period) | — | — |

**Notes to Table 10–13:**

(1) This information is preliminary.

(2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) The minimum and maximum numbers apply only if the internal oscillator is chosen as the clock source for starting the device.

For more information about device configuration options and how to create configuration files, refer to the *Software Settings* section in volume 2 of the *Configuration Handbook*.

## PS Configuration Using a Microprocessor

In the PS configuration scheme, a microprocessor can control the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone III device.

All information in "PS Configuration Using a MAX II Device as an External Host" is also applicable when using a microprocessor as an external host. For all configuration and timing information, refer to "PS Configuration Using a MAX II Device as an External Host".

The MicroBlaster™ software driver allows you to configure Altera FPGAs, including Cyclone III devices, through the ByteBlaster II or ByteBlasterMV cable in PS mode. The MicroBlaster software driver supports a **.rbf** programming input file and is targeted for embedded PS configuration. The source code is developed for the Windows NT operating system (OS). You can customize it to run on other operating systems.

For more information about the MicroBlaster software driver, refer to *AN 423: Configuring the MicroBlaster Passive Serial Software Driver* and source files on the Altera website.

If you enable the **CLKUSR** option in the Quartus II software, Cyclone III devices do not enter user mode after the MicroBlaster has transmitted all the configuration data in the **.rbf** file. You must supply enough initialization clock cycles to the CLKUSR pin to enter user mode.

## PS Configuration Using a Download Cable

In this section, the generic term "download cable" includes the Altera USB-Blaster USB port download cable, MasterBlaster™ serial/USB communications cable, ByteBlaster II parallel port download cable, and the ByteBlaster MV parallel port download cable.

In a PS configuration with a download cable, an intelligent host (such as a PC) transfers data from a storage device to the device via the USB-Blaster, MasterBlaster, ByteBlaster II, or ByteBlasterMV cable.

Upon power-up, Cyclone III devices go through a POR. The POR delay is dependent on the MSEL pin settings, which correspond to the configuration scheme that you select. Depending on the configuration scheme, either a fast POR time or a standard POR time is available. The fast POR time is 3 ms < $T_{POR}$ < 9 ms for fast configuration time. The standard POR time is 50 ms < $T_{POR}$ < 200 ms, which has a lower power-ramp rate. During POR, the device resets, holds nSTATUS low, and tri-states all user I/O pins. Once the device successfully exits POR, all user I/O pins continue to be tri-stated. The user I/O pins and dual-purpose I/O pins have weak pull-up resistors, which are always enabled (after POR) before and during configuration.

For information about the value of the weak pull-up resistors on the I/O pins that are on before and during configuration, refer to the *DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook.*

The three stages of the configuration cycle are reset, configuration, and initialization. When nCONFIG or nSTATUS is low, the device is in reset. To initiate configuration in this scheme, the download cable generates a low-to-high transition on the nCONFIG pin.

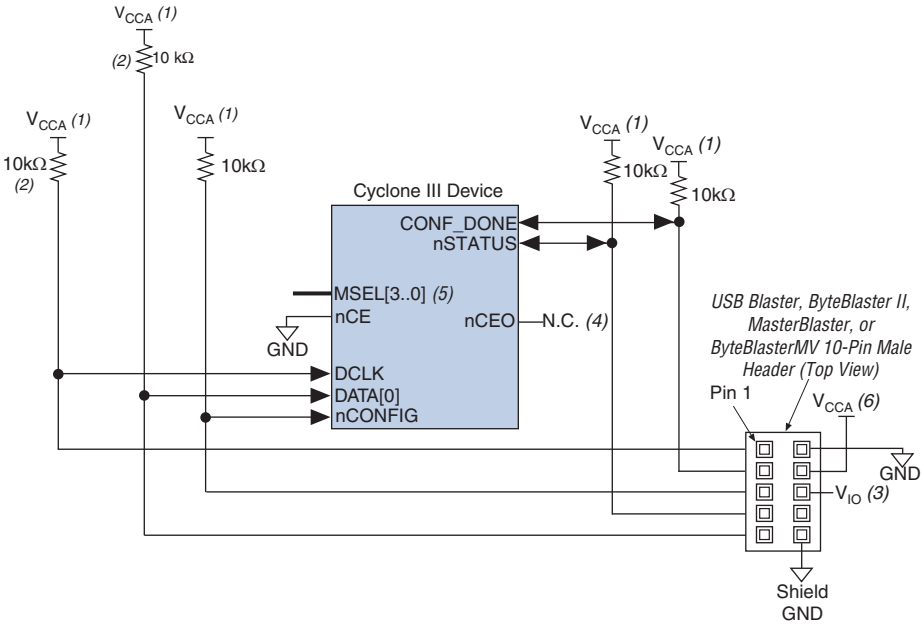
To begin configuration, power the $V_{CCINT}$, $V_{CCA}$, and $V_{CCIO}$ (for the banks in which the configuration and JTAG pins reside) voltages to the appropriate voltage levels.

When nCONFIG goes high, the device comes out of reset and releases the open-drain nSTATUS pin, which is then pulled high by an external 10-kΩ pull-up resistor. Once nSTATUS is released, the device is ready to receive configuration data and the configuration stage begins. The programming hardware or download cable then places the configuration data one bit at a time on the device's DATA[0] pin. The configuration data is clocked into the target device until CONF_DONE goes high. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize.

When you use a download cable, setting the **Auto-restart configuration after error** option does not affect the configuration cycle because you must manually restart configuration in the Quartus II software when an error occurs. Additionally, the **Enable user-supplied start-up clock** (**CLKUSR**) option has no effect on the device initialization because this option is disabled in the **.sof** file when programming the

device using the Quartus II programmer and download cable. Therefore, if you turn on the **CLKUSR** option, you do not need to provide a clock on CLKUSR when you are configuring the device with the Quartus II programmer and a download cable. Figure 10–18 shows a PS configuration for Cyclone III devices using a USB-Blaster, MasterBlaster, ByteBlaster II, or ByteBlasterMV cable.

**Figure 10–18.** PS Configuration Using a USB-Blaster, MasterBlaster, ByteBlaster II, or ByteBlasterMV Cable




**Notes to Figure 10–18:**

(1) The pull-up resistor needs to be connected to the same supply voltage as the $V_{CCA}$ supply.

(2) The pull-up resistors on DATA[0] and DCLK are only needed if the download cable is the only configuration scheme used on your board. This is to ensure that DATA[0] and DCLK are not left floating after configuration. For example, if you are also using a configuration device, the pull-up resistors on DATA[0] and DCLK are not needed.

(3) Pin 6 of the header is a $V_{IO}$ reference voltage for the MasterBlaster output driver. $V_{IO}$ needs to match the device's $V_{CCA}$. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. In ByteBlasterMV, this pin is a no connect. In USB-Blaster and ByteBlaster II, this pin is connected to nCE when it is used for AS programming. Otherwise it is a no connect.

(4) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

(5) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 10–12 for PS configuration schemes. Connect the MSEL pins directly to $V_{CCA}$ or GND.

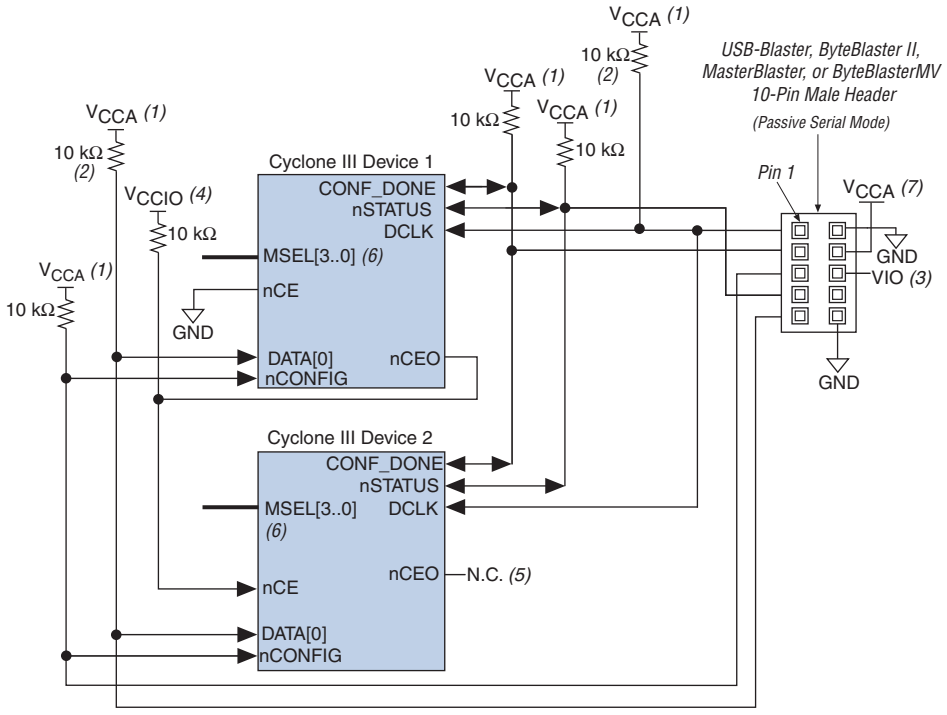
(6) Power up the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable's $V_{CC}$ with a 2.5- V supply from $V_{CCA}$. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a $V_{CC}$ power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.

You can use a download cable to configure multiple Cyclone III devices by connecting each device's nCEO pin to the subsequent device's nCE pin. The first device's nCE pin is connected to GND while its nCEO pin is connected to the nCE of the next device in the chain. The last device's nCE input comes from the previous device, while its nCEO pin is left floating. All other configuration pins, nCONFIG, nSTATUS, DCLK, DATA[0], and CONF_DONE are connected to every device in the chain. Because all CONF_DONE pins are tied together, all devices in the chain initialize and enter user mode at the same time.

In addition, the entire chain halts configuration if any device detects an error because the nSTATUS pins are tied together. The **Auto-restart configuration after error** option does not affect the configuration cycle because you must manually restart configuration in the Quartus II software when an error occurs.

Figure 10–19 shows how to configure multiple Cyclone III devices with a download cable.

**Figure 10–19.** Multi-Device PS Configuration Using a USB-Blaster, MasterBlaster, ByteBlaster II, or ByteBlasterMV Cable




**Notes to Figure 10–19:**

(1) The pull-up resistor needs to be connected to the same supply voltage as the $V_{CCA}$ supply.

(2) The pull-up resistors on DATA[0] and DCLK are only needed if the download cable is the only configuration scheme used on your board. This is to ensure that DATA[0] and DCLK are not left floating after configuration. For example, if you are also using a configuration device, the pull-up resistors on DATA[0] and DCLK are not needed.

(3) Pin 6 of the header is a VIO reference voltage for the MasterBlaster output driver. $V_{IO}$ needs to match the device's $V_{CCA}$. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. In ByteBlasterMV, this pin is a no connect. In USB-Blaster and ByteBlaster II, this pin is connected to nCE when it is used for AS programming. Otherwise, it is a no connect.

(4) Connect the pull-up resistor to the $V_{CCIO}$ supply voltage of the I/O bank in which the nCE pin resides.

(5) The nCEO pin of the last device in the chain can be left unconnected or used as a user I/O pin.

(6) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 10–12 for PS configuration schemes. Connect the MSEL pins directly to $V_{CCA}$ or GND.

(7) Power up the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable's $V_{CC}$ with a 2.5- V supply from $V_{CCA}$. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a $V_{CC}$ power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.

For more information about how to use the USB-Blaster, MasterBlaster, ByteBlaster II, or ByteBlasterMV cables, refer to the *ByteBlaster II Download Cable User Guide, ByteBlasterMV Download Cable User Guide, MasterBlaster Serial/USB Communications Cable User Guide,* and *USB-Blaster Download Cable User Guide.*

# Fast Passive Parallel Configuration

The FPP configuration in Cyclone III devices is designed to meet the increasing demand for faster configuration times. Cyclone III devices are designed with the capability of receiving byte-wide configuration data per clock cycle.

Table 10–14 shows the MSEL pin settings when using the FPP configuration scheme with different configuration voltage standards.

**Table 10–14.** Cyclone III MSEL Pin Settings for FPP Configuration Schemes *(Note 5)*

| Configuration Scheme | MSEL3 *(4)* | MSEL2 | MSEL1 | MSEL0 | Configuration Voltage Standard *(2)* |
|---|---|---|---|---|---|
| Fast Passive Parallel Fast (FPP Fast POR) *(1)* | 1 | 1 | 1 | 0 | 3.3/3.0/2.5 V *(3)* |
| Fast Passive Parallel Fast (FPP Fast POR) *(1)* | 1 | 1 | 1 | 1 | 1.8/1.5 V |

**Notes to Table 10–14:**

(1) Some of the smaller Cyclone III devices or package options do not support the FPP configuration scheme (for more information, refer to Table 10–2).

(2) The configuration voltage standard is applied to the $V_{CCIO}$ supply of the bank in which the configuration pins reside.

(3) You must follow specific requirements when interfacing Cyclone III devices with 2.5-, 3.0-, and 3.3-V configuration voltage standards (for more information about the requirements, refer to "Configuration and JTAG Pin I/O Requirements").

(4) Some of the smaller Cyclone III devices or package options do not support the AP configuration scheme and do not have the `MSEL[3]` pin (for more information about the supported configuration schemes across device densities and package options, refer to Table 10–2).

(5) You needs to connect the MSEL pins to $V_{CCA}$ or GND depending on the MSEL pin settings.

You can perform FPP configuration of Cyclone III devices with an intelligent host, such as a MAX II device or microprocessor with flash memory.

If your system already contains CFI flash memory, you can utilize it for the Cyclone III device configuration storage as well. The MAX II PFL feature in MAX II devices provides an efficient method to program CFI flash memory devices through the JTAG interface and the logic to control configuration from the flash memory device to the Cyclone III device. Both PS and FPP configuration schemes are supported using this PFL feature.

For more information about PFL, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software*.

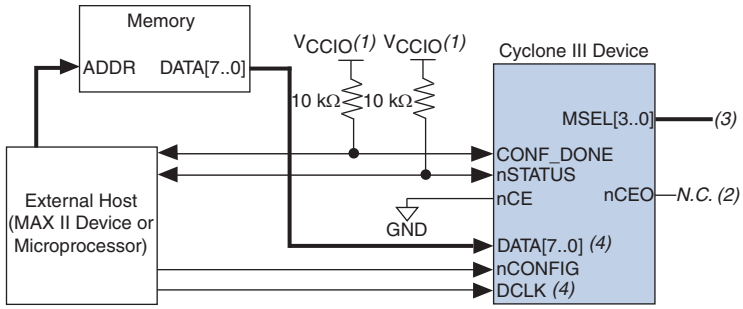
Cyclone III devices do not support enhanced configuration devices for PS or FPP configuration.

## FPP Configuration Using a MAX II Device as an External Host

The FPP configuration using an external host provides a fast method to configure Cyclone III devices. In the FPP configuration scheme, you can use a MAX II device as an intelligent host that controls the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone III device. You can store configuration data in a **.rbf**, **.hex**, or **.ttf** file format. When using a MAX II device as an intelligent host, a design that controls the configuration process, such as fetching the data from flash memory and sending it to the device, must be stored in the MAX II device.

Figure 10–20 shows the configuration interface connections between the Cyclone III device and a MAX II device for single-device configuration.

**Figure 10–20.** Single-Device FPP Configuration Using an External Host




**Notes to Figure 10–20:**

(1) Connect the pull-up resistor to a supply that provides an acceptable input signal for the device. $V_{CC}$ needs to be high enough to meet the $V_{IH}$ specification of the I/O on the device and the external host.

(2) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

(3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 10–14. Connect the MSEL pins directly to $V_{CCA}$ or GND.

(4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. DATA[7..0] and DCLK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

All I/O inputs must maintain a maximum AC voltage of 4.1 V. In a single-device FPP configuration, DATA[7..0] and DCLK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

Upon power-up, Cyclone III devices go through a POR. The POR delay is dependent on the MSEL pin settings which correspond to the configuration scheme that you select. Depending on the configuration scheme, either a fast POR time or a standard POR time is available. The fast POR time is 3 ms < $T_{POR}$ < 9 ms for fast configuration time. The standard POR time is 50 ms < $T_{POR}$ < 200 ms, which has a lower power-ramp rate. During POR, the device resets, holds nSTATUS low, and tri-states all user I/O pins. Once the device successfully exits POR, all user I/O pins continue to be tri-stated. The user I/O pins and dual-purpose I/O pins have weak pull-up resistors, which are always enabled (after POR) before and during configuration.

For more information about the value of the weak pull-up resistors on the I/O pins that are on before and during configuration, refer to the *DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*.

The three stages in the configuration cycle are reset, configuration, and initialization. When nCONFIG or nSTATUS is low, the device is in the reset stage. To initiate configuration, the MAX II device must drive the nCONFIG pin from low-to-high.

To begin configuration, power the $V_{CCINT}$, $V_{CCA}$, and $V_{CCIO}$ (for the banks in which the configuration and JTAG pins reside) voltages to the appropriate voltage levels.

When nCONFIG goes high, the device comes out of reset and releases the open-drain nSTATUS pin, which is then pulled high by an external 10-kΩ pull-up resistor. Once nSTATUS is released, the device is ready to receive configuration data and the configuration stage begins. When nSTATUS is pulled high, the MAX II device places the configuration data one byte at a time on the DATA[7..0] pins.

Cyclone III devices receive configuration data on the DATA[7..0] pins and the clock is received on the DCLK pin. Data is latched into the device on the rising edge of DCLK. Data is continuously clocked into the target device until CONF_DONE goes high. The CONF_DONE pin goes high one byte early in FPP configuration mode. The last byte is required for serial configuration (AS and PS) modes. After the device has received the next to last byte of the configuration data successfully, it releases the open-drain CONF_DONE pin, which is pulled high by an external 10-kΩ pull-up resistor. A low-to-high transition on CONF_DONE indicates configuration is complete and initialization of the device can begin. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize.

Two DCLK falling edges are required after CONF_DONE goes high to begin the initialization of the device.

In Cyclone III devices, the initialization clock source is either the internal oscillator (typically 10 MHz) or the optional CLKUSR pin. By default, the internal oscillator is the clock source for initialization. If you use the internal oscillator, the Cyclone III device provides itself with enough clock cycles for proper initialization. Therefore, if the internal oscillator is the initialization clock source, sending the entire configuration file to the device is sufficient to configure and initialize the device. Driving DCLK to the device after configuration is complete does not affect device operation. Additionally, if you use the internal oscillator as the clock source, you can use the CLKUSR pin as a user I/O pin.

You can also synchronize initialization of multiple devices or to delay initialization with the CLKUSR option. The **Enable user-supplied start-up clock** (**CLKUSR**) option can be turned on in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. Supplying a clock on CLKUSR does not affect the configuration process. The CONF_DONE pin goes high one byte early in a FPP configuration mode.

The last byte is required for serial configuration (AS and PS) modes. After the CONF_DONE pin transitions high, CLKUSR is enabled after the time specified as $t_{CD2CU}$. After this time period elapses, Cyclone III devices require 3,187 clock cycles to initialize properly and enter user mode (for more information about the CLKUSR $f_{MAX}$ value that the Cyclone III devices support, refer to Table 10–15).

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user-mode with a low-to-high transition. This **Enable INIT_DONE Output** option is available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. If you use the INIT_DONE pin, it is high because of an external 10-kΩ pull-up resistor when nCONFIG is low and during the beginning of configuration. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low.

When initialization is complete, the INIT_DONE pin is released and pulled high. The MAX II device must be able to detect this low-to-high transition, which signals the device has entered user mode. When initialization is complete, the device enters user mode. In user mode, the user I/O pins no longer have weak pull-up resistors and function as assigned in your design.

To ensure DCLK and DATA[7..0] are not left floating at the end of configuration, the MAX II device must drive them either high or low, whichever is convenient on your board. The DATA[7..0] pins are available as user I/O pins after configuration. When you select the FPP scheme in the Quartus II software, these I/O pins are tri-stated in user mode by default. To change this default option in the Quartus II software, select the **Dual-Purpose Pins** tab of the **Device and Pin Options** dialog box.

The configuration clock (DCLK) speed must be below the specified frequency to ensure correct configuration. No maximum DCLK period exists, which means you can pause configuration by halting DCLK for an indefinite amount of time.

If an error occurs during configuration, the device drives its nSTATUS pin low, resetting itself internally. The low signal on the nSTATUS pin also alerts the MAX II device that there is an error. If you turn on the **Auto-restart configuration after error** option (available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box, the device releases nSTATUS after a reset time-out period (a maximum of 230 µs). After nSTATUS is released and pulled high by a pull-up resistor, the MAX II device can try to reconfigure the target device without needing to pulse nCONFIG low. If you turn this option off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 500 ns) on CONFIG to restart the configuration process.

The MAX II device can also monitor the CONF_DONE and INIT_DONE pins to ensure successful configuration. The CONF_DONE pin must be monitored by the MAX II device to detect errors and determine when programming completes. If all configuration data is sent, but the CONF_DONE or INIT_DONE signals has not gone high, the MAX II device reconfigures the target device.

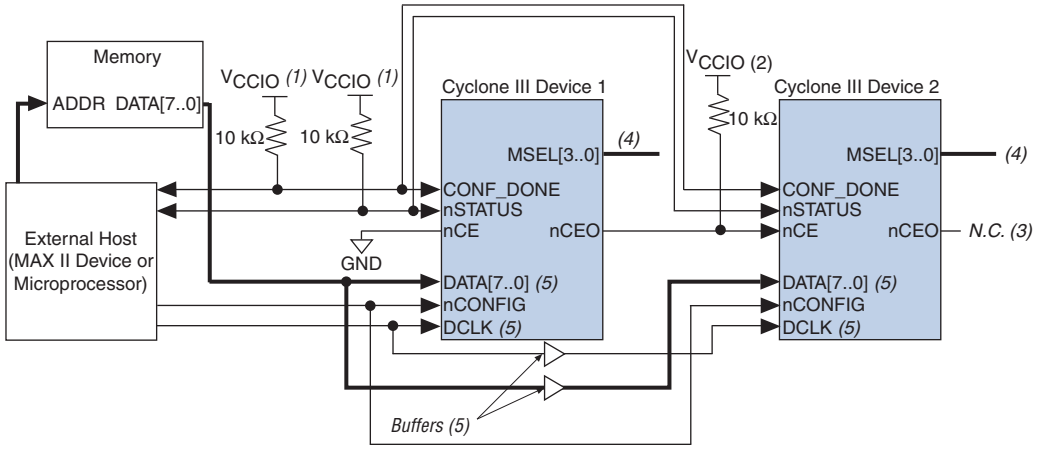
If you use the optional CLKUSR pin and nCONFIG is pulled low to restart configuration during device initialization, ensure CLKUSR continues toggling during the time nSTATUS is low (a maximum of 230 µs).

When the device is in user mode, initiating a reconfiguration is done by transitioning the nCONFIG pin low-to-high. The nCONFIG pin needs to be low for at least 500 ns. When nCONFIG is pulled low, the device also pulls nSTATUS and CONF_DONE low and all I/O pins are tri-stated. When nCONFIG returns to a logic-high level and nSTATUS is released by the device, reconfiguration begins.

For more information about configuration issues, refer to the *Debugging Configuration Problems* chapter in volume 2 of the *Configuration Handbook* and the FPGA Configuration Troubleshooter on the Altera website (www.altera.com).

Figure 10–21 shows how to configure multiple devices using a MAX II device. This circuit is similar to the FPP configuration circuit for a single device, except the Cyclone III devices are cascaded for multi-device configuration.

**Figure 10–21.** Multi-Device FPP Configuration Using an External Host




**Notes to Figure 10–21:**

(1) The pull-up resistor needs to be connected to a supply that provides an acceptable input signal for all devices in the chain. $V_{CC}$ needs to be high enough to meet the $V_{IH}$ specification of the I/O on the device and the external host.

(2) Connect the pull-up resistor to the $V_{CCIO}$ supply voltage of I/O bank in which the nCE pin resides.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 10–14. Connect the MSEL pins directly to $V_{CCA}$ or ground.

(5) All I/O inputs must maintain a maximum AC voltage of 4.1 V. DATA[7..0] and DCLK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

All I/O inputs must maintain a maximum AC voltage of 4.1 V. In a multi-device FPP configuration, DATA[7..0] and DCLK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements". You must connect the repeater buffers between the Cyclone III master and slave device or devices for DATA[7..0] and DCLK.

In a multi-device FPP configuration, the first device's nCE pin is connected to GND while its nCEO pin is connected to the nCE pin of the next device in the chain. The last device's nCE input comes from the previous device, while its nCEO pin is left floating. After the first device completes configuration in a multi-device configuration chain, its nCEO pin drives low to activate the second device's nCE pin, which prompts the second device to begin configuration. The second device in the chain begins configuration within one clock cycle; therefore, the transfer of data destinations is transparent to the MAX II device. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA[7..0], and CONF_DONE) are connected to every device in the chain. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered. All devices initialize and enter user mode at the same time because all device CONF_DONE pins are tied together.

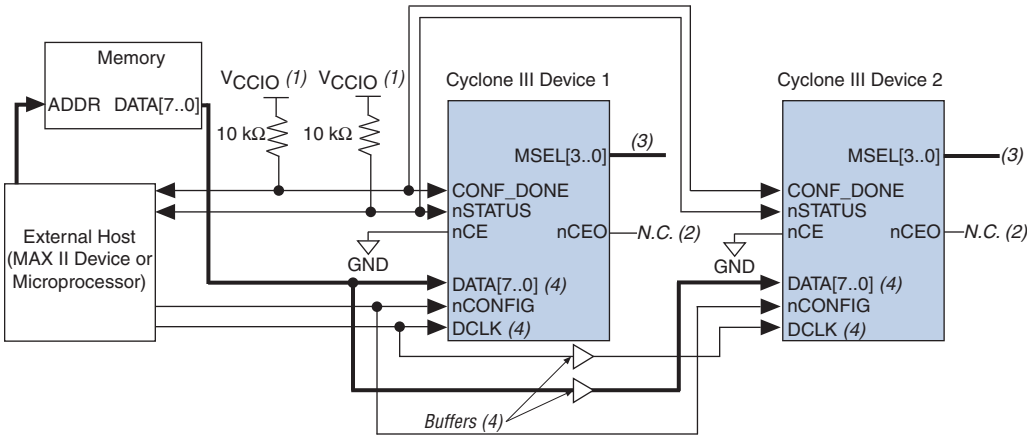
All nSTATUS and CONF_DONE pins are tied together. If any device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured. For example, if the first device flags an error on nSTATUS, it resets the chain by pulling its nSTATUS pin low. This behavior is similar to a single device detecting an error.

If the **Auto-restart configuration after error** option is turned on, the devices release their nSTATUS pins after a reset time-out period (a maximum of 230 µs). After all nSTATUS pins are released and pulled high, the MAX II device tries the to reconfigure the chain without pulsing nCONFIG low. If this option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 500 µs) on nCONFIG to restart the configuration process.

If a system has multiple devices that contain the same configuration data, tie all device nCE inputs to GND, and leave nCEO pins floating. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA[7..0], and CONF_DONE) are connected to every device in the chain. Configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered. Devices must be the same density and package. All devices start and complete configuration at the same time.

Figure 10–22 shows multi-device FPP configuration when both Cyclone III devices are receiving the same configuration data.

**Figure 10–22.** Multi-Device FPP Configuration Using an External Host When Both Devices Receive the Same Data




**Notes to Figure 10–22:**

(1) The pull-up resistor needs to be connected to a supply that provides an acceptable input signal for all devices in the chain. $V_{CC}$ needs to be high enough to meet the $V_{IH}$ specification of the I/O on the device and the external host.

(2) The nCEO pins of both devices can be left unconnected or used as user I/O pins when configuring the same configuration data into multiple devices.

(3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 10–14. Connect the MSEL pins directly to $V_{CCA}$ or GND.

(4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. DATA[7..0] and DCLK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

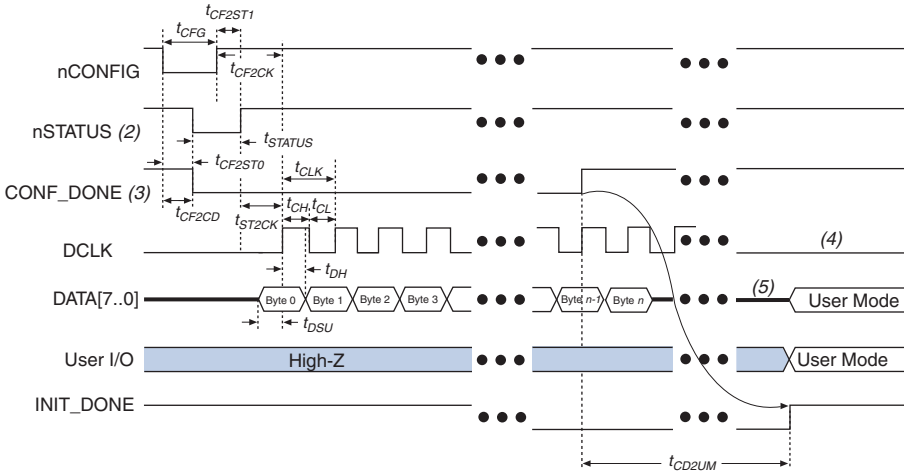
You can use a single configuration chain to configure Cyclone III devices with other Altera devices that support FPP configuration. To ensure that all devices in the chain complete configuration at the same time or that an error flagged by one device initiates reconfiguration in all devices, tie all of the device CONF_DONE and nSTATUS pins together.

For more information about configuring multiple Altera devices in the same configuration chain, refer to *Configuring Mixed Altera FPGA Chains* in volume 2 of the *Configuration Handbook*.

## FPP Configuration Timing

Figure 10–23 shows the timing waveform for FPP configuration when using a MAX II device as an external host.

**Figure 10–23.** FPP Configuration Timing Waveform *(Note 1)*




**Notes to Figure 10–23:**

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) Upon power-up, the Cyclone III device holds nSTATUS low for the time of the POR delay.

(3) Upon power-up, before and during configuration, CONF_DONE is low.

(4) Do not leave DCLK floating after configuration. It needs to be driven high or low, whichever is more convenient.

(5) DATA[7..0] are available as user I/O pins after configuration; the state of these pins depends on the dual-purpose pin settings.

Table 10–15 defines the timing parameters for Cyclone III devices for a FPP configuration.

**Table 10–15.** FPP Timing Parameters for Cyclone III Devices *(Note 1)* (Part 1 of 2)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 500 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 500 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 500 | — | ns |
| $t_{STATUS}$ | nSTATUS low pulse width | 45 | 230 *(2)* | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 230 *(2)* | µs |
| $t_{CF2CK}$ | nCONFIG high to first rising edge on DCLK | 230 *(2)* | — | µs |
| $t_{ST2CK}$ | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | Data setup time before rising edge on DCLK | 5 | — | ns |
| $t_{DH}$ | Data hold time after rising edge on DCLK | 0 | — | ns |
| $t_{CH}$ | DCLK high time | 3.2 | — | ns |
| $t_{CL}$ | DCLK low time | 3.2 | — | ns |
| $t_{CLK}$ | DCLK period | 7.5 | — | ns |
| $f_{MAX}$ | DCLK frequency | — | 100 *(4)* | MHz |

**Table 10–15.** FPP Timing Parameters for Cyclone III Devices *(Note 1)* (Part 2 of 2)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{CD2UM}$ | CONF_DONE high to user mode *(3)* | 300 | 650 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (3,187 × CLKUSR period) | — | — |

**Notes to Table 10–15:**

(1) This information is preliminary.

(2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for starting up the device.

(4) EP3C5, EP3C10, EP3C16, EP3C25, and EP3C40 devices support a DCLK $f_{MAX}$ of 133 MHz. EP3C55, EP3C80, and EP3C120 devices support a DCLK $f_{MAX}$ of 100 MHz.

For more information about device configuration options and how to create configuration files, refer to the *Software Settings* section in volume 2 of the *Configuration Handbook*.

## FPP Configuration Using a Microprocessor

In the FPP configuration scheme, a microprocessor can control the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone III device.

All information in "FPP Configuration Using a MAX II Device as an External Host" is also applicable when using a microprocessor as an external host. For all configuration and timing information, refer to "FPP Configuration Using a MAX II Device as an External Host".

# JTAG Configuration

JTAG has developed a specification for boundary-scan testing. This boundary-scan test (BST) architecture offers the capability to efficiently test components on PCBs with tight lead spacing. The BST architecture can test pin connections without using physical test probes and capture functional data while a device is operating normally. You can also use the JTAG circuitry to shift configuration data into the device. The Quartus II software automatically generates **.sof** files that you can use for JTAG configuration with a download cable in the Quartus II software programmer.

For more information about JTAG boundary-scan testing, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing* chapter in volume 1 of the *Cyclone III Device Handbook*.

Cyclone III devices are designed such that JTAG instructions have precedence over any device configuration modes. Therefore, JTAG configuration can take place without waiting for other configuration modes to complete. For example, if you attempt JTAG configuration of Cyclone III devices during PS configuration, PS configuration terminates and JTAG configuration begins. If the Cyclone III MSEL pins are set to AS mode, the Cyclone III device does not output a DCLK signal when JTAG configuration takes place.

You cannot use the Cyclone III decompression feature if you are configuring your Cyclone III device when using JTAG-based configuration.

The four required pins for a device operating in JTAG mode are TDI, TDO, TMS, and TCK. The TCK pin has an internal weak pull-down resistor, while the TDI and TMS pins have weak internal pull-up resistors (typically 25 kΩ). The TDO output pin is powered by $V_{CCIO}$ in I/O bank 1. All of the JTAG input pins are powered by the $V_{CCIO}$ pin. All the JTAG pins support only LVTTL I/O standard. All user I/O pins are tri-stated during JTAG configuration. Table 10–16 explains each JTAG pin's function.

TDO output is powered by the $V_{CCIO}$ power supply of I/O bank 1.

For recommendations on how to connect a JTAG chain with multiple voltages across devices in the chain, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing* chapter in volume 1 of the *Cyclone III Device Handbook*.

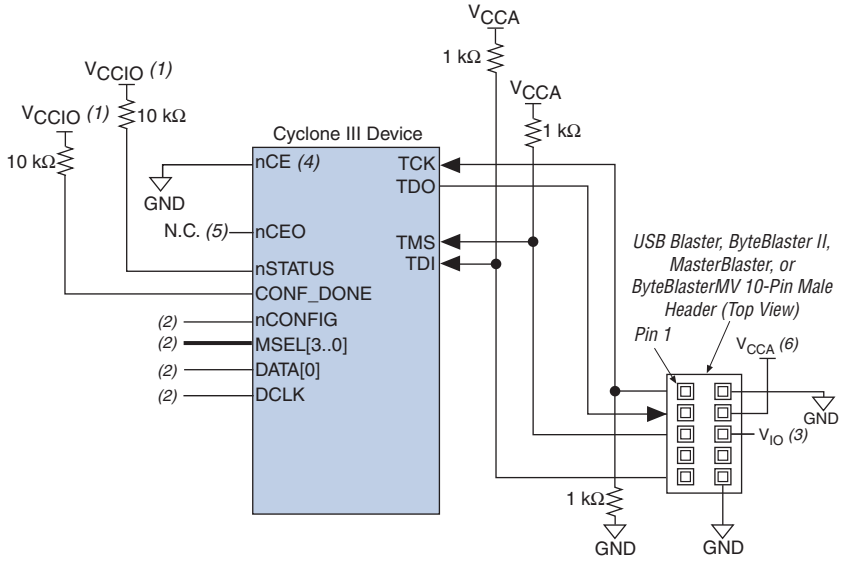
**Table 10–16.** Dedicated JTAG Pins

| Pin Name | Pin Type | Description |
|---|---|---|
| TDI | Test data input | Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to $V_{CC}$. |
| TDO | Test data output | Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by leaving this pin unconnected. |
| TMS | Test mode select | Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur on the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to VCC. |
| TCK | Test clock input | The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to GND. |

You can download data to the device on the PCB through the USB-Blaster, MasterBlaster, ByteBlaster II, or ByteBlasterMV download cable during JTAG configuration. Configuring devices using a cable is similar to programming devices in-system. Figure 10–24 and Figure 10–25 show a JTAG configuration of a single Cyclone III device.

For device $V_{CCIO}$ of 2.5 V, 3.0 V, or 3.3 V, refer to Figure 10–24. All I/O inputs must maintain a maximum AC voltage of 4.1 V. Because JTAG pins do not have the internal PCI clamping diodes to prevent voltage overshoot when using $V_{CCIO}$ of 2.5 V, 3.0 V, or 3.3 V, you must power up the download cable's $V_{CC}$ with a 2.5- V supply from $V_{CCA}$. For device $V_{CCIO}$ of 1.2 V, 1.5 V, or 1.8 V, refer to Figure 10–25. You can power up the download cable's $V_{CC}$ with the supply from $V_{CCIO}$.

**Figure 10–24.** JTAG Configuration of a Single-Device Using a Download Cable (2.5-, 3.0-, or 3.3- V $V_{CCIO}$ Powering the JTAG Pins)




**Notes to Figure 10–24:**

(1) Connect these pull-up resistors to the $V_{CCIO}$ supply of the bank in which the pin resides.

(2) Connect the `nCONFIG` and `MSEL[3..0]` pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the `nCONFIG` pin to logic-high and the `MSEL[3..0]` pins to ground. In addition, pull `DCLK` and `DATA[0]` to either high or low, whichever is convenient on your board.

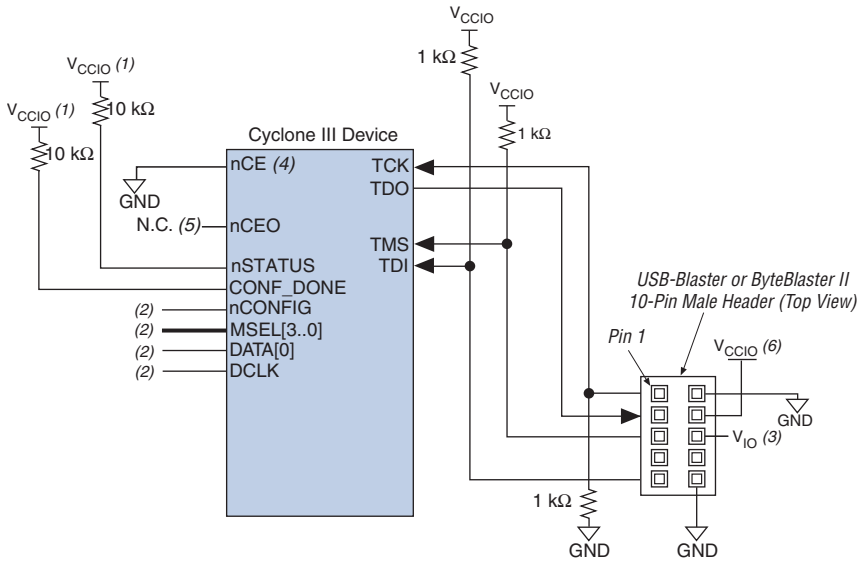
(3) Pin 6 of the header is a $V_{IO}$ reference voltage for the MasterBlaster output driver. $V_{IO}$ needs to match the device's $V_{CCA}$. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. In the USB-Blaster, ByteBlaster II, and ByteBlasterMV, this pin is a no connect.

(4) `nCE` must be connected to GND or driven low for successful JTAG configuration.

(5) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed other device's `nCE` pin.

(6) Power up the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable's $V_{CC}$ with a 2.5- V supply from $V_{CCA}$. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a $V_{CC}$ power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.

**Figure 10–25.** JTAG Configuration of a Single-Device Using a Download Cable (1.5-, or 1.8-V $V_{CCIO}$ Powering the JTAG Pins)




**Notes to Figure 10–25:**

(1) Connect these pull-up resistors to the $V_{CCIO}$ supply of the bank in which the pin resides.

(2) Connect the nCONFIG and MSEL[3..0] pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the nCONFIG pin to logic-high and the MSEL[3..0] pins to ground. In addition, pull DCLK and DATA[0] to either high or low, whichever is convenient on your board.

(3) In the USB-Blaster, ByteBlaster II, and ByteBlasterMV, this pin is a no connect.

(4) nCE must be connected to GND or driven low for successful JTAG configuration.

(5) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

(6) Power up the ByteBlaster II or USB-Blaster cable's $V_{CC}$ with supply from $V_{CCIO}$. The ByteBlaster II and USB-Blaster cables do not support a target supply voltage of 1.2 V. For the target supply voltage value, refer to the *ByteBlaster II Download Cable User Guide* and the *USB-Blaster Download Cable User Guide*.

To configure a single device in a JTAG chain, the programming software places all other devices in bypass mode. In bypass mode, devices pass programming data from the TDI pin to the TDO pin through a single bypass register without being affected internally. This scheme enables the programming software to program or verify the target device. Configuration data driven into the device appears on the TDO pin one clock cycle later.

The Quartus II software verifies successful JTAG configuration upon completion. At the end of configuration, the software checks the state of CONF_DONE through the JTAG port. When the Quartus II software generates a Jam file (.**jam**) file for a multi-device chain, it contains instructions so that all the devices in the chain are initialized at the same time. If CONF_DONE is not high, the Quartus II software indicates that the configuration has failed. If CONF_DONE is high, the software indicates that the configuration was successful. After the configuration bitstream is transmitted serially via the JTAG TDI port, the TCK port is clocked an additional 3,180 cycles to perform device initialization.

Cyclone III devices have dedicated JTAG pins that always function as JTAG pins. Not only can you perform JTAG testing on Cyclone III devices before and after, but also during configuration. Cyclone III devices support BYPASS, IDCODE, and SAMPLE instructions during configuration without interrupting configuration. All other JTAG instructions may only be issued by first interrupting configuration and reprogramming I/O pins using the ACTIVE_DISENGAGE and CONFIG_IO instructions.

The CONFIG_IO instruction allows I/O buffers to be configured via the JTAG port and when issued after the ACTIVE_DISENGAGE instruction, interrupts configuration. This instruction allows you to perform board-level testing prior to configuring the Cyclone III device or waiting for a configuration device to complete configuration. In Cyclone III devices, prior to issuing the CONFIG_IO instruction, you must issue the ACTIVE_DISENGAGE instruction. This is because in Cyclone III devices, the CONFIG_IO instruction does not hold nSTATUS low until reconfiguration, so you must disengage the active configuration mode controller when active configuration is interrupted. The ACTIVE_DISENGAGE instruction places the active configuration mode controllers in an idle state prior to JTAG programming. Additionally, the ACTIVE_ENGAGE instruction allows you to re-engage an already disengaged active configuration mode controller (for more information about the instruction flow, refer to "Cyclone III JTAG Instructions").

You must follow a specific flow when executing the CONFIG_IO, ACTIVE_DISENGAGE, and ACTIVE_ENGAGE JTAG instructions in Cyclone III devices.

The chip-wide reset (DEV_CLRn) and chip-wide output enable (DEV_OE) pins on Cyclone III devices do not affect JTAG boundary-scan or programming operations. Toggling these pins does not affect JTAG operations (other than the usual boundary-scan operation).

When designing a board for JTAG configuration of Cyclone III devices, consider the dedicated configuration pins.

Table 10–17 shows how these pins needs to be connected during JTAG configuration.

**Table 10–17.** Dedicated Configuration Pin Connections During JTAG Configuration (Part 1 of 2)

| Signal | Description |
|---|---|
| nCE | On all Cyclone III devices in the chain, nCE needs to be driven low by connecting it to ground, pulling it low via a resistor, or driving it by some control circuitry. For devices that are also in multi-device AS, AP, PS, or FPP configuration chains, the nCE pins needs to be connected to GND during JTAG configuration or JTAG configured in the same order as the configuration chain. |
| nCEO | On all Cyclone III devices in the chain, nCEO can be left floating or connected to the nCE of the next device. |
| MSEL[3..0] | These pins must not be left floating. These pins support whichever non-JTAG configuration that is used in production. If you only use a JTAG configuration, tie these pins to GND. |
| nCONFIG | Driven high by connecting to $V_{CCIO}$ supply of the bank in which the pin resides and pulling up via a resistor, or driven high by some control circuitry. |
| nSTATUS | Pull to $V_{CCIO}$ supply of the bank in which the pin resides via a 10-kΩ resistor. When configuring multiple devices in the same JTAG chain, each nSTATUS pin needs to be pulled up to $V_{CCIO}$ individually. |

**Table 10–17.** Dedicated Configuration Pin Connections During JTAG Configuration (Part 2 of 2)

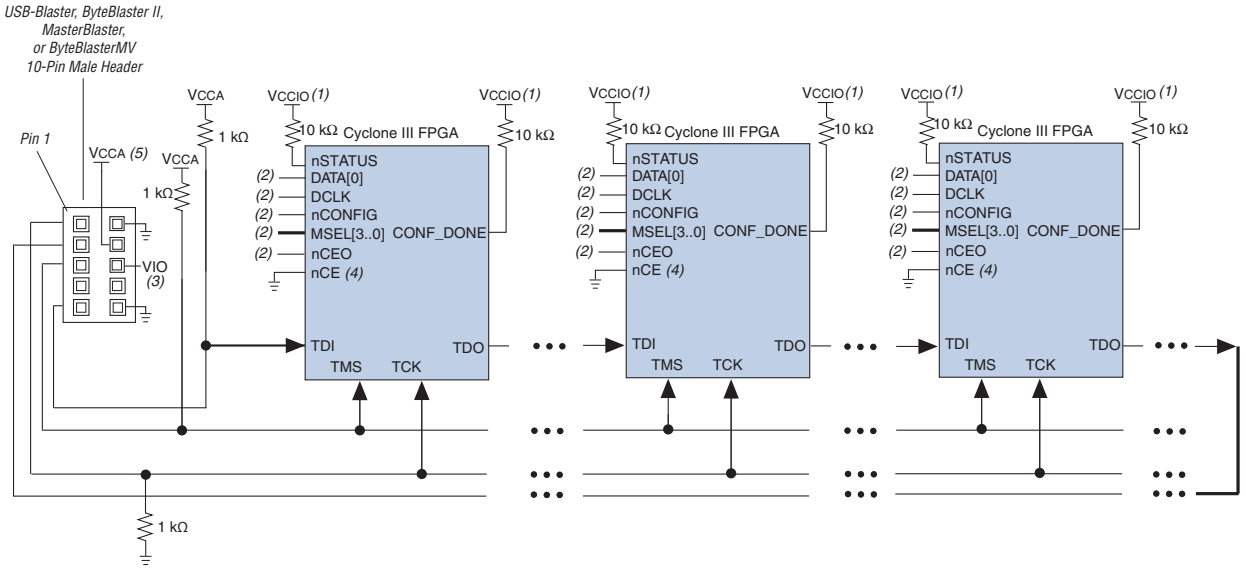
| Signal | Description |
|---|---|
| CONF_DONE | Pull to $V_{CCIO}$ supply of the bank in which the pin resides via a 10-kΩ resistor. When configuring multiple devices in the same JTAG chain, each CONF_DONE pin needs to be pulled up to the $V_{CCIO}$ supply of the bank in which the pin resides individually. CONF_DONE going high at the end of JTAG configuration indicates successful configuration. |
| DCLK | This pin must not be left floating. Drive low or high, whichever is more convenient on your board. |

When programming a JTAG device chain, one JTAG-compatible header is connected to several devices. The number of devices in the JTAG chain is limited only by the drive capability of the download cable. When four or more devices are connected in a JTAG chain, Altera recommends buffering the TCK, TDI, and TMS pins with an on-board buffer.

JTAG-chain device programming is ideal when the system contains multiple devices, or when testing your system using JTAG BST circuitry. Figure 10–26 and Figure 10–27 show a multi-device JTAG configuration.

For device $V_{CCIO}$ of 2.5 V, 3.0 V, or 3.3 V, you must refer to Figure 10–26. All I/O inputs must maintain a maximum AC voltage of 4.1 V. Because JTAG pins do not have the internal PCI clamping diodes to prevent voltage overshoot when using $V_{CCIO}$ of 2.5 V, 3.0 V, or 3.3 V, you must power up the download cable's $V_{CC}$ with a 2.5- V supply from $V_{CCA}$. For device $V_{CCIO}$ of 1.2 V, 1.5 V, or 1.8 V, refer to Figure 10–27. You can power up the download cable's $V_{CC}$ with the supply from $V_{CCIO}$.

**Figure 10–26.** JTAG Configuration of Multiple Devices Using a Download Cable (2.5-, 3.0-, or 3.3- V $V_{CCIO}$ Powering the JTAG Pins)




**Notes to Figure 10–26:**

(1) Connect these pull-up resistors to the $V_{CCIO}$ supply of the bank in which the pin resides.

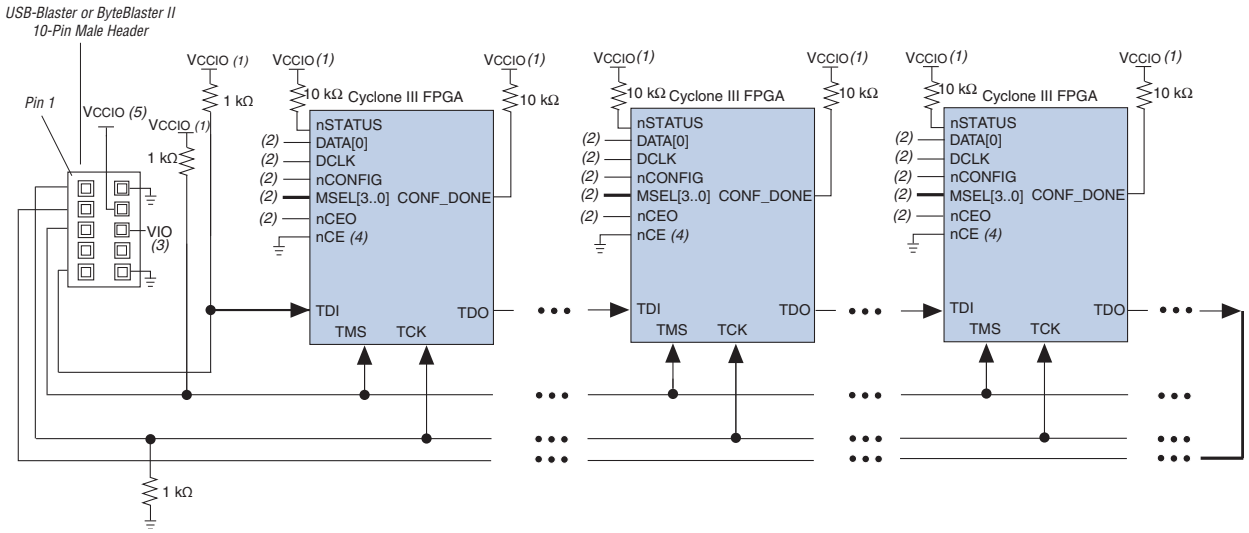
(2) Connect the `nCONFIG` and `MSEL[3..0]` pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the `nCONFIG` pin to logic-high and the `MSEL[3..0]` pins to ground. In addition, pull `DCLK` and `DATA[0]` to either high or low, whichever is convenient on your board.

(3) Pin 6 of the header is a $V_{IO}$ reference voltage for the MasterBlaster output driver. $V_{IO}$ needs to match the device's $V_{CCA}$. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. In the USB-Blaster, ByteBlaster II, and ByteBlasterMV, this pin is a no connect.

(4) `nCE` must be connected to ground or driven low for successful JTAG configuration.

(5) Power up the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable's $V_{CC}$ with a 2.5- V supply from $V_{CCA}$. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a $V_{CC}$ power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications User Guide*.

**Figure 10–27.** JTAG Configuration of Multiple Devices Using a Download Cable (1.2-, 1.5-, or 1.8- V $V_{CCIO}$ Powering the JTAG Pins)




**Notes to Figure 10–27:**

(1) Connect these pull-up resistors to the $V_{CCIO}$ supply of the bank in which the pin resides.

(2) Connect the nCONFIG and MSEL[3..0] pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the nCONFIG pin to logic-high and the MSEL[3..0] pins to ground. In addition, pull DCLK and DATA[0] to either high or low, whichever is convenient on your board.

(3) In the USB-Blaster, ByteBlaster II, and ByteBlasterMV, this pin is a no connect.

(4) nCE must be connected to ground or driven low for successful JTAG configuration.

(5) Power up the ByteBlaster II or USB-Blaster cable's $V_{CC}$ with supply from $V_{CCIO}$. The ByteBlaster II and USB-Blaster cables do not support a target supply voltage of 1.2 V. For the target supply voltage value, refer to the *ByteBlaster II Download Cable User Guide* and the *USB-Blaster Download Cable User Guide*.

All I/O inputs must maintain a maximum AC voltage of 4.1V. If a non-Cyclone III device is cascaded in the JTAG-chain, TDO of the non-Cyclone III device driving into TDI of Cyclone III must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

The nCE pin must be connected to GND or driven low during JTAG configuration. In multi-device AS, AP, PS, and FPP configuration chains, the first device's nCE pin is connected to GND while its nCEO pin is connected to the nCE pin of the next device in the chain. The last device's input for the nCE pin comes from the previous device, while its nCEO pin is left floating. In addition, the CONF_DONE and nSTATUS signals are all shared in multi-device AS, AP, PS, and FPP configuration chains so the devices can enter user mode at the same time after configuration is complete. When the CONF_DONE and nSTATUS signals are shared among all the devices, every device must be configured when JTAG configuration is performed.

If you only use JTAG configuration, Altera recommends that you connect the circuitry shown in Figure 10–26 or Figure 10–27, where each of the CONF_DONE and nSTATUS signals are isolated so that each device can enter user mode individually.

After the first device completes configuration in a multi-device configuration chain, its nCEO pin drives low to activate the second device's nCE pin, which prompts the second device to begin configuration. Therefore, if these devices are also in a JTAG chain, make sure the nCE pins are connected to GND during JTAG configuration or that the devices are JTAG configured in the same order as the configuration chain. As long as the devices are JTAG configured in the same order as the multi-device configuration chain, the nCEO of the previous device drives the nCE pin of the next device low when it has successfully been JTAG configured.

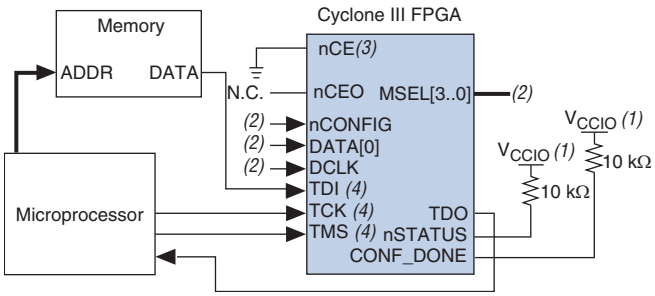
You can place other Altera devices that have JTAG support in the same JTAG chain for device programming and configuration.

JTAG configuration allows an unlimited number of Cyclone III devices to be cascaded in a JTAG chain.

For more information about configuring multiple Altera devices in the same configuration chain, refer to the *Configuring Mixed Altera FPGA Chains* chapter in volume 2 of the *Configuration Handbook*.

Figure 10–28 shows a JTAG configuration of a Cyclone III device with a microprocessor.

**Figure 10–28.** JTAG Configuration of a Single-Device Using a Microprocessor




**Notes to Figure 10–28:**

(1) The pull-up resistor needs to be connected to a supply that provides an acceptable input signal for all devices in the chain.

(2) Connect the nCONFIG and MSEL[3..0] pins to support a non-JTAG configuration scheme. If you only use a JTAG configuration, connect the nCONFIG pin to logic-high and the MSEL[3..0] pins to ground. In addition, pull DCLK and DATA[0] to either high or low, whichever is convenient on your board.

(3) nCE must be connected to GND or driven low for successful JTAG configuration.

(4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. Signals driving into TDI, TMS, and TCK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

All I/O inputs must maintain a maximum AC voltage of 4.1 V. Signals driving into TDI, TMS, and TCK must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements".

## Jam STAPL

Jam STAPL, JEDEC standard JESD-71, is a standard file format for in-system programmability (ISP) purposes. Jam STAPL supports programming or configuration of programmable devices and testing of electronic systems, using the IEEE 1149.1 JTAG interface. Jam STAPL is a freely licensed open standard.

The Jam Player provides an interface for manipulating the IEEE Std. 1149.1 JTAG TAP state machine.

For more information about JTAG and Jam STAPL in embedded environments, refer to *AN 425: Using Command-Line Jam STAPL Solution for Device Programming*. To download the Jam Player, visit the Altera website (www.altera.com).

## Configuring Cyclone III Devices with JRunner

JRunner is a software driver that allows you to configure Cyclone III devices through ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in a **.rbf** file format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code has been developed for the Windows NT OS. You can customize the code to make it run on your embedded platform.

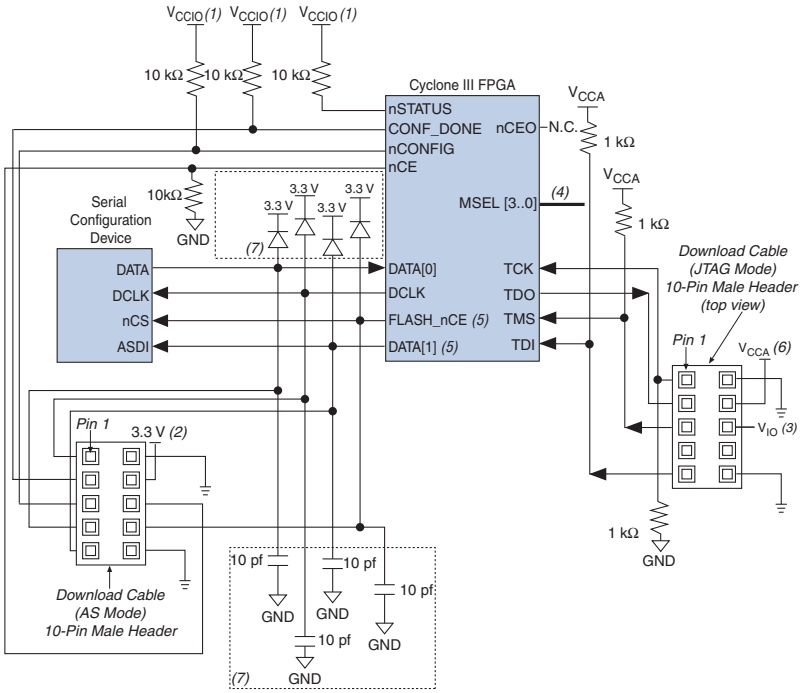
The **.rbf** file used by the JRunner software driver cannot be a compressed **.rbf** file because JRunner uses JTAG-based configuration. During JTAG-based configuration, the real-time decompression feature is not available.

For more information about the JRunner software driver, refer to *AN 414: JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera website (www.altera.com).

## Combining JTAG and Active Serial Configuration Schemes

You can combine the AS configuration scheme with the JTAG-based configuration (Figure 10–29). This setup uses two 10-pin download cable headers on the board. One download cable is used in JTAG mode to configure the Cyclone III device directly via the JTAG interface. The other download cable is used in AS mode to program the serial configuration device in-system via the AS programming interface. The `MSEL[3..0]` pins needs to be set to select the AS configuration mode (refer to Table 10–6). If you try configuring the device using both schemes simultaneously, the JTAG configuration takes precedence and AS configuration terminates.

**Figure 10–29.** Combining JTAG and AS Configuration Schemes




**Notes to Figure 10–29:**

(1) Connect these pull-up resistors to the $V_{CCIO}$ supply of the bank in which the pin resides.

(2) Power up the ByteBlaster II or USB-Blaster cable's $V_{CC}$ with the 3.3- V supply.

(3) Pin 6 of the header is a $V_{IO}$ reference voltage for the MasterBlaster output driver. $V_{IO}$ needs to match the device's $V_{CCA}$. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. In the USB-Blaster, ByteBlaster II, and ByteBlasterMV, this pin is a no connect..

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect `MSEL[3..0]`, refer to Table 10–6 for AS configuration schemes. Connect the MSEL pins directly to $V_{CCA}$ or GND.

(5) These are dual-purpose I/O pins. The `FLASH_nCE` pin functions as the `nCSO` pin in the AS configuration scheme. The `DATA[1]` pin functions as the `ASDO` pin in AS configuration scheme.

(6) Power up the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable's $V_{CC}$ with a 2.5- V supply from $V_{CCA}$. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a $V_{CC}$ power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.

(7) The diodes and capacitors must be placed as close as possible to the Cyclone III device. Altera recommends using the Schottky diode, which has a relatively lower forward diode voltage (VF) than the switching and Zener diodes, for effective voltage clamping.

## Programming Serial Configuration Devices In-System Using the JTAG Interface

Cyclone III devices in a single-device chain or in a multiple-device chain support in-system programming of a serial configuration device using the JTAG interface via the serial flash loader design. The board's intelligent host or download cable can use the four JTAG pins on the Cyclone III device to program the serial configuration device in system, even if the host or download cable cannot access the configuration device's configuration pins (`DCLK`, `DATA`, `ASDI`, and `nCS` pins).

The serial flash loader design is a JTAG-based in-system programming solution for Altera serial configuration devices. The serial flash loader is a bridge design for the Cyclone III device that uses its JTAG interface to access the EPCS **.jic** file and then uses the AS interface to program the EPCS device. Both the JTAG interface and AS interface are bridged together inside the serial flash loader design.

In a multiple device chain, you only need to configure the master Cyclone III device which is controlling the serial configuration device. The slave devices in the multiple device chain which are configured by the serial configuration device do not need to be configured when using this feature. To use this feature successfully, set the MSEL[3..0] pins of the master Cyclone III device to select the AS configuration scheme (refer to Table 10–6).

The serial configuration device in-system programming through the Cyclone III JTAG interface has three stages, which are described in the following sections.

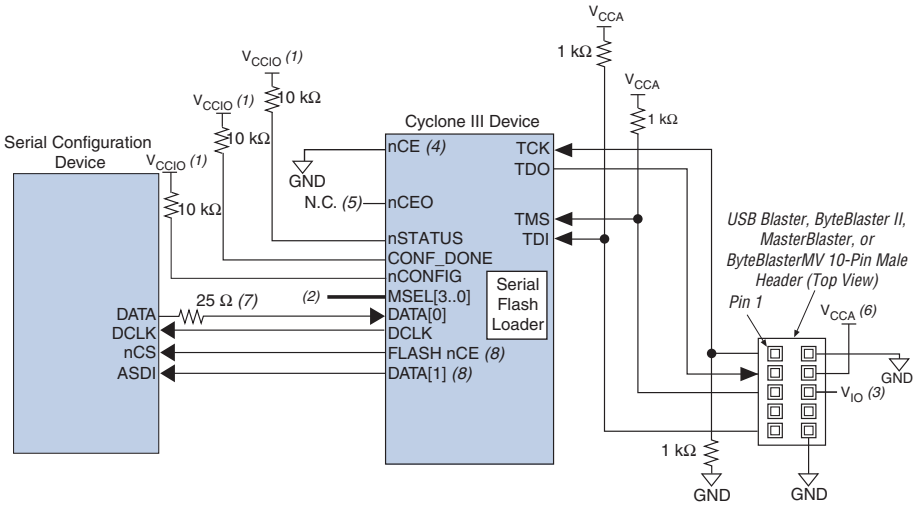
### Loading the Serial Flash Loader Design

The serial flash loader design is a design inside the Cyclone III device that bridges the JTAG interface and AS interface inside the Cyclone III device using glue logic.

The intelligent host uses the JTAG interface to configure the master Cyclone III device with a serial flash loader design. The serial flash loader design allows the master Cyclone III device to control the access of four serial configuration device pins, also known as the Active Serial Memory Interface (ASMI) pins, through the JTAG interface. The ASMI pins are serial clock input (DCLK), serial data output (DATA), AS data input (ASDI), and active-low chip select (nCS) pins.

If you configure a master Cyclone III device with a serial flash loader design, the master Cyclone III device can enter user mode even though the slave devices in the multiple device chain are not being configured. The master Cyclone III device can enter user mode with a serial flash loader design even though the CONF_DONE signal is externally held low by the other slave devices in chain. Figure 10–30 shows the JTAG configuration of a single Cyclone III device with a serial flash loader design.

**Figure 10–30.** Programming Serial Configuration Devices In-System Using the JTAG Interface




**Notes to Figure 10–30:**

(1) Connect the pull-up resistors to the $V_{CCIO}$ supply of the bank in which the pin resides.

(2) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect `MSEL[3..0]`, refer to Table 10–6 for AS configuration schemes. Connect the MSEL pins directly to $V_{CCA}$ or GND.

(3) Pin 6 of the header is a $V_{IO}$ reference voltage for the MasterBlaster output driver. $V_{IO}$ needs to match the device's $V_{CCA}$. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*. In the USB-Blaster, ByteBlaster II, and ByteBlasterMV, this pin is a no connect.

(4) `nCE` must be connected to GND or driven low for successful JTAG configuration.

(5) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed other device's `nCE` pin.

(6) Power up the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable's $V_{CC}$ with a 2.5- V supply from $V_{CCA}$. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a $V_{CC}$ power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. For this value, refer to the *MasterBlaster Serial/USB Communications Cable User Guide*.

(7) Connect the series resistor at the near end of the serial configuration device.

(8) These are dual-purpose I/O pins. The `FLASH_nCE` pin functions as the `nCSO` pin in the AS configuration scheme. The `DATA[1]` pin functions as the `ASDO` pin in AS configuration scheme.

## ISP of Serial Configuration Device

In the second stage, the serial flash loader design in the master Cyclone III device allows you to write the configuration data for the device chain into the serial configuration device by using the Cyclone III JTAG interface. The JTAG interface sends the programming data for the serial configuration device to the Cyclone III device first. The Cyclone III device then uses the `ASMI` pins to transmit the data to the serial configuration device.

## Reconfiguration

After all the configuration data is written into the serial configuration device successfully, the Cyclone III device does not reconfigure by itself. The intelligent host issues the `PULSE_NCONFIG` JTAG instruction to initialize the reconfiguration process. During reconfiguration, the master Cyclone III device is reset and the serial flash loader design no longer exists in the Cyclone III device and the serial configuration device configures all the devices in the chain with your user design.

For more information about the SFL, refer to *AN 370: Using the Serial FlashLoader with Quartus II Software*.

# Cyclone III JTAG Instructions

This section describes a few JTAG instructions for Cyclone III devices. These instructions are CONFIG_IO, ACTIVE_DISENGAGE, ACTIVE_ENGAGE, EN_ACTIVE_CLK, DIS_ACTIVE_CLK, and APFC_BOOT_ADDR.

For more information about the JTAG binary instruction code, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing* chapter in volume 1 of the *Cyclone III Device Handbook*.

## I/O Reconfiguration

The CONFIG_IO instruction is used to reconfigure the I/O configuration shift register (IOCSR) chain. This instruction allows you to perform board-level testing prior to configuring the Cyclone III device or waiting for a configuration device to complete configuration. Once configuration has been interrupted and JTAG testing is complete, the part must be reconfigured via JTAG (PULSE_NCONFIG instruction) or by pulsing the nCONFIG pin low.

You can issue the CONFIG_IO instruction any time during user mode. The CONFIG_IO instruction cannot be issued while the nCONFIG pin is asserted low (during power up) or immediately after issuing a JTAG instruction that triggers reconfiguration (for the wait time for issuing the CONFIG_IO instruction, refer to Table 10–18).

You must meet the following timing restrictions when using the CONFIG_IO instruction:

- CONFIG_IO instruction cannot be issued during nCONFIG pin low
- Observe a 230 ms minimum wait time after any one of the following conditions:
  - nCONFIG pin goes high
  - issuing PULSE_NCONFIG instruction
  - issuing ACTIVE_ENGAGE instruction, before issuing CONFIG_IO instruction
- Wait 230 ms after power up, with nCONFIG pin high before issuing CONFIG_IO instruction (or wait for the nSTATUS pin to go high).

**Table 10–18.** Wait Time for Issuing the CONFIG_IO Instruction

| Wait Time | Time |
|---|---|
| Wait time after nCONFIG pin is released. | 230 ms |
| Wait time after PULSE_NCONFIG or ACTIVE_ENGAGE is issued | 230 ms |

The ACTIVE_DISENGAGE instruction can be used together with the CONFIG_IO instruction to interrupt configuration. Table 10–19 shows the sequence of instructions to use for various CONFIG_IO usage scenarios.

**Table 10–19.** JTAG CONFIG_IO (without JTAG_PROGRAM) Instruction Flows *(Note 1)*

| JTAG Instruction | Configuration Scheme and Current State of the Cyclone III Device | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Prior to User Mode (Interrupting Configuration) | | | | User Mode | | | | Power Up | | | |
| | PS | FPP | AS | AP | PS | FPP | AS | AP | PS | FPP | AS | AP |
| ACTIVE_DISENGAGE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — |
| CONFIG_IO | R | R | R | R | R | R | R | R | NA | NA | NA | NA |
| JTAG Boundary Scan Instructions (no JTAG_PROGRAM) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — |
| ACTIVE_ENGAGE | A | A | R *(2)* | R *(2)* | A | A | R *(2)* | R *(2)* | — | — | — | — |
| PULSE_NCONFIG | | | A *(3)* | A *(3)* | | | 0 | 0 | — | — | — | — |
| Pulse nCONFIG pin | | | A *(3)* | A *(3)* | | | 0 | 0 | — | — | — | — |
| JTAG TAP Reset | R | R | R | R | R | R | R | R | — | — | — | — |

**Notes to Table 10–19:**

(1) "R" indicates required, "O" indicates optional, "A" indicates any of these instructions, and "NA" indicates not allowed.

(2) Required if ACTIVE_DISENGAGE is used.

(3) Neither of the instructions is required if ACTIVE_ENGAGE is used.

The instructions ACTIVE_DISENGAGE and ACTIVE_ENGAGE are unique to Cyclone III devices, and are related to the change to CONFIG_IO instruction. Since in Cyclone III devices, the CONFIG_IO instruction does not hold nSTATUS pin low until reconfiguration, you must disengage the active configuration (AS and AP) controllers when active configuration is interrupted. You must issue the ACTIVE_DISENGAGE instruction alone or prior to the CONFIG_IO instruction if the JTAG_PROGRAM instruction is to be issued later (refer to Table 10–20). This puts the active configuration controllers into idle state. The active configuration controller is re-engaged once user mode is reached via JTAG programming (refer to Table 10–20).

While executing the CONFIG_IO instruction, all user IOs are tri-stated.

If reconfiguration after interruption is performed using configuration modes (rather than using JTAG_PROGRAM), it is not necessary to issue the ACTIVE_DISENGAGE instruction prior to CONFIG_IO. You can initiate reconfiguration by either pulling the nCONFIG pin low for at least 500 ns, or issuing the PULSE_NCONFIG instruction. In the case where the ACTIVE_DISENGAGE instruction was issued and the JTAG_PROGRAM instruction failed to enter user mode, you must issue the ACTIVE_ENGAGE instruction to reactivate the active configuration (AS and AP) controller. Issuing the ACTIVE_ENGAGE instruction also triggers reconfiguration in configuration modes; therefore, it is not necessary to pull the nCONFIG pin low or issue the PULSE_NCONFIG instruction.

### ACTIVE_DISENGAGE

ACTIVE_DISENGAGE is a unique JTAG instruction on Cyclone III devices that places the active configuration (AS and AP) controllers into an idle state prior to JTAG programming. The active configuration controllers are the AS controller when the MSEL pins are set to the AS configuration scheme, and the AP controller when the MSEL pins are set to the AP configuration scheme. The two purposes of placing the active controllers in an idle state is to ensure that they are not trying to configure the device in their respective configuration modes during JTAG programming and to allow the controllers to properly recognize a successful JTAG programming that results in the device reaching user mode.

The ACTIVE_DISENGAGE instruction is required before JTAG programming regardless of the current state of the Cyclone III device if the MSEL pins are set to an active configuration scheme (AS or AP). The ACTIVE_DISENGAGE instruction can be issued during a passive configuration scheme (PS or FPP) with no effect on the Cyclone III device. Similarly, the CONFIG_IO instruction can be issued after an ACTIVE_DISENGAGE instruction, but is no longer required to properly halt configuration.

For a summary of the required, recommended, and optional instructions for each configuration mode, refer to Table 10–20. The ordering of the required instructions is a hard requirement and must be met to ensure functionality.

**Table 10–20.** JTAG Programming Instruction Flows *(Note 1)*

| JTAG Instruction | Configuration Scheme and Current State of the Cyclone III Device | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Prior to User Mode (Interrupting Configuration) | | | | User Mode | | | | Power Up | | | |
| | PS | FPP | AS | AP | PS | FPP | AS | AP | PS | FPP | AS | AP |
| ACTIVE_DISENGAGE | O | O | R | R | O | O | O | R | O | O | R | R |
| CONFIG_IO | Rc | Rc | O | O | O | O | O | O | NA | NA | NA | NA |
| Other JTAG instructions | O | O | O | O | O | O | O | O | O | O | O | O |
| JTAG_PROGRAM | R | R | R | R | R | R | R | R | R | R | R | R |
| CHECK_STATUS | Rc | Rc | Rc | Rc | Rc | Rc | Rc | Rc | Rc | Rc | Rc | Rc |
| JTAG_STARTUP | R | R | R | R | R | R | R | R | R | R | R | R |
| JTAG TAP Reset/ other instruction | R | R | R | R | R | R | R | R | R | R | R | R |

**Note to Table 10–20:**

(1) "R" indicates required, "O" indicates optional, "Rc" indicates recommended, and "NA" indicates not allowed.

The effect of the ACTIVE_DISENGAGE instruction is similar to the AS and AP controllers. In the AS or AP configuration scheme, the ACTIVE_DISENGAGE instruction puts the active configuration controllers into idle state. If a successful JTAG programming is executed, the active controllers are automatically re-engaged once user mode is reached via JTAG programming. This causes the active controllers to transition to their respective user mode states.

If JTAG programming is not successful in getting the Cyclone III device to user mode and re-engage the active programming, the methods available to achieve this are different for the AS and AP configuration schemes. When in the AS configuration scheme, you can re-engage the AS controller either by moving the JTAG TAP controller to the reset state or by issuing the ACTIVE_ENGAGE instruction. When in the AP configuration scheme, the only way to re-engage the AP controller is to issue the ACTIVE_ENGAGE instruction. In this case, asserting the nCONFIG pin will not re-engage either active controller.

### ACTIVE_ENGAGE

The ACTIVE_ENGAGE instruction allows you to re-engage an already disengaged active controller. You can issue this instruction any time during configuration or user mode to re-engage an already disengaged active controller as well as trigger reconfiguration of the Cyclone III device in active configuration scheme specified by the MSEL pin settings.

The ACTIVE_ENGAGE instruction functions as the PULSE_NCONFIG instruction when the device is in passive configuration schemes (PS or FPP). The nCONFIG pin is disabled when the ACTIVE_ENGAGE instruction is issued.

You should never have to use the ACTIVE_ENGAGE instruction but it is provided as a fail-safe instruction for re-engaging the active configuration (AS and AP) controllers.

## Overriding the Internal Oscillator

This feature allows you to override the internal oscillator during the active configuration scheme. The active configuration (AS and AP) controllers use the internal oscillator as the clock source. You can change the clock source to CLKUSR through JTAG instruction.

The JTAG instructions EN_ACTIVE_CLK and DIS_ACTIVE_CLK toggle on or off whether the active clock is sourced from the CLKUSR pin or the internal configuration oscillator. To source the active clock from the CLKUSR pin, issue the EN_ACTIVE_CLK instruction. This causes the CLKUSR pin to become the active clock source. When using the EN_ACTIVE_CLK instruction, the internal oscillator must be enabled for the clock change to occur. By default, the configuration oscillator is disabled once configuration and initialization is complete and the device has entered user mode. However, the internal oscillator is enabled in user mode by either one of the following conditions:

- A reconfiguration event (for example, driving nCONFIG low)
- Remote update is enabled
- Error detection is enabled

You must clock the CLKUSR pin at two times the expected DCLK frequency. The CLKUSR pin allows a maximum frequency of 80 MHz (40 MHz DCLK). Normally, a test instrument uses the CLKUSR pin when it wants to drive its own clock to control the AS state machine.

To revert the clock source back to the configuration oscillator, issue the DIS_ACTIVE_CLK instruction. After you issues the DIS_ACTIVE_CLK instruction, you must continue to clock the CLKUSR pin for 10 clock cycles. Otherwise, even toggling the nCONFIG pin will not revert the clock source and reconfiguration will not occur. A POR reverts the clock source back to the configuration oscillator. Toggling the nCONFIG pin or driving the JTAG state machine to the reset state will not revert the clock source.

### EN_ACTIVE_CLK

The EN_ACTIVE_CLK instruction causes the CLKUSR pin signal to replace the internal oscillator as the clock source. When using the EN_ACTIVE_CLK instruction, the internal oscillator must be enabled in order for the clock change to occur. After this instruction is issued, other JTAG instructions can be issued while the CLKUSR pin signal remains as the clock source. The clock source is only reverted back to the internal oscillator by issuing the DIS_ACTIVE_CLK instruction or a POR.

### DIS_ACTIVE_CLK

The DIS_ACTIVE_CLK instruction breaks the CLKUSR enable latch set by the EN_ACTIVE_CLK instruction and causes the clock source to revert back to the internal oscillator. After the DIS_ACTIVE_CLK instruction is issued, you must continue to clock the CLKUSR pin for 10 clock cycles.

The CLKUSR pin must be clocked at two times the expected DCLK frequency. The CLKUSR pin allows a maximum frequency of 80 MHz (40 MHz DCLK).

## Changing the Start Boot Address of the AP Flash

In the AP configuration scheme, you can change the default configuration boot address of the parallel flash memory to any desired address using the JTAG instruction APFC_BOOT_ADDR.

### APFC_BOOT_ADDR

The APFC_BOOT_ADDR instruction defines a start boot address for the parallel flash memory in the AP configuration scheme.

This instruction shifts in a start boot address for the AP flash. When this instruction becomes the active instruction, TDI and TDO are connected through a 22-bit active boot address shift register. The shifted-in boot address bits get loaded into the 22-bit AP boot address update register, which feeds into the AP controller. The content of the AP boot address update register can be captured and shifted-out of the active boot address shift register from TDO.

The boot address in the boot address shift register and update register are shifted to the right (in the LSB direction) by two bits versus the intended boot address. The reason for this is that the two LSB of the address are not accessible. When this boot address is fed into the AP controller, two 0s are attached in the end as least significant bits thereby pushing the shifted-in boot address to the left by two bits, which becomes the actual AP boot address the AP controller gets.

When the remote update feature is enabled, the APFC_BOOT_ADDR instruction sets the boot address for the factory configuration only.

The APFC_BOOT_ADDR instruction is retained after reconfiguration while the system board is still powered on. However, you must reprogram the instruction whenever you restart the system board.

# Device Configuration Pins

The following tables describe the connections and functionality of all the configuration-related pins on Cyclone III devices. Table 10–21 summarizes the Cyclone III pin configuration.

**Table 10–21.** Cyclone III Configuration Pin Summary (Part 1 of 2)

| Bank | Description | Input/Output | Dedicated | Powered By | Configuration Mode |
|---|---|---|---|---|---|
| 1 | FLASH_nCE, nCSO | Output | — | $V_{CCIO}$ | AS, AP |
| 6 | CRC_ERROR | Output | — | $V_{CCIO}$/ Pull-up *(1)* | Optional, all modes |
| 1 | DATA[0] | Input | Yes | $V_{CCIO}$ | PS, FPP, AS |
| | | Bidirectional | | $V_{CCIO}$ | AP |
| 1 | DATA[1], ASDO | Input | — | $V_{CCIO}$ | FPP |
| | | Output | | $V_{CCIO}$ | AS |
| | | Bidirectional | | $V_{CCIO}$ | AP |
| 8 | DATA[7..2] | Input | — | $V_{CCIO}$ | FPP |
| | | Bidirectional | | $V_{CCIO}$ | AP |
| 8 | DATA[15..8] | Bidirectional | | $V_{CCIO}$ | AP |
| 6 | INIT_DONE | Output | — | Pull-up | Optional, all modes |
| 1 | nSTATUS | Bidirectional | Yes | Pull-up | All modes |
| 1 | nCE | Input | Yes | $V_{CCIO}$ | All modes |
| 1 | DCLK | Input | Yes | $V_{CCIO}$ | PS, FPP |
| | | Output | | $V_{CCIO}$ | AS, AP |
| 6 | CONF_DONE | Bidirectional | Yes | Pull-up | All modes |
| 1 | TDI | Input | Yes | $V_{CCIO}$ | JTAG |
| 1 | TMS | Input | Yes | $V_{CCIO}$ | JTAG |
| 1 | TCK | Input | Yes | $V_{CCIO}$ | JTAG |
| 1 | nCONFIG | Input | Yes | $V_{CCIO}$ | All modes |
| 6 | CLKUSR | Input | — | $V_{CCIO}$ | Optional |
| 6 | nCEO | Output | — | $V_{CCIO}$ | Optional, all modes |
| 6 | MSEL[3..0] | Input | Yes | $V_{CCINT}$ | All modes |
| 1 | TDO | Output | Yes | $V_{CCIO}$ | JTAG |
| 7 | PADD[14..0] | Output | — | $V_{CCIO}$ | AP |
| 8 | PADD[19..15] | Output | — | $V_{CCIO}$ | AP |
| 6 | PADD[23..20] | Output | — | $V_{CCIO}$ | AP |
| 1 | nRESET | Output | — | $V_{CCIO}$ | AP |
| 6 | nAVD | Output | — | $V_{CCIO}$ | AP |

**Table 10–21.** Cyclone III Configuration Pin Summary (Part 2 of 2)

| Bank | Description | Input/Output | Dedicated | Powered By | Configuration Mode |
|---|---|---|---|---|---|
| 6 | nOE | Output | — | $V_{CCIO}$ | AP |
| 6 | nWE | Output | — | $V_{CCIO}$ | AP |
| 5 | DEV_OE | Input | — | $V_{CCIO}$ | Optional, AP |
| 5 | DEV_CLRn | Input | — | $V_{CCIO}$ | Optional, AP |

**Note to Table 10–21:**

(1) By default, the CRC_ERROR pin is a dedicated output. Optionally, you can enable the CRC_ERROR pin as an open-drain output in the CRC Error Detection tab from the **Device and Pin Options** dialog box.

Table 10–22 describes the dedicated configuration pins, which need to be connected properly on your board for successful configuration. Some of these pins may not be required for your configuration scheme.

**Table 10–22.** Dedicated Configuration Pins on the Cyclone III Device (Part 1 of 5)

| Pin Name | User Mode | Configuration Scheme | Pin Type | Description |
|---|---|---|---|---|
| MSEL[3..0] | N/A | All | Input | 4-bit configuration input that sets the Cyclone III device configuration scheme. Some of the smaller devices or package options do not support the AP configuration scheme and do not have the MSEL[3] pin. For the appropriate connections, refer to Table 10–1.<br>These pins must be hardwired to $V_{CCA}$ or GND.<br>The MSEL[3..0] pins have internal 9-kΩ pull-down resistors that are always active. |
| nCONFIG | N/A | All | Input | Configuration control input. Pulling this pin low with an external circuitry during user mode causes the Cyclone III device to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic-high level initiates a reconfiguration. |

**Table 10–22.** Dedicated Configuration Pins on the Cyclone III Device (Part 2 of 5)

| Pin Name | User Mode | Configuration Scheme | Pin Type | Description |
|---|---|---|---|---|
| nSTATUS | N/A | All | Bidirectional open-drain | The Cyclone III device drives nSTATUS low immediately after power-up and releases it after the POR time.<br>Status output. If an error occurs during configuration, nSTATUS is pulled low by the target device.<br>Status input. If an external source (for example, another Cyclone III device) drives the nSTATUS pin low during configuration or initialization, the target device enters an error state.<br>Driving nSTATUS low after configuration and initialization does not affect the configured device. If you use a configuration device, driving nSTATUS low causes the configuration device to attempt to configure the device, but because the device ignores transitions on nSTATUS in user mode, the device does not reconfigure. To initiate a reconfiguration, nCONFIG must be pulled low. |
| CONF_DONE | N/A | All | Bidirectional open-drain | Status output. The target Cyclone III device drives the CONF_DONE pin low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, the target device releases CONF_DONE.<br>Status input. After all data is received and CONF_DONE goes high, the target device initializes and enters user mode. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize.<br>Driving CONF_DONE low after configuration and initialization does not affect the configured device. |
| nCE | N/A | All | Input | Active-low chip enable. The nCE pin activates the Cyclone III device with a low signal to allow configuration. The nCE pin must be held low during configuration, initialization, and user-mode. In a single-device configuration, the nCE pin needs to be tied low. In a multi-device configuration, nCE of the first device is tied low while its nCEO pin is connected to nCE of the next device in the chain.<br>The nCE pin must also be held low for successful JTAG programming of the device. |

**Table 10–22.** Dedicated Configuration Pins on the Cyclone III Device (Part 3 of 5)

| Pin Name | User Mode | Configuration Scheme | Pin Type | Description |
|---|---|---|---|---|
| nCEO | N/A if option is on. I/O if option is off. | All | Output open drain | Output that drives low when Cyclone III device configuration is complete. In a single-device configuration, you can leave this pin floating or use it as a user I/O pin after configuration. In a multi-device configuration, this pin feeds the next device's nCE pin. The nCEO of the last device in the chain can be left floating or used as a user I/O pin after configuration.<br>If you use the nCEO pin to feed the next device's nCE pin, use an external 10-kΩ pull-up resistor to pull the nCEO pin high to the $V_{CCIO}$ voltage of its I/O bank to help the internal weak pull-up resistor.<br>If you use the nCEO pin as a user I/O pin after configuration, set the state of the pin in the **Dual-Purpose Pin** settings. |
| FLASH_nCE, nCSO | I/O | AS, AP | Output | Output control signal from the Cyclone III device to the serial configuration device in AS mode that enables the configuration device. The FLASH_nCE pin functions as the nCSO pin in AS mode.<br>Output control signal from the Cyclone III device to the parallel flash in AP mode that enables the flash. Connects to the CE# pin on the Numonyx P30 or P33 flash.<br>In AS or AP mode, FLASH_nCE has an internal pull-up resistor that is always active. |
| DCLK | N/A | PS, FPP, AS, AP | Input (PS, FPP). Output (AS, AP) | In PS and FPP configurations, DCLK is the clock input used to clock data from an external source into the target Cyclone III device. Data is latched into the device on the rising edge of DCLK.<br>In AS and AP modes, DCLK is an output from the Cyclone III device that provides timing for the configuration interface. In AS mode, DCLK has an internal pull-up resistor (typically 25 kΩ) that is always active.<br>After configuration, this pin is tri-stated. In schemes that use a configuration device, DCLK is driven low after configuration is complete. In schemes that use a control host, DCLK needs to be driven either high or low, whichever is more convenient. Toggling this pin after configuration does not affect the configured device. |

**Table 10–22.** Dedicated Configuration Pins on the Cyclone III Device (Part 4 of 5)

| Pin Name | User Mode | Configuration Scheme | Pin Type | Description |
|---|---|---|---|---|
| DATA[0] | I/O | PS, FPP, AS, AP | Input (PS, FPP, AS). Bidirectional (AP) | Data input. In serial configuration modes, bit-wide configuration data is presented to the target Cyclone III device on the DATA[0] pin.<br>In AS mode, DATA[0] has an internal pull-up resistor that is always active. After AS configuration, DATA[0] is a dedicated input pin with optional user control.<br>After PS or FPP configuration, DATA[0] is available as a user I/O pin and the state of this pin depends on the **Dual-Purpose Pin** settings.<br>After AP configuration, DATA[0] is a dedicated bidirectional pin with optional user control. |
| DATA[1], ASDO | I/O | FPP, AS, AP | Input (FPP). Output (AS). Bidirectional (AP) | Data input in non-AS mode. Byte-wide or word-wide configuration data is presented to the target Cyclone III device on DATA[7..0] or DATA[15..0], respectively.<br>Control signal from the Cyclone III device to the serial configuration device in AS mode used to read out configuration data. The DATA[1] pin functions as the ASDO pin in AS mode.<br>In AS mode, DATA[1] has an internal pull-up resistor that is always active. After AS configuration, DATA[1] is a dedicated output pin with optional user control.<br>In the PS configuration scheme, DATA[1] functions as a user I/O pin during configuration, which means it is tri-stated.<br>After FPP configuration, DATA[1] is available as a user I/O pin and the state of this pin depends on the **Dual-Purpose Pin** settings.<br>After AP configuration, DATA[1] is a dedicated bidirectional pin with optional user control. |
| DATA[7..2] | I/O | FPP, AP | Inputs (FPP). Bidirectional (AP) | Data inputs. Byte-wide or word-wide configuration data is presented to the target Cyclone III device on DATA[7..0] or DATA[15..0], respectively.<br>In the AS or PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated.<br>After FPP configuration, DATA[7..2] are available as user I/O pins and the state of these pin depends on the **Dual-Purpose Pin** settings.<br>After AP configuration, DATA[7..2] are dedicated bidirectional pins with optional user control. |

**Table 10–22.** Dedicated Configuration Pins on the Cyclone III Device (Part 5 of 5)

| Pin Name | User Mode | Configuration Scheme | Pin Type | Description |
|---|---|---|---|---|
| DATA[15..8] | I/O | AP | Bidirectional | Data inputs. Word-wide configuration data is presented to the target Cyclone III device on DATA[15..0].<br>In the PS, FPP, or AS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated.<br>After AP configuration, DATA[15:8] are dedicated bidirectional pins with optional user control. |
| PADD[23..0] | I/O | AP | Output | 24-bit address bus from the Cyclone III device to the parallel flash in AP mode. Connects to the A[24:1] bus on the Numonyx P30 or P33 flash. |
| nRESET | I/O | AP | Output | Active-low reset output. Driving the nRESET pin low resets the parallel flash. Connects to the RST# pin on the Numonyx P30 or P33 flash. |
| nAVD | I/O | AP | Output | Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that valid address is present on the PADD[23..0] address bus. Connects to the ADV# pin on the Numonyx P30 or P33 flash. |
| nOE | I/O | AP | Output | Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[15..0]). Connects to the OE# pin on the Numonyx P30 or P33 flash. |
| nWE | I/O | AP | Output | Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[15..0] bus is valid. Connects to the WE# pin on the Numonyx P30 or P33 flash. |

Table 10–23 describes the optional configuration pins. If these optional configuration pins are not enabled in the Quartus II software, they are available as general-purpose user I/O pins. Therefore, during configuration, these pins function as user I/O pins and are tri-stated with weak pull-up resistors.

**Table 10–23.** Optional Configuration Pins

| Pin Name | User Mode | Pin Type | Description |
|---|---|---|---|
| CLKUSR | N/A if option is on. I/O if option is off. | Input | Optional user-supplied clock input synchronizes the initialization of one or more devices. This pin is enabled by turning on the **Enable user-supplied start-up clock** (**CLKUSR**) option in the Quartus II software. |
| INIT_DONE | N/A if option is on. I/O if option is off. | Output open-drain | Status pin can be used to indicate when the device has initialized and is in user-mode. When nCONFIG is low and during the beginning of configuration, the INIT_DONE pin is tri-stated and pulled high due to an external 10-kΩ pull-up resistor. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and pulled high and the device enters user mode. Thus, the monitoring circuitry must be able to detect a low-to-high transition. This pin is enabled by turning on the **Enable INIT_DONE output** option in the Quartus II software.<br>The functionality of this pin changes if the **Enable OCT_DONE** option is enabled in the Quartus II software. This option controls whether the INIT_DONE signal is gated by the OCT_DONE signal, which indicates the Power-Up OCT calibration is completed. If this option is turned off, the INIT_DONE signal is not gated by the OCT_DONE signal. |
| DEV_OE | N/A if option is on. I/O if option is off. | Input | Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as programmed. This pin is enabled by turning on the **Enable device-wide output enable** (**DEV_OE**) option in the Quartus II software. |
| DEV_CLRn | N/A if option is on. I/O if option is off. | Input | Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. This pin is enabled by turning on the **Enable device-wide reset** (**DEV_CLRn**) option in the Quartus II software. |

Table 10–24 describes the dedicated JTAG pins. JTAG pins must be kept stable before and during configuration to prevent accidental loading of JTAG instructions. TDI and TMS have weak internal pull-up resistors, while TCK has a weak internal pull-down resistor. If you plan to use the SignalTap® II Embedded Logic Array Analyzer, you need to connect the JTAG pins of the Cyclone III device to a JTAG header on your board.

**Table 10–24.** Dedicated JTAG Pins

| Pin Name | User Mode | Pin Type | Description |
|---|---|---|---|
| TDI | N/A | Input | Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK. The TDI pin is powered by the $V_{CCIO}$ supply.<br>If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to $V_{CC}$. |
| TDO | N/A | Output | Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device. The TDO pin is powered by $V_{CCIO}$ in I/O bank 1. For recommendations on connecting a JTAG chain with multiple voltages across the devices in the chain, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing* chapter in volume 1 of the *Cyclone III Device Handbook*.<br>If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by leaving this pin unconnected. |
| TMS | N/A | Input | Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur on the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. The TMS pin is powered by the $V_{CCIO}$ supply.<br>If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to $V_{CC}$. |
| TCK | N/A | Input | The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge. The TCK pin is powered by the $V_{CCIO}$ supply.<br>If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting TCK to GND. |

# Conclusion

You can configure Cyclone III devices in a number of different schemes to fit your system's needs. In addition, configuration data decompression and remote system upgrade support supplement the Cyclone III configuration solution.

# Referenced Documents

This chapter references the following documents:

- *AN 370: Using the Serial FlashLoader with the Quartus II Software*
- *AN 386: Using the Parallel Flash Loader with the Quartus II Software*
- *AN 414: JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration*
- *AN 418: SRunner: An Embedded Solution for Serial Configuration Device Programming*
- *AN 423: Configuring the MicroBlaster Passive Serial Software Driver*
- *AN 425: Using Command-Line Jam STAPL Solution for Device Programming*
- *AN 523: Cyclone III Configuration Interface Guidelines with EPCS Devices*
- *ByteBlaster II Download Cable User Guide*
- *ByteBlasterMV Download Cable User Guide*
- *Configuring Mixed Altera FPGA Chains* in volume 2 of the *Configuration Handbook*

- *DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*
- *Debugging Configuration Problems* chapter in volume 2 of the *Configuration Handbook*
- *Hot Socketing and Power-On Reset* chapter in volume 1 of the *Cyclone III Device Handbook*
- *IEEE 1149.1 (JTAG) Boundary-Scan Testing* chapter in volume 1 of the *Cyclone III Device Handbook*
- *MasterBlaster Serial/USB Communications Cable User Guide*
- *PCN 0514 Manufacturing Changes on EPCS Family*
- *Remote System Upgrade* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Serial Configuration Devices (EPCS1, EPCS4, EPCS16, EPCS64, and EPCS128) Data Sheet* chapter in volume 2 of the *Configuration Handbook*
- *Software Settings* section in volume 2 of the *Configuration Handbook*
- *USB-Blaster Download Cable User Guide*

# Document Revision History

Table 10–25 shows the revision history for this chapter.

**Table 10–25.** Document Revision History (Part 1 of 4)

| Date and Document Version | Changes Made | Summary of Changes |
|---|---|---|
| October 2008 v2.1 | ■ Updated "Configuration Schemes" section<br>■ Updated Table 10–1, Table 10–4, Table 10–5, Table 10–10, Table 10–11, Table 10–12, Table 10–13, Table 10–14, Table 10–15, and Table 10–22<br>■ Updated "Single-Device AS Configuration" section<br>■ Updated "AP Configuration Supported Flash Memories" section<br>■ Updated "Single-Device AS Configuration" section<br>■ Updated Figure 10–8 and *(Note 4)*<br>■ Updated "Single-Device AP Configuration" section<br>■ Updated Figure 10–9 and *(Note 5)*<br>■ Updated Figure 10–10 and *(Note 5)*<br>■ Updated Figure 10–11 and *(Note 4)*<br>■ Updated Figure 10–12<br>■ Updated "Estimating AP Configuration Time" section<br>■ Updated Figure 10–20<br>■ Revised *(Note 3)* to Figure 10–24<br>■ Updated "Overriding the Internal Oscillator" section<br>■ Chapter updated to new template | ■ Removed Intel and replaced with Numonyx. |
| May 2008 v2.0 | ■ Updated Table 10–1 and *(Note 5)* and *(Note 9)* Also added new *(Note 12)* and *(Note 13)*<br>■ Updated Table 10–2 and *(Note 2)*<br>■ Updated Table 10–3<br>■ Updated Table 10–5 and added new *(Note 13)*<br>■ Updated Table 10–6 and *(Note 3)*, and added new *(Note 6)* and *(Note 7)*<br>■ Deleted Note 1 to Table 10–7<br>■ Updated Figure 10–4 and *(Note 2)* and added new *(Note 8)* | ■ Updated the uncompressed Raw Binary File sizes<br>■ Added information about the level shifter usage, which is not recommended for AS and AP configuration<br>■ Added information about AS configuration support at 3.0/2.5 V configuration voltage standard |

**Table 10–25.** Document Revision History (Part 2 of 4)

| Date and Document Version | Changes Made | Summary of Changes |
|---|---|---|
| May 2008<br>v2.0 | ■ Updated Figure 10–5 and *(Note 2)*, and added new *(Note 2)*<br>■ Updated Figure 10–6 and added new *(Note 7)*<br>■ Added new "Guidelines for Connecting Parallel Flash to Cyclone III for AP Interface" section and Table 10–8<br>■ Updated Figure 10–7<br>■ Updated Table 10–9 and *(Note 3)*, and added new *(Note 7)*<br>■ Updated Figure 10–8 and *(Note 4)*<br>■ Updated Figure 10–9 and *(Note 5)*<br>■ Updated Figure 10–10 and *(Note 2)* and *(Note 5)*<br>■ Added new "Guidelines for Connecting Parallel Flash to Cyclone III for AP Interface" section and Table 10–11<br>■ Updated Figure 10–11 and *(Note 4)*<br>■ Added new Figure 10–12<br>■ Updated *(Note 2)* to Figure 10–15<br>■ Updated Figure 10–17<br>■ Updated *(Note 2)* and added *(Note 5)* to Table 10–14<br>■ Updated *(Note 2)* to Figure 10–21<br>■ Updated Figure 10–23<br>■ Updated *(Note 2)* and *(Note 6)* to Figure 10–24<br>■ Updated *(Note 2)* to Figure 10–25<br>■ Updated Table 10–16<br>■ Updated *(Note 2)* to Figure 10–26<br>■ Updated *(Note 2)* to Figure 10–27<br>■ Updated *(Note 2)* to Figure 10–28<br>■ Updated "Configuring Cyclone III Devices with JRunner" section<br>■ Updated Figure 10–29 and *(Note 2)*<br>■ Updated Table 10–21 and added *(Note 1)*<br>■ Updated Table 10–22<br>■ Updated Table 10–23 | ■ Removed RDY pin and replaced with a normal I/O to monitor the WAIT signal<br>■ Added information about M164 Package<br>■ Added information about CRC ERROR pin that will support both dedicated output and open-drain<br>■ Updated the configuration timing waveform for FPP and PS schemes |

**Table 10–25.** Document Revision History (Part 3 of 4)

| Date and Document Version | Changes Made | Summary of Changes |
|---|---|---|
| July 2007<br>v1.1 | ■ Updated "Configuration Devices" section<br>■ Removed references to Spansion in Table 10–1, Table 10–4, Table 10–5, Table 10–9, Table 10–10, Table 10–22, "AP Configuration Supported Flash Memories", "Single-Device AP Configuration", and "Programming Parallel Flash Memories" sections<br>■ Changed $V_{CCIO}$ to $V_{CCA}$ for MSEL pin connection in "Configuration Schemes" section, in footnotes to Table 10–1, Figure 10–3, Figure 10–4, Figure 10–5, Figure 10–6, Figure 10–7, Figure 10–8, Figure 10–9, Figure 10–10, Figure 10–11, Figure 10–15, Figure 10–16, Figure 10–18, Figure 10–19, Figure 10–20, Figure 10–21, Figure 10–22, Figure 10–29, Figure 10–30, and in MSEL[3..0] row in Table 10–22<br>■ Updated "Configuration Schemes" section<br>■ Updated Table 10–6 with *(Note 5)*<br>■ Updated "Programming Serial Configuration Devices" section<br>■ Updated Figure 10–7<br>■ Updated Figure 10–8<br>■ Deleted version 1.0 Figure10-9<br>■ Updated Figure 10–9<br>■ Updated "Word-Wide Multi-Device AP Configuration" section<br>■ Updated Figure 10–10 and Figure 10–11<br>■ Updated "Programming Parallel Flash Memories" section<br>■ Updated Figure 10–13<br>■ Added *(Note 4)* to Table 10–12<br>■ Added *(Note 4)* to Table 10–14<br>■ Updated "JTAG Configuration" section<br>■ Added Figure 10–25 and Figure 10–27<br>■ Updated Figure 10–26<br>■ Updated "Configuring Cyclone III Devices with JRunner" section<br>■ Aded new "Programming Serial Configuration Devices In-System Using the JTAG Interface" section with Figure 10–30<br>■ Updated Table 10–19<br>■ Added chapter TOC and "Referenced Documents" section | ■ Removed support for Spansion S29WS-N flash memory<br>■ Added information about the default AP configuration boot address in Quartus II software<br>■ Added information about JTAG configuration. When using different $V_{CCIO}$ voltages, user must power up the download cable's $V_{CC}$ with the specific recommended voltage<br>■ Added information about programming serial configuration devices in-system using the JTAG interface (SFL approach)<br>■ Changed $V_{CCIO}$ to $V_{CCA}$ for MSEL pin connection<br>■ Removed support for Spansion S29WS-N flash memory<br>■ Added information about the default AP configuration boot address in Quartus II software<br>■ Added information about JTAG configuration. When using different $V_{CCIO}$ voltages, user must power up the download cable's $V_{CC}$ with the specific recommended voltage<br>■ Added information about programming serial configuration devices in-system using the JTAG interface (SFL approach)<br>■ Changed $V_{CCIO}$ to $V_{CCA}$ for MSEL pin connection |

**Table 10–25.** Document Revision History (Part 4 of 4)

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| March 2007 v1.0 | Initial release. | — |

101 Innovation Drive
San Jose, CA 95134
www.altera.com
Technical Support
www.altera.com/support