Homework 5: Theory of Operation and Hardware Design Narrative

Team Code Name: Drink Mixer_____ Group No. 2

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Evaluation:

SCORE	DESCRIPTION
10	***Excellent*** *– among the best papers submitted for this assignment. Very few corrections needed for version submitted in Final Report.*
9	***Very good*** *– all requirements aptly met. Minor additions/corrections needed for version submitted in Final Report.*
8	***Good*** *– all requirements considered and addressed. Several noteworthy additions/corrections needed for version submitted in Final Report.*
7	***Average*** *– all requirements basically met, but some revisions in content should be made for the version submitted in the Final Report.*
6	***Marginal*** *– all requirements met at a nominal level. Significant revisions in content should be made for the version submitted in the Final Report.*
*	***Below the passing threshold*** *– major revisions required to meet report requirements at a nominal level.* ***Revise and resubmit.***

** Resubmissions are due within **one week** of the date of return, and will be awarded a score of "6" provided all report requirements have been met at a nominal level.*

Comments:

1.0 Introduction

The Drink Mixer is an eight channel digital audio mixer with stereo master output as well as three auxiliary outputs. In order to accomplish this a significant amount of hardware is required. Not only are there components with a critical need of noise reduction, there are also motorized fader components requiring drivers and high current draw. In addition to these issues there is the added complexity contributed by the vast array of LEDs and rotary pulse encoders. All these systems must be able to communicate in order to adjust the various settings of the audio mixer.

2.0 Theory of Operation

The following sections will describe all the major subsections of the audio mixer and how they interact with each other.

Master Board Subsection

The master board is considered the brain of the system. This is where all the user interface information as well as incoming data is received and processed. For this reason the Hammer ARM9 is on this board as well as the SHARC ADSP-21262. These 2 chips connect out to the other subsections for their specific purposes. While the ARM9 is acquiring user interface data, the DSP is processing the incoming audio streams and sending them to the outputs. In order for the ARM9 to communicate to the DSP to notify it of processing changes the DSP runs in SPI slave mode and is told what to do by the ARM9 after it has finished processing any user interface changes. This separation of processes gives the benefit of maximizing the use of the features of the DSP and reducing any chances of user interface processing from slowing and possibly distorting audio output. The ARM9 will also be responsible for displaying user pertinent information on the LCD display and taking feedback from the touch screen.

Also on the main board are two ATMEGA32A micro-controllers. These are located here to control and monitor the master faders and effects faders for output control. These talk to the on board ARM9 via an I2C interface. This interface is also sent out over jumper pins to the four dual channel subsections described later.

As for audio data interaction the DSP has two I2S busses that are connected over jumpers to the analog processing subsection, which will be described later.

The last thing also placed on this board is the power regulator. All the power supply related circuits will be placed in a separate section on this board and power will be sent out to all the other subsection interfaces from here.

Dual Channel Interface Subsection

The dual channel interface subsection is used to handle motorized faders, LEDs, RPGs, and other user interface related parts. On each of these boards there are two ATMEGA32A micro-controllers. These micro-controllers each handle a channel. Each channel interface consists of a LED bar graph for displaying the control's estimated levels as well as an RPG for adjusting parameters and the motor-driven fader. Each fader requires an H-bridge in order to be interfaced with the Atmel. There are a total of four of these subsections in the design and all communicate with the Main Board over an I2C data bus. Through the I2C bus each ATMEGA32A will be able to get instructions about where to move faders to as well as update the ARM9 with changes.

Analog Processing Subsection

The Analog processing subsection is where all the analog audio inputs are processed and digitized as well as where the outputs are processed and converted to analog. In order for this to happen each channel must have its own balanced preamplifier circuit. This circuit consists of a modified custom design [1] using JFET transistors as the inputs. The high impedance input as well as low noise are the two reasons for the JFET usage. Package mounted female XLR connectors will feed these input channels.

For every two channels there exists a dual input A/D converter. This means there will be a total of four of these in this subsection. These are Analog Devices AD1871 analog to digital converters. All of these will be configured to run in TDM mode for the DSP as well as a daisy chained SPI. This means that the command sets can be sent into them like a daisy chain / shift register. This SPI interface is used to initialize and configure the A/D converters. This SPI bus will interface to the ARM9, which will take on the task of configuring the A/D converters at power on. These A/D converters then use an I2S bus in TDM mode to send data back to the main board subsection.

Also on the board are the AD1852 24-bit D/A converters. These will be used to convert the digital output signals to an analog output. These in turn will be sent to basic pre-out

amplifiers to balance the signal for master output. These receive their data and are initialized over the same interface as the A/D converters with the main subsection.

3.0 Hardware Design Narrative

Main Board Subsection ARM9

The main interfaces used on the Hammer ARM9 are a combination of SPI interfacing, as well as I2C interfacing. It is also important to note that the video out support of the Hammer ARM9 will be fully utilized to drive an 8-bit color display.

As far as the I2C bus is concerned the SDA and SCL pins are sent to a bidirectional level shifting circuit. This is due to the 3.3V board operation and the ATMEGA processors running at 5V. This I2C bus will be used to receive updated interface information as well as send updates to the individual channel interface microcontrollers.

The Hammer ARM9 we are currently using has two SPI ports. Both of these devices can potentially be used but the primary SPI bus (SPI0) pins will be used to initialize the A/D converters, D/A converters, as well as communicate with the DSP. The other SPI module on the chip may or may not be used to interface with a SD Card.

In this design, the TX0 and RX0 pins will be utilized and routed to a level shifter for RS232 communication. This is the primary means for programming and debugging the Hammer.

Main Board Subsection DSP SHARC ADSP-21262

The Analog Devices SHARC digital signal processor has the primary task of processing data input and sending it back out to the D/A. This processor has four TDM mode serial interfaces. In the design only two out of these four will be needed and turned on accordingly. The other system worth mentioning is the slave mode pin that will have to be tied high so that the SHARC knows to operate its SPI interface in slave mode. This will allow the Hammer ARM9 to dish out commands to the DSP. The rest of the pins will be used for general purpose I/O to show the amplitude variations with 40 LEDs.

Individual Channel ATMEGA32A

The ATMEGA32A micro-controller, as mentioned earlier, will be used to control most of the user interface switches. This will involve the ATD0 pin enabled as an analog to digital

converter to monitor the fader value. Also two PWMs will have to be used to operate the H-bridge for the motor.

The last important pins to mention are the TWI (I2C) pins. These pins will have to be set up to operate in slave mode and switch to master mode upon an addressing call from the Hammer ARM9. The rest of the pins will be utilized as GPIO for reasons such as monitoring an RPG and displaying readouts on a LED bar graph.

Summary

In this report theories of operation as well as hardware narratives were discussed. Information regarding the individual hardware subsections of the device as well as the pin configurations on the microcontrollers was explained and discussed.

List of References

[1] P. Allison and R. Elliot, "Low Noise Balanced Microphone Preamp," May 17, 2008. [Online], Available: **http://sound.westhost.com/project66.htm**. [Accessed: Sept 29, 2009].

Appendix A: System Block Diagram