Homework 6: Printed Circuit Board Layout Design

Due: Friday, February 24, at NOON

Team Code Name: __RFID Xpr3ss_____ **Group No.** __10__

Team Member Completing This Homework: __Jared Suttles_____

NOTE: This is the third in a series of four "design component" homework assignments, each of which is to be completed by one team member. The completed homework will count for 10% of the team member's individual grade. The report itself should be a minimum of five pages, **not** including the cover sheet, references, or any of the attachments (statistics report). **Electronically submit the ".MAX" PCB layout file along with the ".doc" version of this report zipped into one file.**

Evaluation:

Component/Criterion	Score	Multiplier	Points
Introduction & Layout Considerations	0 1 2 3 4 5 6 7 8 9 10	X 3	
Documentation for PCB Layout Design	0 1 2 3 4 5 6 7 8 9 10	X 5	
List of References	0 1 2 3 4 5 6 7 8 9 10	X 1	
Technical Writing Style	0 1 2 3 4 5 6 7 8 9 10	X 1	
		TOTAL	

Comments:

1.0 Introduction

The RFID Xpr3ss self-checkout system is an attempt at integrating two innovative technologies in order to increase both retail efficiency and customer experience. It aims to allow a smooth and easy transition from using UPC barcodes to using RFID tags in retail transactions. The RFID Xpr3ss incorporates an RFID reader and an intuitive user interface to make the system both functional and customer friendly.

Self-checkout lanes and RFID technology are both growing in popularity, and the integration of the two is only a matter of time. Because of the prevalence of UPC technology, the design of the RFID Xpr3ss system is convenient for easy implementation, or to be used as a bolt-on upgrade to existing systems. Hence, the PCB layout is very important to its functionality. There were many considerations that needed to be made for the RFID Xpr3ss PCB, which will be discussed in the following pages.

2.0 PCB Layout Design Considerations

RFID Reader / Antenna

One of the most important design considerations in a project utilizing RFID technology is the placement of the RFID reader in relation to the other signals. Placing the antenna and transmitter too close to sensitive components could cause interference and result in unexpected circuit operation. This is not a concern in the design, due to the fact that the RFID reader and antenna are not built into the circuit, but rather exist in a separate housing connected by a three foot RS232 cable to a DB9 connector attached to the PCB [1].

Oscillator / PLL Circuits

An important analog component in the design is the crystal oscillator, which inherently must be placed close to the microcontroller. Not only must it also have short traces, but in order to provide the correct clock rate for the 100 Mbps Ethernet communication, the crystal must be connected in a Pierce configuration to the XTAL and EXTAL pins of the microcontroller [2]. It is also strongly recommended that, when using the Ethernet capabilities of the MC9S12NE64 microcontroller, the PLL circuits and filter capacitors must be configured in accordance with the data sheet diagrams [2]. The RFID Xpr3ss circuit was designed to match these circuits exactly.

Ethernet Circuit

The Ethernet circuitry also has a few more considerations to be taken into account. The microcontroller can be configured by software to provide LED signals that detail the status of the Ethernet communication. This design chooses to use two of those signals, link and activity, to drive LEDs mounted on the RJ45 jack. Another requirement is that the magnetics module needed for the Ethernet communication be placed as close as possible to the RJ45 jack; specifically, it must be less than one inch away from it. This is inherently achieved since the Molex HyperJack chosen for the design has the magnetics built into the jack [3]. This particular RJ45 module also satisfies the requirement that the magnetics module use a 1:1 turn ratio for both the receive and transmit lines. In order to ensure stability and reliability of the Ethernet communication, 12 mil traces and spacing are used, and 1% precision components will be used in the circuitry [2][4].

Power Supply

Another point of concern in the design was the power supply design. Because of the power dissipation and mixed voltage levels, the power supply is set away from the rest of the circuitry. Each part will generate a lot of heat, and hence will need to be given ample room to dissipate. There are copper pours beneath the tabs of the two TI REG1117 voltage regulators in the SOT-223 surface mount package. These will act as simple heat sinks to help draw out the heat generated in the voltage regulation [5].

The TI MC34063A Switching Regulator also requires some considerations to be taken into account. First, there are two relatively large inductors involved with the circuit, which must be placed apart from one another so that their mutual inductance doesn't affect the circuit. They are also part of the motivation to place the entire power circuit away from everything else because of their magnetic characteristics, which might otherwise cause interference [6].

The final power consideration was given to the LCD inverter which uses a large step up converter to provide the high voltage required to power the LCD backlight. This could cause interference if placed close to any sensitive circuits, and hence is located at the top of the PCB, away from any sensitive circuits [7].

Microcontroller

Many considerations also need to be made for the microcontroller part of the design. First, the MC9S12NE64 80-pin package has a small flag exposed on the underside of the chip. This is designed for heat dissipation, and while this application is not processing intensive, and heat will likely not be a problem, a copper pour was place beneath the chip as dictated by the data sheet [2].

The microcontroller also has many power pins which need to be bypassed with capacitors so as to provide an instantaneous current source during transitions. It is very important that these capacitors be close to their associated pins, so most of them are placed on the bottom side of the board. The data sheet also mentioned the importance of providing the central power and ground to the VDDA and VSSA pins at the "top" of the chip. Hence, those pins are connected to the main 3.3 V and ground rails. Finally, the area beneath the capacitors associated with the PLL and oscillator circuits was recommended to be left open and free of traces [2].

General Considerations

There were also many considerations taken into account in general when routing the PCB. Overall size was not a major design constraint, but compactness was a definite goal, both for functionality and cost practicality reasons. Hence, all design blocks are arranged around the central processor in order to save space. In order to make the use of the design more flexible, all of the external interfaces were also placed on one side of the board so that the board can be mounted on any face of the packaging.

Signal traces were routed with 12 mil copper to decrease line inductance and improve signal reliability, and 45 degree angles were used at all times. Main power and ground traces were routed with 60 mil copper to help drive their inherently longer nets. Because of the large number of surface mount parts used, a larger number of vias was unavoidable, but this condition also allowed for many parts to be mounted on the bottom side of the board to conserve space. Also whenever possible, power and ground traces were routed next to each other in order to decrease line noise [8].

In order to account for future modifications to the circuit design, a header was placed on the unused G port. This allows for 7 spare I/O pins that can be programmed later in development. Although the IRQ and XIRQ pins are not currently implemented, they are also

routed to headers so as to make them available for future implementation or design changes. Also, rather than leave unused input pins floating on the board, they are routed through 10 kΩ SIP resistors and tied to ground.

3.0 Summary

The RFID Xpr3ss system has many PCB considerations that have been taken into account. Because the size of the board was not a design constraint, care was taken to place critical parts in good positions, such as bypass capacitors near their associated power pins. Signals were routed using minimal trace lengths and no acute angles. The Ethernet and oscillator circuitry were configured exactly as documented in the data sheet so as to guarantee optimal performance and reliability [2]. The power supply circuitry is placed away from the other digital components so as to avoid any possible interference.

These considerations help to insure maximum performance from the RFID Xpr3ss system. The RFID Xpr3ss is a product that could truly revolutionize the retail industry on a customer experience level, and thus it must be both reliable and highly functional. This design will achieve both of these goals easily.

List of References

[1] Intersoft Corp WM-RO-MR2 Medium Range RFID Reader
http://www.intersoft-us.com/dnload/WMROMR2.pdf

[2] Freescale MC9S12NE64 Microcontroller
http://www.freescale.com/files/microcontrollers/doc/data_sheet/MC9S12NE64V1.pdf

[3] Molex HyperJack Modular RJ45 Jack with Integrated Magnetics and LED
http://www.molex.com/pdm_docs/sd/480250002_sd.pdf

[4] Motorola Application Note AN2759
http://www.freescale.com/files/microcontrollers/doc/app_note/AN2759.pdf

[5] Texas Instruments REG1117 LDO Positive Voltage Regulator
http://focus.ti.com/lit/ds/symlink/reg1117.pdf

[6] Texas Instruments MC34063A Switching Regulator
http://focus.ti.com/lit/ds/symlink/mc34063a.pdf

[7] CrystalFontz CFAICCFL1 Inverter for Backlit Graphic Modules
http://www.crystalfontz.com/products/240128d/CFAICCFL1.pdf

[8] Motorola Application Note AN1259
http://www.freescale.com/files/microcontrollers/doc/app_note/AN1259.pdf

Appendix A: Routing Statistics Report

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*                                       *
* STATISTICS REPORT                     *
*                                       *
* Y:\ORCAD\ORCAD2.5\SENIORDESIGN-14.MAX  *
* Fri Feb 24 02:03:06 2006              *
*                                       *
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STATISTIC	ENABLED	TOTAL
Board Area	27.4	27.4
Equivalent IC's	26.7	26.7
Sq. inches per IC	1.02	1.02
# of pins	401	401
Layers	4	28
Design Rule Errors	0	0
Time Used	20:14	20:14
% Placed	100.00%	100.00%
Placed	74	74
Off board	0	0
Unplaced	0	0
Clustered	0	0
Routed	246	246
% Routed	100.00%	100.00%
Unrouted	0	0
% Unrouted	0.00%	0.00%
Partials	0	0
% Partials	0.00%	0.00%
Vias	108	108
Test Points	0	0
Vias per Conn	0.44	0.44
Segments	1144	1144
Connections	246	246
Nets	128	128
Components	74	74
Footprints	193	193
Padstacks	85	85
Obstacles	555	555

Theoretical Dist	191.7	191.7
Routed Dist	183.4	183.4
Unrouted Dist	0.2	0.2