Fault Tolerant Approaches to Nanoelectronic Programmable Logic Arrays

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Overview

- Motivation
- Contributions
- Fault Models
- Fault tolerant approaches

Motivation

- Small scale of fabrication process =>
  - Large number of manufacturing defects
  - High occurrences of online faults
  - Expensive top down fabrication process
- New implications:
  - Regularity in structure
  - Online reconfigurability

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Contributions

- Two hardware redundancy based fault tolerant approaches:
  - Online fault diagnosis scheme
  - Fault masking scheme
- Categories of online fault tolerance

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Fault tolerance approaches

- Online repair base scheme
  - Online fault detection
  - Online diagnosis phase
  - Reconfiguration based repair
- Cons: Delay introduced
- Fault masking scheme
  - Known approach is: N-modular redundancy scheme (NMR)

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Fault Model for PLA

- Four types of faults

type	K-map	cause	effect	output	example
G	growth	missing device in AND plane	missing variable	$0 \rightarrow 1$	$f = ab + cd \rightarrow b + cd$
S	shrink	extra device in AND plane	extra variable	$1 \rightarrow 0$	$f = ab + cd \rightarrow abe + cd$
D	disap-pearance	missing device in OR plane	missing product term	$1 \rightarrow 0$	$f = ab + cd \rightarrow cd$
A	appear-ance	extra device in OR plane	extra product term	$0 \rightarrow 1$	$f = ab + cd \rightarrow ab + cd + e$

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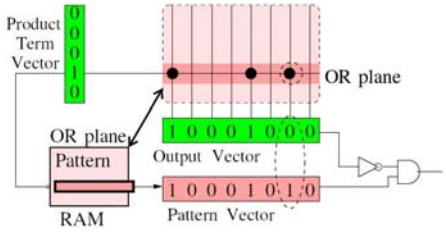
Online diagnosis for nano-PLAs

- Basic idea:
  - Offline vs Online diagnosis
- Information required to identify a fault online –
  - Input Vector(IV): Inputs to PLA's AND plane
  - Product Term Vector(PTV): Outputs of AND plane and inputs to OR plane
  - Output Vector(OV): Outputs of the PLA's OR plane.
- A RAM for each AND and OR plane.

An example

- A D type [missing device in OR plane] error occurs iff:
- P th product term wire has a value 1
- O th output wire shows 0
- The device connecting P th product term and O th output wire is configured as "on" in the fault free PLA.



Online diagnosis conditions

- General diagnosis conditions for 4 types of faults

fault type	fault location	occurring plane	C_1: input to the plane	fault effect	C_2: output of the plane	device crosspoint	C_3: configuration bit from RAM
G	$[i][p]$	AND	$IV[i]=0$	$0\rightarrow 1$	$PTV[p]=1$	miss	$R_{AND}[i][p]=1$
S	$[i][p]$	AND	$IV[i]=0$	$1\rightarrow 0$	$PTV[p]=0$	extra	$R_{AND}[i][p]=0$
D	$[p][o]$	OR	$PTV[p]=1$	$1\rightarrow 0$	$OV[o]=0$	miss	$R_{OR}[p][o]=1$
A	$[p][o]$	OR	$PTV[p]=1$	$0\rightarrow 1$	$OV[o]=1$	extra	$R_{OR}[p][o]=0$

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To identify a fault,
We need to look at C_1 and C_2 and C_3 columns

Online fault diagnosis algorithm

- Diagnosis for AND plane faults:
- For every bit position i in IV (Input Vector) , if IV [i] = 0: //*Diagnosis for AND plane faults*
- (a) PV = R_{AND}[i] //*Read Pattern Vector (*PV *) from the* i*'th column of RAM* R_{AND}
- (b) For every bit p that (PV [p] = 1; PTV [p] = 1), identify a G type fault at location [i][p]
- (c) For every bit p that (PV [p] = 0; PTV [p] = 0), identify an S type fault at location [i][p]

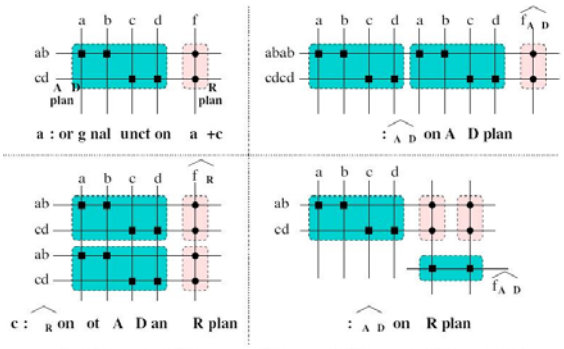
- Diagnosis for OR plane faults:
- For every bit position p in PTV (Product Term Vector), if PTV [p] = 1:
- (a) PV = ROR[p] //*Read Pattern Vector (*PV *) from the* p*'th row of RAM* R_{OR}
- (b) For every bit o that (PV [o] = 1;OV [o] = 0), identify a D type fault at location [p][o]
- (c) For every bit o that (PV [o] = 0;OV [o] = 1), identify an A type fault at location [p][o]

Fault Masking in nano-PLA

- Logic tautology form

$f_{AND} = f \cdot f = f$
$f_{OR} = f + f = f$

Basic Idea:
-Redundancy integrated within logic function



Fault	(a)	(b)	(c)	(d)
G type: missing device @ AND plane		✓		
S type: extra device @ AND plane			✓	
D type: missing device @ OR plane			✓	
A type: extra device @ OR plane				✓

Figure: Fault Masking example

Continue..

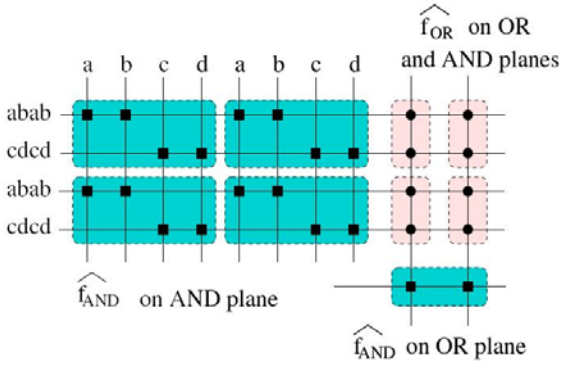


Figure: An example of tautology based PLA that can mask all 4 types of faults

Comparison of Fault masking schemes

- Original 2 level PLA has:
  - P x I AND plane
  - P x O OR plane
  - Da = P x I and Do = P x O
- Proposed 3 level PLA scheme has:
  - 2P x 2I AND plane
  - 2P x 2O OR plane
  - Extra level of AND logic: 2O number of devices and O wires.
  - Overall: 4Da + 4Do + 2O devices
- TMR is a majority voting fault masking algorithm having 4 levels:
  - Overall: 3Da + 3Do + 9O devices

Cont..

- Proposed scheme vs TMR:
  - Redundancy in logic vs voting hardware
  - Compatible with any nano-PLA implementation vs large area of wiring for voting structure

Conclusion

- Online fault diagnosis scheme
  - precisely identify location of error
  - Introduces delay
- Fault masking scheme
  - Generates correct output
  - Susceptible to multiple faults
- Just a framework for online fault tolerance approaches