Wafer-recyclable, environment-friendly transfer printing for large-scale thin-film nanoelectronics

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Transfer printing of thin-film nanoelectronics from their fabrication wafer commonly requires chemical etching on the sacrifice of wafer but is also limited by defects with a low yield. Here, we introduce a wafer-recyclable, environment-friendly transfer printing process that enables the wafer-scale separation of high-performance thin-film nanoelectronics from their fabrication wafer in a defect-free manner that enables multiple reuses of the wafer. The interfacial delamination is enabled through a controllable cracking phenomenon in a water environment at room temperature. The physically liberated thin-film nanoelectronics can be then pasted onto arbitrary places of interest, thereby endowing the particular surface with desirable add-on electronic features. Systematic experimental, theoretical, and computational studies reveal the underlying mechanics mechanism and guide manufacturability for the transfer printing process in terms of scalability, controllability, and reproducibility.

transfer printing method | thin-film nanoelectronics | Internet of Things | delamination | nondestructive wafer recycling

Thin-film nanoelectronics that can offer performances beyond traditional bulk systems but on diverse substrates or surfaces in lightweight, low-cost, transparent, and/or flexible forms could enable many emerging applications. Example devices include flexible complementary metal oxide semiconductor (CMOS) systems, multifunctional nanosensors and optoelectronics, and high-speed nanowire circuits (1–8). Conventional transfer printing methods that utilize either epitaxial lift-off (9–13) or controlled spalling (14–18) serve as mainstream strategies, enabling the physical separation of single-crystalline semiconducting nanomaterials (e.g., Si, Ge, GaAs, InAs, etc.) from their native substrate. The separated semiconducting nanomaterials are first printed onto a range of foreign substrates including polyurethanes, polyimides, and silicone elastomers, followed by postfabrication steps to yield completed electronic circuits. These approaches have provided great achievements over the last decades, but the choice of foreign substrate remains limited by which the substrate materials must have a certain degree of thermal and chemical resistance to accommodate the conditions for postfabrication process. Alternative strategies that involve a chemical etching of a thin sacrificial layer such as silicon dioxide (SiO_2) and poly(methyl methacrylate) (PMMA) allow the physical separation of fully fabricated thin-film nanoelectronics from their fabrication wafer in a deterministic manner (19–23). Although this methodology can eliminate the need of postfabrication, the chemical etching process of a sandwiched thin sacrificial layer is often challenged, especially for large-scale applications, by a long immersion of the devices in the etchant solution where the embedded electronic components and substrate/superstrate materials are properly protected from degradation or deformation. In these schemes, the fabrication wafer is often consumed and cannot be recycled. Recently, we demonstrated a proof of concept of water-assisted transfer printing process that involves a single mechanical peeling of a metallic separation layer (i.e., Ni) and a careful treatment on surface wettability in a manipulated environment (24–27), but the performances of the resulting thin-film electronics remain limited by exclusive use of the directly deposited amorphous or polycrystalline Si thin films as the active element. Transfer printing of thin-film integrated circuits that could support various combinations of single-crystalline semiconducting nanomaterials through a wafer-scale batch process has not been explored yet.

Here, we show a complementary transfer printing process that includes a series of key transferring steps: (*i*) The first step is to define various combinations of dissimilar forms and compositions of single-crystalline semiconducting nanomaterials on desired locations of a SiO_2/Si wafer in a single device layout, followed by conventional CMOS fabrication processes to yield a completed electronic circuits on the wafer. (*ii*) The second transferring step is to physically separate the entire layer of the completed thin-film nanoelectronics from the fabrication SiO_2/Si wafer in a defect-free manner that allows the fabrication wafer to be recycled for the next fabrication cycles. The physically liberated thin-film nanoelectronics can be then pasted onto an arbitrary kind of supporting substrates or surfaces. Both experimental and computational studies provide a route to understand underlying mechanism of the transfer printing process and therefore achieve necessary manufacturability in terms of scalability, controllability, and

Significance

The ability to endow the surface of existing objects with desired electronic features enables many emerging applications such as Internet of Things (IoT). Despite significant progress in the optimization of thin-film materials and construction schemes, the realization of high-performance thin-film electronics on arbitrary place through a wafer-scale batch process is limited. This paper presents a wafer-recyclable, environment-friendly transfer printing process that enables the physical delivery of large-scale thin-film integrated circuits with various combinations of active nanomaterials from their fabrication wafer to nearly any kind of places. Detailed experimental and theoretical studies reveal the essential attributes of this approach. Demonstrations in electronics and sensors realized on the surface of commercial appliances to meet the user-specific needs illustrate the utility.

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reproducibility. Demonstrations of these schemes in various representative nanoelectronics and nanosensors such as logic gates, switches, photodetectors, and environmental monitors that exhibit the electronic properties comparable to control counterpart devices illustrate the capability of this methodology.

Results

Transfer Printing Process. Device fabrication begins with depositing layers of Ni (300 nm) and diluted polyimide (D-PI) (a 1:1 mixture of 1-methyl-2-pyrrolidinone and polyimide, 300 nm) on a SiO_2/Si wafer to serve as a separation and glue layer, respectively (Fig. 1*A*, *Inset*). Conventional pick-and-place transfer printing approaches allow the delivery of epitaxial-grown single-crystalline semiconducting nanomaterials from their growth substrates to the D-PI layer in a spatial layout that matches requirement (28–30). As model systems, various forms and compositions of dissimilar nanomaterials are used in this report, including 2D Si nanomembranes (Si NMs) and molybdenum disulfide (MoS_2) monolayer, 1D Si nanoribbons (Si NRs) and silver nanowires (Ag NWs), and/or their heterogeneous integrations in a single circuit layout (*SI Appendix*, Fig. S1). Depositing other necessary thin-film materials for the conducting/insulating/encapsulating layers and patterning them by photolithography yield completed electronic circuits on the SiO_2/Si wafer (Fig. 1*A*, *Left* image). Herein, these materials and steps include atomic layer deposition (ALD) of aluminum oxide (Al_2O_3, 20 nm) for gate and dielectrics, plasma-enhanced chemical vapor deposition (PECVD) of SiO_2 (100 nm) for insulating layer, electron-beam (e-beam) evaporator of chromium/gold (Cr/Au) (10 nm/300 nm) for source, drain, gate contacts, and interconnect pads, and spin-casting of D-PI for adhesive and encapsulation layer. Details about the synthesis and fabrication procedures appear in *Materials and Methods*.

The next step involves attaching a temporary handling holder such as thermally releasable tape (Nitto Denko) on top and gently peeling it in distilled (DI) water at room temperature, which allows the bottom Ni film to be cleanly delaminated from the SiO_2/Si wafer (Fig. 1*A*, *Middle* image). A demonstration showing the interfacial debonding of a 4-inch wafer-size test bed sample in a water bath appears in Movie S1. The delaminated Ni film can either remain to serve as a functional layer (i.e., back reflecting layer for solar cells, back gate electrode for transistors, etc.) or be removed at this stage by briefly soaking in a mixture solution of etchant (TFB; Transene) for ∼2 min at room temperature. Any unnecessary part such as corner spaces or align markers of the delaminated structure can be trimmed by using commercial scissors (Fig. 1*A*, *Right* image). The resulting structure can be then pasted onto a desired place of interest with a commercial adhesive such as silicone glues, spray adhesives, or tapes. Removing the temporary handling holder from the surface finishes the entire transfer printing process.

Fig. 1*B* presents representative optical images of the test bed sample (here, multiple stacked layers of D-PI/Si NMs and Si NRs/SiO_2/Cu/Au) at the each key step during the transfer printing process, with their magnified views in the bottom frame. The representative microscope images appear in *SI Appendix*, Fig. S2. These optical inspections confirm that there is no induction of visible damage or defect during/after the interfacial debonding process in water. This aspect allows the donor Si wafer to be recycled multiple times with proper postcleaning treatments (*SI Appendix*, Fig. S3), which can serve as an additional cost-saving factor in the manufacturing scheme. As an example demonstration, the test bed sample was pasted onto the surface of a building window (*SI Appendix*, Fig. S4), wherein the transferred electronics were concealed by covering them with a commercial sticker in the interest of providing better appearance

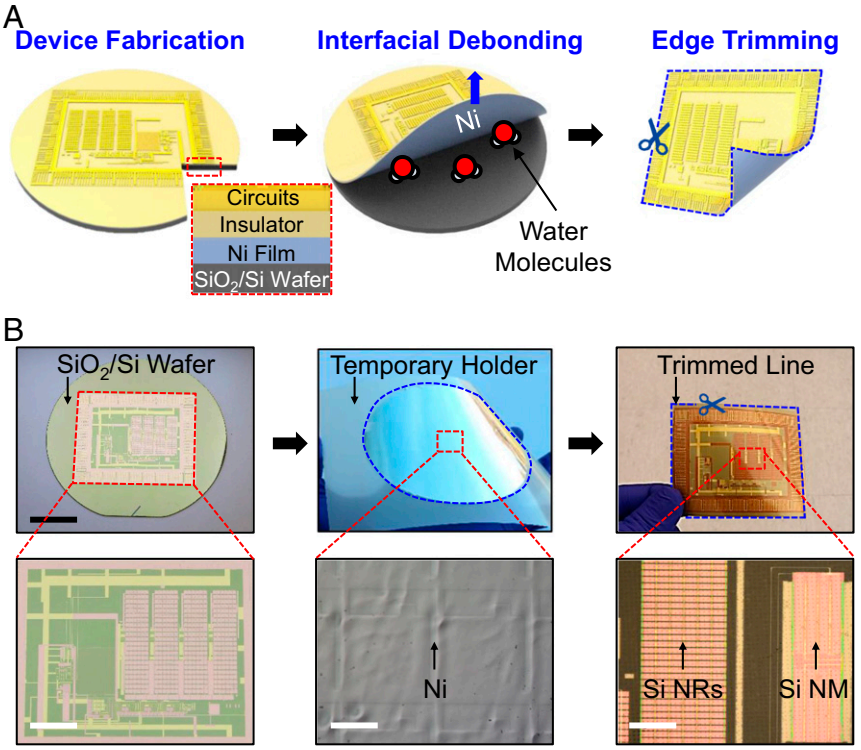

Fig. 1. (*A*) Schematic illustrations of key steps for physically liberating a thin-film nanoelectronics from its fabrication SiO_2/Si wafer in water. The *Inset* shows a cross-sectional illustration. (*B*) Optical images of the thin-film nanoelectronics on the SiO_2/Si wafer (*Left*), and peeled with a thermally releasable tape (*Middle*), and then trimmed neatly (*Right*). (Scale bar: 2.5 cm.) The *Bottom* frame shows the corresponding microscope images. (Scale bars: 1 cm, 400 μm, and 300 μm, respectively.)

of final products. When the process was conducted in dry air condition (20% relative humidity) for comparisons, mechanical damage or unwanted delamination of thin films (i.e., torn apart) was occasionally observed in the areas that have weak intrinsic interfacial adhesions (*SI Appendix*, Fig. S5).

Mechanism Study and Mechanics Analysis. The working principle of the interfacial debonding process in liquid water is underpinned by strong coupling of the elasto-plastic deformation of adherent thin films and the molecular reactions of liquid and solid at the interface. Fig. 2*A* shows an experimental setup equipped with a high resolution of force gauge that is designed for thin-film mechanical peeling experiments, with the enlarged view in *SI Appendix*, Fig. S6. Fig. 2*B* provides experimental and finite-element analysis (FEA) results of a peeling strength–peeling distance (p–d) curve, obtained by mechanical peeling of a simplified thin-film nanoelectronics architecture (here, the Ni/D-PI/Si NM) in water (blue color) and dry air condition (20% relative humidity; red color) at room temperature. Details about the measurement setup appear in *Materials and Methods*. The results indicate consistent agreement, where the p increases quickly at the beginning until reaching a maximum for initiating interfacial debonding, and then gradually decreases until it eventually becomes constant for a steady debonding process. The results also reveal that the p is largely decreased by ~80% in the peak regime in water (~14 J/m^2) by comparison with that in air (~79 J/m^2), indicating that the presence of water promotes the interfacial debonding. In addition, the magnified view in the *Inset* image presents that the steady-state peeling strength (p_{ss}) in water (~2.3 J/m^2) is also decreased by ~60% compared to that in air (~5.3 J/m^2), which confirms that the water environment leads to the reduction of interfacial energy required to delaminate the thin films.

Fig. 2*C* presents experimental, computational (FEA), and theoretical results that reveal the effect of peeling angle (α) on p_{ss}. The corresponding p–d curves for Fig. 2*C* appear in *SI Appendix*, Fig. S7*A*. These results indicate that p_{ss} decreases with the increase of α, which is attributed to increased dissipation of energy in bending thin films from the substrate, similar to that in dry air conditions (31). The thickness of Ni layer (t) is a critical parameter due to its role in spreading the induced stress uniformly

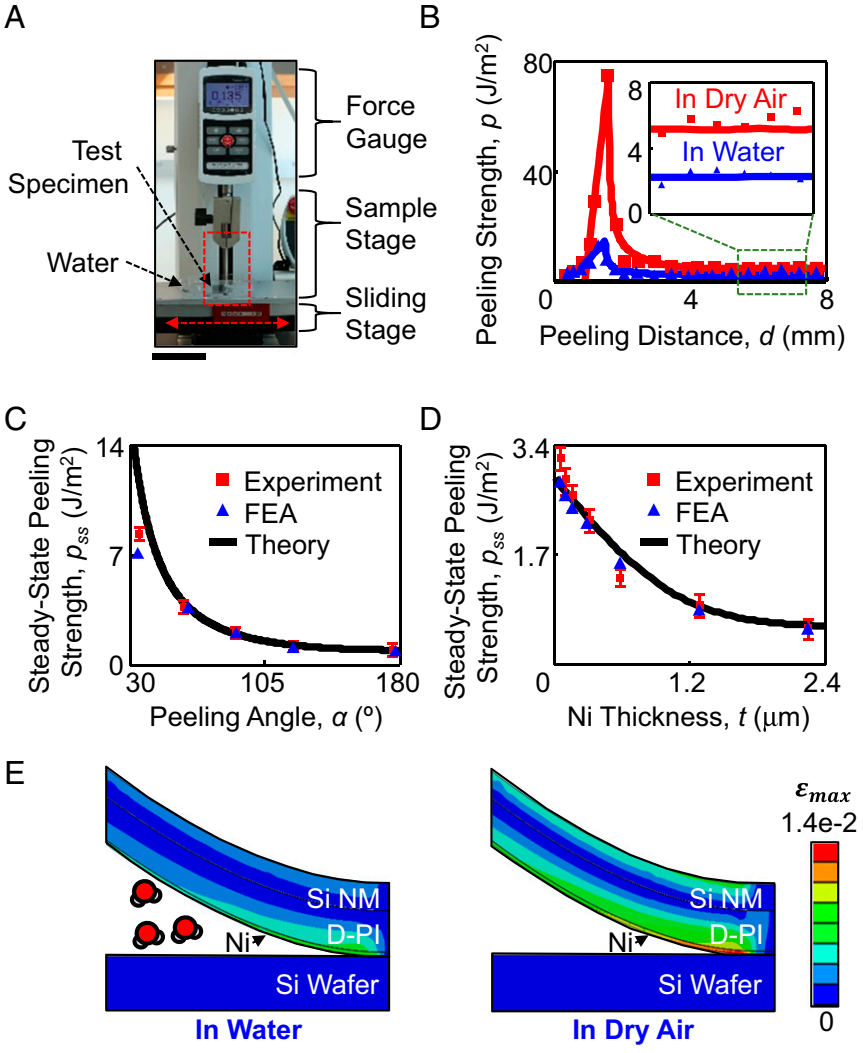

Fig. 2. (*A*) An optical image of a custom-modified mechanical peeling apparatus. (Scale bar: 6 cm.) (*B*) Experimental (dots) and finite-element analysis (FEA, lines) results of peeling strength as a function of peeling distance in water and dry air conditions. The *Inset* shows a magnified view of the peeling strength–distance curves at steady-state stage. (*C*) Experimental, FEA, and theoretical results of the steady-state peeling strength in water with varied peeling angles from 30° to 180°. (*D*) Experimental, FEA, and theoretical data of steady-state peeling strength in water with varied Ni thickness from 30 nm to 2.4 μm. (*E*) FEA results of maximum principal strain distributions in the thin films under mechanical peeling in water (*Left*) and dry air conditions (*Right*).

along the layer during the water-assisted interfacial debonding process, thereby facilitating to avoid plastic deformation of thin films. Fig. 2*D* shows the relationship between p_{ss} and t in water environment at the given $\alpha \sim 90°$. The corresponding p–d curves for Fig. 2*D* appear in *SI Appendix*, Fig. S7*B*. The results show that the p decreases monotonously as the t increases due to the reduced deformation energy. When the t is large enough, ~2.4 μm, the effect of plastic deformation can be negligible where the p_{ss} becomes independent of t and equal to the adhesion energy at the debonding interface. For these cases, the experimental (red rectangular dots), FEA (blue triangular dots), and theoretical (black line) results are in a good agreement to support the findings. The peeling rate (r) during these measurements remains at or slower than a certain threshold value due to the fact that the p_{ss} increases exponentially when the r becomes larger than $\sim 2 \times 10^{-3}$ m/s (*SI Appendix*, Fig. S8).

Fig. 2*E* presents strain distribution (ε) of thin films under the interfacial debonding process with (*Left* image) and without (*Right* image) the presence of water. The modeled thin films consist of multiple stacked layers of Ni (300 nm)/D-PI (300 nm)/Si NM (200 nm) with the mechanical modulus (E) of 200, 2.5, and 130 GPa, respectively. Details about the computational method appear in *Materials and Methods*. The results show that the maximum principal strain (ε_{max}) exists in the Ni film where the magnitude in water is about 40% smaller than that in dry air condition. This aspect causes the most fragile material such as Si NM to experience insignificant mechanical constraints during the interfacial debonding process in water and therefore prevent mechanical failure, as consistent with the experimental observations described above. For example, the peak strain at the Si NM when peeled in water was about 0.4%, which is far below its fracture limit (~1%) (32). In contrast, when peeled in dry air condition, the peak strain at the Si NM was about 0.9%, which is expected to yield potential mechanical damages. The corresponding strain distributions at peeling distance (d) of 1 to ~11 mm for both in water and dry air condition, and with varied Ni thickness (t) of 30 nm to ~2.4 μm in water appear in *SI Appendix*, Figs. S9 and S10.

The knowledge gained from these studies provides important insights to identify the optimal operational conditions for reliable interfacial debonding process with high fidelity. A custom-modified setup by exploiting an automated peeling apparatus illustrates a demonstrative example, showing the capability to provide high-precision motions with controlled parameters in the peeling force, rate, and angle (Movie S2). The yield for defect-free interfacial debonding was 98.26% among >200 test bed samples. The failures mostly occurred along a certain edge area of the wafer (*SI Appendix*, Fig. S11) that includes inadvertently deposited residues (D-PI, SiO_2, etc.), which could be eliminated by careful removal of the residues before the interfacial debonding process.

Component-Level Validation of Transferred Thin-Film Nanoelectronics. Fig. 3*A* shows representative microscopy images of the component level of thin-film nanoelectronics, including an array of resistors (*Left* image), diodes (*Middle* image), and transistors (*Right* image), each of which is transferred from its fabrication SiO_2/Si wafer to a piece of glass. The test bed samples are composed of dissimilar kinds of single-crystalline inorganic nanomaterials including Ag NWs, p-i-n–doped Si NRs, and n-doped Si NM to serve as the active element. Details about the fabrication procedures appear in *Materials and Methods*. Fig. 3*B* presents the measured current–voltage (I–V) curves obtained from these test bed samples before

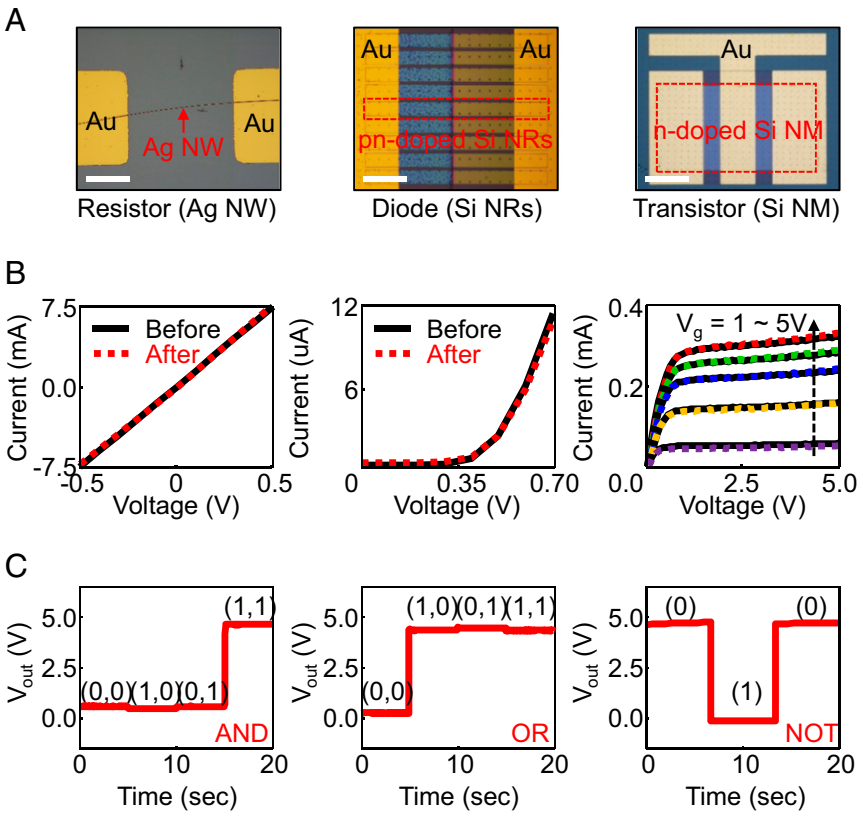

Fig. 3. (*A*) Microscope images showing the transferred Ag NW-based resistor (*Left*), Si NRs-based p-i-n diode (*Middle*), and Si NM-based transistor (*Right*) on a piece of glass, each of which is transferred from its fabrication SiO_2/Si wafer. (Scale bars: 40, 200, and 250 μm, respectively.) (*B*) Corresponding electrical characteristics to the each device before and after the transfer printing process. (*C*) Output voltage characteristics of AND (*Left*), OR (*Middle*), and NOT (*Right*) logic gates with V_{in} = 5 V.

(black lines) and after (colored dots) the transfer printing process: the Ag NW-based resistor showed the resistance of ~73 Ω; the Si NRs-based diode showed the diode quality factor (n) of ~2.2 with applied voltage at ~0.4 V; the Si NM-based transistor showed the linear mobility of ~76 $cm^2/v{\cdot}s$. The corresponding transfer curves to those of Fig. 3*B*, *Right* appear in *SI Appendix*, Fig. S12. The electrical characteristics were remained nearly identical before and after the transfer printing process, implying that no degradation occurred in the electronic performances. The overall electrical properties of these electronic components can be improved by optimizing the doping process and device architecture (20).

To confirm the functionality, the test bed samples were assembled into a range of logic gates such as AND, OR, and NOT gates (Fig. 3*C*), where the corresponding circuit diagram to each logic gate appears in *SI Appendix*, Fig. S13. The resulting logic gates perform well in a manner that can modulate the output state (V_{out}) depending on the on/off state of each input signal ($V_{in} \sim 5$ V): the AND gate provides a high V_{out} only if both V_{in1} and V_{in2} are high; the OR gate provides a high V_{out} if either V_{in} is high; the NOT gate provides an inverted version of V_{in} at its output. This demonstration suggests that further integrations of these kinds of thin-film nanoelectronics into the practices are possible with the transfer printing process. To further illustrate the possibility, several examples of system-level demonstrations are presented in the following sections.

System-Level Demonstrations of Transferred Thin-Film Nanoelectronics. An interesting aspect of this transfer printing process arises from its unique ability that can easily define various shapes of final products to suit desired appearance. Fig. 4*A* presents an experimental demonstration by using a 4-inch wafer size of thin-film nanoelectronics that is peeled from the fabrication SiO_2/Si wafer with a thermally releasable tape (Fig. 4*A*, *Left*) and then trimmed into desired shapes, and finally pasted to fit onto the intrinsic shapes of target substrates such as commercial wooden blocks (Toys"R"Us) as an example (Fig. 4*A*, *Right*). In this particular demonstration, the test bed samples are composed of multiple stacked layers of D-PI/n-doped Si NMs/Al_2O_3/Cr/Au to function as capacitors in which the embedded single-crystalline Si NMs serve as the active semiconducting element. Fig. 4*B* shows representative electrical characteristics of an embedded capacitor where the average capacitance of 60 capacitors in a single device layer was 250 ± 40 pF. This demonstration highlights the key feature of this approach, which is capable of installing single-crystalline level of thin-film nanoelectronics on arbitrary shapes of objects with desired fits.

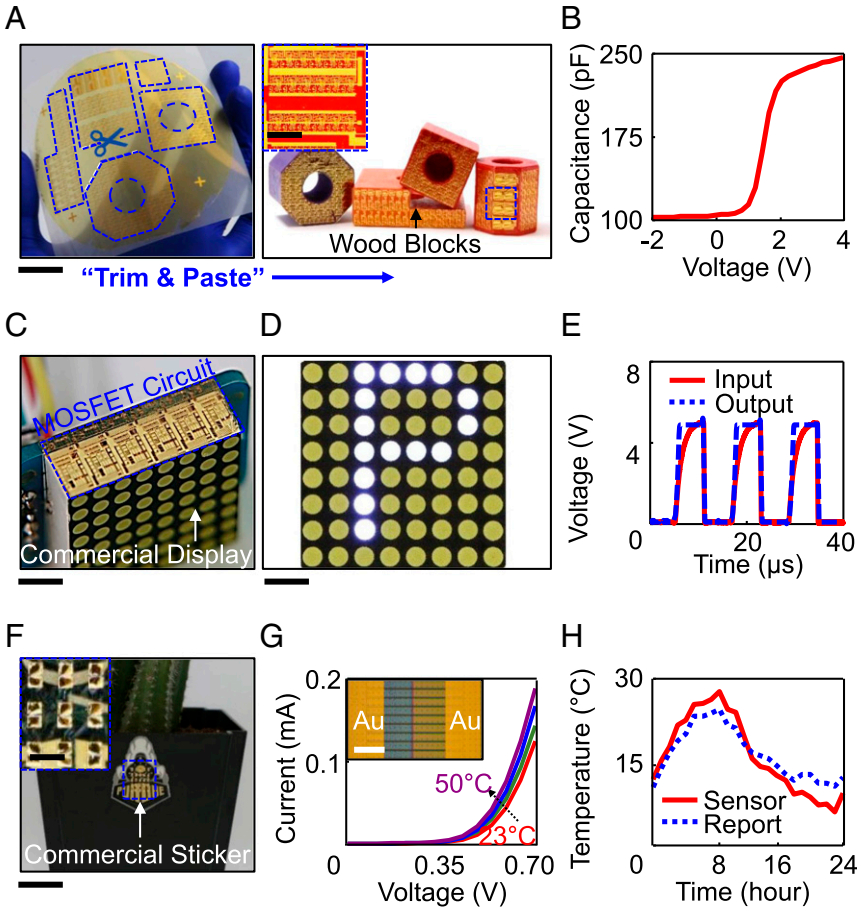

Fig. 4. (*A*) Optical images of arrays of n-doped Si NM-based thin-film capacitors on a thermally releasable tape (*Left*) and after pasted on the surface of commercial wooden blocks with right fits (*Right*). (Scale bar: 2 cm.) The *Inset* shows a magnified view of the transferred devices. (*B*) Electrical characteristics of a representative capacitor in the arrays. (Scale bar: 2 mm.) (*C*) Optical image of arrays of n-doped Si NM-based MOSFETs pasted on the side wall of a commercial LED display. (Scale bar: 6 mm.) (*D*) Screen-captured image of the displayed letter "P." (Scale bar: 4 mm.) (*E*) Measured clock signals switched by the transferred n-MOSFETs. (*F*) Optical image of arrays of pn-doped Si NRs-based temperature sensors pasted on the surface of a commercial flowerpot with a commercial sticker. (Scale bar: 2 cm.) The *Inset* shows a magnified view of the transferred sensor arrays. (Scale bar: 2 mm.) (*G*) Electrical characteristics of the Si NRs-based sensors with varied temperature ranging from 23 to 50 °C with a hot plate. The *Inset* shows an optical microscope image of the embedded Si NRs. (Scale bar: 150 μm.) (*H*) Measured environmental temperature obtained from the Si NRs-based sensor and a local weather report over a period of 24 h.

More system-level demonstrations that have generic relevance to envisioned applications, such as Internet of Things (IoT), are followed to validate the utility of the transfer printing process. Fig. 4*C* presents an example system that includes an array of n-doped Si NM-based metal–oxide–semiconductor field-effect transistors (n-MOSFETs) that is pasted on the side wall of a commercial light-emitting diode (LED) display (8 × 8 pixel; Luckylight) with an excellent fit. In this circuit configuration, the embedded n-MOSFETs serve as functional switches that can control LED lights to display digital letters and images on the screen in a preprogrammed manner (Movie S3). Fig. 4*D* shows a screen-captured image of an alphabet "P" from the recorded video. Representative clock signals switched by the transferred n-MOSFETs appear in Fig. 4*E*, with the corresponding *I*–*V* and transfer curves shown in *SI Appendix*, Fig. S14.

Fig. 4*F* presents another system-level demonstration by exploiting arrays of p-i-n–doped Si NR-based diodes that are pasted on the side wall of a flowerpot with a commercial sticker. In this circuit configuration, the embedded p-i-n junction diodes serve as the active semiconducting element that is capable of detecting the change of temperature (33, 34). Fig. 4*G* presents representative *I*–*V* curves of a p-i-n junction diode as a function of temperature ranging from 23 to 50 °C, externally controlled by a hot plate. The *Inset* image shows a magnified view of the embedded p-i-n–doped Si NRs with a pair of Cr/Au contact pads for the electrical measurements. The use of single-crystalline Si NRs enables the measurement of environmental temperature with a level of fidelity that is comparable to that obtained using a conventional infrared (IR) sensor (*SI Appendix*, Fig. S15*A*). The corresponding calibration curves appear in *SI Appendix*, Fig. S15*B*, clearly displaying the linear dependence of the p-i-n junction diode on temperature. Fig. 4*H* presents a demonstration of the measured environmental temperature over a period of 24 h by using the transferred Si NR-based sensor (red line), which is matched well to that from a local weather report (blue dotted line).

Integration of Heterojunction Photodiode Nanosystem. The ability to integrate dissimilar classes of 2D semiconducting nanomaterials into a single device platform provides benefits to many existing and emerging heterojunction hybrid nanoelectronics including multifunctional optoelectronic devices, biomolecular detectors, superconductors, and hyperspectral imaging (35–38). To demonstrate the utility of the transfer printing process in this scheme, a hybrid photodiode nanosystem that combines

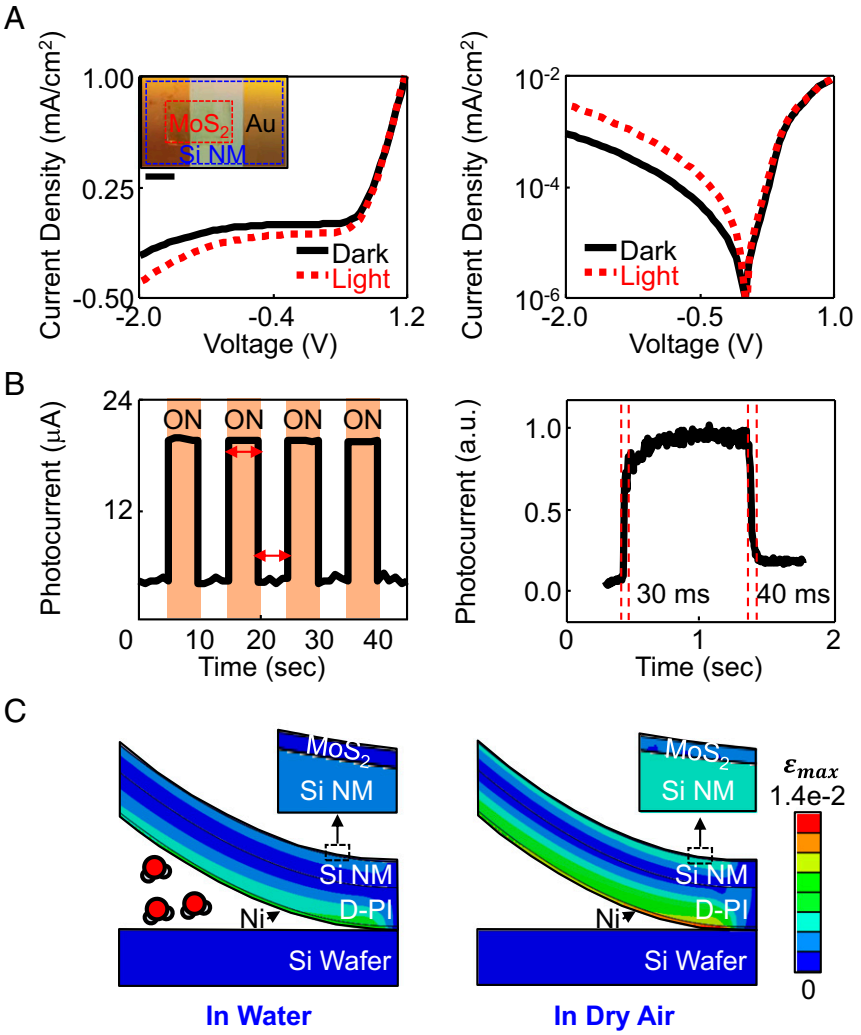

Fig. 5. (*A*) Linear (*Left*) and logarithmic (*Right*) expression of current density–voltage (*J*–*V*) characteristics of a hybrid photodiode system that combines p-doped Si NM and n-doped MoS_2 under dark and light conditions. The *Inset* shows a top view of the hybrid photodiode nanosystem. (Scale bar: 3 mm.) (*B*) Time-dependent on/off photoresponse in multiple (*Left*) and single (*Right*) light stimulation with external bias voltage of −2 V. (*C*) FEA results of maximum principle strain distributions in the thin films under mechanical peeling in water (*Left*) and dry air conditions (*Right*).

p-doped Si NM (~1 cm wide and ~200 nm thick) and n-doped MoS_2 monolayer (~5 mm wide and ~4 nm thick) in a vertically stacked layout is constructed on a piece of glass as a model system. The hybrid integration platform facilitates to overcome the impediment in the application of MoS_2 in photodiode systems due to the lack of high-quality p-n junction and low-light absorption (39). The synthesis of MoS_2 monolayer occurs by the use of a traditional chemical vapor deposition (CVD) method (40), and the representative Raman spectroscopy image in *SI Appendix*, Fig. S16 indicates that the characteristic peaks of E^1_{2g} and A_{1g} appear at 383 and 403 cm^{-1}, respectively. Details about the synthesis and fabrication procedures appear in the *Materials and Methods* section.

Fig. 5*A* shows linear (*Left*) and logarithmic (*Right*) expressions of current density–voltage (*J*–*V*) curves of the hybrid photodiode under conditions of darkness (black lines) and illumination (red dotted lines) by 540-nm laser with a light intensity at 3 μW/cm^2. The *Inset* optical image shows the top view of a representative test bed sample, with the corresponding schematic illustration shown in *SI Appendix*, Fig. S17. These results indicate that, at forward bias, the current densities for both dark and illumination conditions have barely any difference, whereas a clear distinction exists at reverse bias at the photocurrent (I_{ph}) of ~33 μA. Fig. 5*B* presents photoresponse of the hybrid photodiode, displaying abrupt rise and fall in the photocurrent with 540-nm laser. The test bed sample exhibited its external quantum efficiency of ~16%, light responsivity of 2.67 A/W for 540 nm at −2-V bias, detectability of $\sim 3.31 \times 10^{11}$, time responses of 30 and 40 ms at the rise and fall edges, and I_{on}/I_{off} ratio of ~210 at the external bias voltage of −2 V. These electrical characteristics were almost identical compared with those of control samples prepared on a SiO_2/Si wafer (*SI Appendix*, Fig. S18). In addition, the overall performances are comparable to those reported in previous reports (41, 42), confirming that the established heterojunction between Si NM and MoS_2 remains intact during/after the transfer printing process. The computational (FEA) results in Fig. 5*C* identify that the constituent nanomaterials including both Si NM and MoS_2 experience insignificant mechanical strains under the mechanical debonding process in water. For instance, the peak strain at MoS_2 monolayer was about 0.2% when peeled in water, which was approximately two times smaller than that in dry condition (~0.4%). The strain distributions for the thin films at peeling distance (d) of 1 to ~11 mm in water appear in *SI Appendix*, Fig. S19.

Discussion

The transfer printing process reported herein implies several important consequences: First, this process provides the ability to integrate various combinations of nanomaterials into thin-film nanoelectronics on a donor Si wafer, and then physically transfer onto nearly any kind of place to endow the target surface with desired electronic functionalities. Second, this process is versatile to generate diverse shapes of the thin-film nanoelectronics tailored to fit onto a specific target surface, thereby providing a route that can modulate the physical appearance and aesthetics of final products. Last, this process is fully driven by a fundamental understanding of the underlying chemomechanics mechanisms in a water environment and proves to be reliable for multiple recycles of the donor Si wafer in a defect-free manner, significantly reducing the manufacturing cost. These features overcome several difficulties of conventional transfer printing approaches that rely on chemicals with consumption of growth or native substrates such as Si wafer and can be particularly useful for many emerging applications such as IoT wherein the implementation of these kinds of high-performance thin-film nanoelectronics on arbitrary places or objects would become important. Further applications of this transfer printing process for flexible and stretchable thin-film electronics would be potentially enabled by incorporating several advanced mechanics designs into circuit layouts (43–45).

Materials and Methods

FEA Method. The modeling of the interfacial debonding process for multilayer-stacked thin films from a SiO_2/Si wafer was performed by using the ABAQUS/standard package. The material deformation was modeled by linear elastic behavior with the mechanical modulus (E) and the Poisson's ratio (v) for Si, E = 130 GPa and v = 0.27, for D-PI, E = 2.5 GPa and v = 0.34, and for MoS_2, E = 330 GPa and v = 0.125, and for Ni film, it was modeled by elastic-perfectly plastic behavior, and E = 200 GPa, v = 0.31, and yield stress σ_y = 400 MPa. A mesh convergence study was conducted in advance to confirm the discretization of model sufficient enough for extracting converged steady-state peeling force. The adhesive bonding at the interface between Ni film and SiO_2/Si wafer was modeled using the cohesive zone model. In the cohesive zone model, it is described by a trilinear traction–separation relation, and the fracture energy (G_c) is defined as the area of the traction–separation curve. A constant displacement loading rate was applied on one edge of thin films when peeled from the bottom fixed SiO_2/Si substrate at a given peeling angle (α).

Theoretical Modeling. Considering a quasistatic peeling process, the energy balance can be expressed as follows:

$$W_P = W_{\text{adhesion}} + W_{\text{plastic}}, \quad [1]$$

where $W_P (= P \cdot b \cdot (1 - \cos\alpha) \cdot \Delta l)$ is the work done by peeling force. P is the steady-state peeling strength, which is defined as the peel-off force per unit width, b is the width of thin film, α is the peeling angle, and Δl is the peeling length. $W_{\text{adhesion}} (= G \cdot b \cdot \Delta l)$ is the total adhesion energy of interface between thin film and substrate. G is the adhesion energy per unit area at the interface. $W_{\text{plastic}} (= Q \cdot b \cdot \Delta l)$ is the plastic work dissipation of thin film. As a consequence, Eq. **1** becomes the following:

$$P(1 - \cos\alpha) = G + Q. \quad [2]$$

At the steady-state debonding process, the internal plastic work of the thin film can be expressed as follows (46):

$$Q = \int_l M(K) dK, \quad [3]$$

where M and K are the local bending moment and curvature, respectively, and l is the curvature path. The bending moment–curvature relationship can be obtained via $M(K) = -\int_{-(T/2)}^{-(T/2)+t_{Ni}} \sigma\{\varepsilon\} \cdot y \cdot dy = -\int_{-(T/2)}^{-(T/2)+t_{Ni}} \sigma\{-Ky\} \cdot y \cdot dy$, where T is the total thickness of the thin films, t_{Ni} is the thickness of Ni film, y is the local coordinate in the tangent direction, and $\sigma\{\varepsilon\}$ is the local normal stress. During the peeling process, the thin films experience elastic bending, elasto-plastic bending, and unloading bending deformation, as illustrated in *SI Appendix*, Fig. S20. Considering an elastic-perfectly plastic behavior for these bending deformation, the bending moment at each local position of the thin films can be obtained. Defining E and σ_y as the Young's modulus and yield stress of Ni film, respectively, at $0 \le K \le 2\sigma_y/ET$, the local thin films (OA position) are in elastic deformation and the bending moment can be expressed as follows:

$$M_1(K) = -\int_{-\frac{T}{2}}^{-\frac{T}{2}+t_{Ni}} E(-Ky) y dy = \frac{EK}{12}\left(4{t_{Ni}}^3 - 6T{t_{Ni}}^2 + 3T^2 t_{Ni}\right). \quad [4]$$

At $2\sigma_y/ET < K < K_{max}$, the plastic deformation happens at local AB position, where $K_{\max}$ is the maximum curvature in the peeled films and can be obtained from the equilibrium conditions. As a consequence, the corresponding bending moment is as follows:

$$M_2(K) = -\int_{-\frac{T}{2}}^{-\frac{\sigma_y}{EK}} \sigma_y y dy - \int_{-\frac{\sigma_y}{EK}}^{-\frac{T}{2}+t_{Ni}} E(-Ky) y dy$$

$$= \frac{EK}{24}\left(8{t_{Ni}}^3 - 12T{t_{Ni}}^2 + 6T^2 t_{Ni} - T^3\right) - \frac{\sigma_y^3}{6E^2K^2} + \frac{\sigma_y T^2}{8}. \quad [5]$$

Beyond the $K_{\max}$, the unloading elastic deformation in the peeled films occurs, and at $K_{\max} - 4\sigma_y/ET \le K \le K_{\max}$, the bending moment at BC position of thin films can be calculated as follows:

$$M_3(K) = -\int_{-\frac{T}{2}}^{-\frac{\sigma_y}{EK_{\max}}} \left[\sigma_y - E(-K_{\max}y + Ky)\right] y dy - \int_{-\frac{\sigma_y}{EK_{\max}}}^{-\frac{T}{2}+t_{Ni}} E(-Ky) y dy$$

$$= \frac{EK}{12}\left(4{t_{Ni}}^3 - 6T{t_{Ni}}^2 + 3T^2 t_{Ni}\right) - \frac{EK_{\max}}{24}T^3 + \frac{\sigma_y}{8}T^2 - \frac{{\sigma_y}^3}{6E^2{K_{\max}}^2}. \quad [6]$$

Furthermore, at $0 \le K \le K_{\max} - 4\sigma_y/ET$, the moment of reverse plastic bending at CD position of thin films can be calculated as follows:

$$M_4(K) = -\int_{-\frac{T}{2}}^{-\frac{2\sigma_y}{E(K_{\max}-K)}} \sigma_y y dy - \int_{-\frac{2\sigma_y}{E(K_{\max}-K)}}^{-\frac{\sigma_y}{EK_{\max}}} \left[\sigma_y - E(-K_{\max}y + Ky)\right] y dy$$

$$- \int_{-\frac{\sigma_y}{EK_{\max}}}^{-\frac{T}{2}+t_{Ni}} E(-Ky) y dy = \frac{EK}{24}\left(8{t_{Ni}}^3 - 12T{t_{Ni}}^2 + 6T^2 t_{Ni} - T^3\right)$$

$$- \frac{8{\sigma_y}^3}{3E^2(K_{\max}-K)^2} + \frac{\sigma_y}{8}T^2 - \frac{{\sigma_y}^3}{6E^2{K_{\max}}^2}. \quad [7]$$

Therefore, based on Eqs. **3–7**, the expression of plastic work per unit area in the peeled thin films can be determined as follows:

$$Q = \int_0^{\frac{2\sigma_y}{ET}} M_1(K)dK + \int_{\frac{2\sigma_y}{ET}}^{K_{\max}} M_2(K)dK + \int_{K_{\max}-\frac{4\sigma_y}{ET}}^{K_{\max}} M_3(K)dK$$

$$+ \int_0^{K_{\max}-\frac{4\sigma_y}{ET}} M_4(K)dK = \frac{EK_{\max}{}^2}{3}{t_{Ni}}^3 - \frac{EK_{max}{}^2 T}{2}{t_{Ni}}^2 + \frac{EK_{max}{}^2 T^2}{4}t_{Ni}$$

$$- \frac{EK_{\max}{}^2 T^3}{24} + \frac{\sigma_y K_{\max} T^2}{4} - \frac{5{\sigma_y}^2 T}{4E}. \quad [8]$$

With Eqs. **2** and **8**, the peel-off strength can be expressed as follows:

$$P = \frac{G}{(1-\cos\alpha)} + \frac{1}{(1-\cos\alpha)}\left(\frac{EK_{\max}{}^2}{3}{t_{Ni}}^3 - \frac{EK_{\max}{}^2 T}{2}{t_{Ni}}^2\right.$$

$$\left. + \frac{EK_{\max}{}^2 T^2}{4}t_{Ni} - \frac{EK_{\max}{}^2 T^3}{24} + \frac{\sigma_y K_{\max} T^2}{4} - \frac{5{\sigma_y}^2 T}{4E}\right). \quad [9]$$

Note that when the plastic deformation of the thin films can be neglected, Eq. **9** can be reduced to the classical Kendall model $P = G/(1-\cos\alpha)$ (47).

Synthesis of Ag NWs. A conventional solution-based multistep growth mechanism was used for the synthesis of Ag NWs (48). The synthesis began with heating 50 mL of ethylene glycol (9356-09; J. T. Baker) at 150 °C for ∼1 h in an oil bath (CG-1100; Chemglass). The preheated ethylene glycol solution was mixed with 400 μL of copper(II) chloride ($CuCl_2$, 4 mM; Sigma-Aldrich) and 15 mL of polyvinylpyrrolidone (0.147 M; Sigma-Aldrich) in consecutive order with the time interval of 15 min. Constant injections of silver nitrate ($AgNO_3$, 15 mL, 0.094 M; Sigma-Aldrich) at a rate of 1 mL/min using a syringe pump (AL-4000; World Precision Instrument) initiated the growth of Ag NWs in the solution. Repeating these steps allowed the Ag NWs to be grown up to ∼250 μm in their maximum length. The synthesized Ag NWs can be stored in a solution of isopropanol (99.5%; Sigma-Aldrich) before the device fabrication.

Synthesis of MoS_2 Monolayer. A monolayer of 2H-MoS_2 was grown on a SiO_2/Si substrate using a tube furnace system (Lindberg/Blue M TF55030A; Thermo Scientific) loaded with two alumina boats that contained molybdenum trioxide (MoO_3) and sulfur (S) powders (40). During the synthesis, the alumina boats with MoO_3 and S powders were placed in the center and upstream of the tube furnace at the temperature of ∼750 and ∼200 °C, respectively. Argon (Ar) was used as the carrier gas to bring S vapor from upstream to the center of the tube furnace at 1 atm.

Characterization of Interfacial Debonding Process. The interfacial debonding process was characterized using a custom-modified mechanical peeling apparatus equipped with a high-resolution force gauge (Mark-10; resolution, ±0.25%). A thin layer of Ni film with thickness ranging from 30 nm to 2.4 μm was prepared on a SiO_2/Si wafer by using an e-beam evaporation or electroplating. A mixture of 1-methyl-2-pyrrolidinone (Sigma-Aldrich) and polyimide (PI) (Sigma-Aldrich) with 1:1 ratio was spin-casted onto the prepared Ni film, followed by a brief curing step at 110 °C for ∼20 s to evaporate the solvent. A piece of Si NM (1.5 × 1.5 cm, 200 nm) was delivered from silicon-on-insulator (SOI) wafer (SOITEC) to the surface of the D-PI using a polydimethylsiloxane stamp. An annealing step at 220 °C for 60 min was followed to ensure the bonding between the D-PI and Si NM. The prepared specimen was firmly attached on a plastic Petri dish with a double-sided tape (Kapton), and then laminated by a thermally releasable tape (Nitto Denko) across the top surface. The Petri dish was mounted on the horizontal stage of the automatic peeling apparatus, and ∼30 mL of DI water was poured to fill in the Petri dish. The thermally releasable tape was pulled at a predefined peeling angle and rate for the measurements. The measurements were averaged from total 60 test bed samples. Although more reactive environmental solutions such as methanol at elevated temperature would promote the interfacial delamination process (49), commercial DI water at room temperature was exclusively used in this study as the most cost-effective, safe, and readily available solution.

Fabrication of Ag NW-Based Resistor. The as-grown Ag NWs were dispersed on a spin-cast bilayer of Ni/D-PI on a SiO_2/Si wafer, followed by a curing step at 70 °C for ∼10 min to evaporate the solvent. A photolithographic patterning was used to define the source and drain regions on each end of Ag NW. Deposition of a bilayer of Cr/Au (10 nm/300 nm) using an e-beam evaporator followed by a conventional lift-off process enabled the formation of contact pads and interconnectors of the device. The interfacial debonding process reported here was then conducted in water to deliver the device layer to a receiver substrate.

Fabrication of Si NRs-Based Diode. The fabrication began with doping of SOI wafer (SOITEC) with spin-on-dopant for p-type (Boron, B153; Filmtronics) and n-type (Phosphorous, P509; Filmtronics). PECVD (Axic) of a thin layer of SiO_2 (800 nm) was used to form a diffusion mask for source and drain regions. Photolithographic patterning and wet etching by buffer oxide etchant (BOE) (1:6) were followed to expose the diffusion areas and annealed at 950 to ∼1,000 °C. The underlying buried oxide layer (SiO_2) was removed by soaking in concentrated hydrofluoric acid (HF) (49%) for ∼20 min, allowing the device Si layer to be released from the SOI wafer and then transferred onto a spin-cast bilayer of Ni/D-PI on a SiO_2/Si wafer. The doped Si NMs were patterned into multiple ribbons by reactive ion etching (RIE) (Plasmatech) with sulfur hexafluoride (SF_6). Thin layers of Cr/Au (10/300 nm) deposited with an e-beam evaporator were formed to serve as the source and drain electrodes as well as the interconnectors. The interfacial debonding process reported here was then conducted in water to deliver the device layer to a receiver substrate.

Fabrication of Si NM-Based Transistor. All of the fabrication procedures for doping and transfer of the Si NM were similar to those described for the Si NRs-based diodes. A Si NM (1.5 × 1.5 cm, 200 nm thick) was transferred on a spin-cast bilayer of Ni/D-PI on a SiO_2/Si wafer and then isolated by RIE (SF_6) to expose the active regions. A thin layer of Al_2O_3 (∼20 nm) deposited with ALD served as the gate dielectric. Other thin layers of Cr/Au (10 nm/300 nm) were formed to define the source, drain, and gate contact pads. The interfacial debonding process reported here was then conducted in water to deliver the device layer to a receiver substrate.

Fabrication of Logic Gate Circuits. All of the fabrication procedures for doping and transfer of the Si NM and Ag NWs were similar to those described for the Si NM-based transistor and the Ag NW-based resistor, respectively. A number of p-i-n–doped Si NRs-based diodes and Ag NW-based resistors (∼10 kΩ) were aligned across two different pairs of electrodes in predefined circuit configurations. A thin layer of D-PI layer (300 nm) was spin-casted on the top to encapsulate the device with contact openings formed by conventional photolithography and RIE etching process (O_2: 20 sccm, 50 mTorr, 150 W, 3 min). The interfacial debonding process reported here was then conducted in water to deliver the device layer to a receiver substrate.

Fabrication of Si NM-Based Capacitor. All of the fabrication procedures for the doping and patterning of n-doped Si NM is similar to those described for the Si NM-based transistor. A thin layer of Al_2O_3 deposited with ALD served as the dielectrics. Using conventional photolithographic patterning and wet etching (BOE, 6:1) opens the contact area of Si NM. Another thin layer of Cr/Au (10 nm/300 nm) patterned with photolithography provided conducting pads for electrical measurements. The interfacial debonding process reported here was then conducted in water to deliver the device layer to a receiver substrate.

Fabrication of Si NM/MoS_2 Heterojunction Photodiode Nanosystem. The as-synthesized MoS_2 monolayers were spin-coated with PMMA (Microchem) from their growth Si substrate. Immersion of the specimen into a solution of potassium hydroxide (KOH, 2 M; Fisher Scientific) allowed the MoS_2 monolayers to be separated from the Si surface. The MoS_2 monolayers were then fished out with a preprepared SiO_2/Si wafer that contains photolithographic patterned Cr/Au (5 nm/50 nm) electrodes, Si NM, D-PI, and Ni on the top. Immersion of the entire structure in acetone washed away the PMMA layer to expose the surface. The interfacial debonding process reported here was then conducted in water to deliver the device layer to a receiver substrate.

Characterization of Si NRs-Based Temperature Sensor. The *I–V* curves of the semiconductor devices were recorded using a semiconductor analyzer (4200A-SCS; Keithley) in a probe station (Signatone). The constant current at 50 or 100 μA was applied to measure voltage for the p-i-n–doped Si NR-based diodes. For the calibration of the temperature sensor, constant temperature ranging from 23 to 50 °C was applied using a hot plate during the measurements. These measurements were simultaneously monitored using an IR thermometer (Kintrex) for control comparisons. The typical changes of the voltage on the temperature were ∼1.7 and ∼1.8 $mV•°C^{-1}$ at the constant current of 50 and 100 μA, respectively.

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