Solution-processed single-walled carbon nanotube field effect transistors and bootstrapped inverters for disintegratable, transient electronics

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Solution-processed single-walled carbon nanotube field effect transistors and bootstrapped inverters for disintegratable, transient electronics

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This paper presents materials, device designs, and physical/electrical characteristics of a form of nanotube electronics that is physically transient, in the sense that all constituent elements dissolve and/or disperse upon immersion into water. Studies of contact effects illustrate the ability to use water soluble metals such as magnesium for source/drain contacts in nanotube based field effect transistors. High mobilities and on/off ratios in transistors that use molybdenum, silicon nitride, and silicon oxide enable full swing characteristics for inverters at low voltages (~5 V) and with high gains (~30). Dissolution/disintegration tests of such systems on water soluble sheets of polyvinyl alcohol demonstrate physical transience within 30 min. © *2014 AIP Publishing LLC*.
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Transient electronics represents an emerging technology in which the constituent devices are designed to allow complete or partial physical disappearance in a controlled manner after serving their targeted functions. Application concepts range from active biodegradable implants to hardware-secure memory systems, vanishing environmental sensors, and consumer electronics with reduced waste streams.[1–6] These envisioned technologies create opportunities for research into electronic materials, device designs, and unconventional techniques for micro/nanofabrication. Among the various essential materials, the semiconductor is often the most challenging. Recent work demonstrates that nanomembranes of silicon are attractive for this purpose because of their stable, reproducible, and superior electrical characteristics together with their dissolution by hydrolysis in biofluids, ground water, and sea water.[1–5] Other materials, such as ZnO[6] and organic/bioorganic polymers,[7] represent additional options.

The results reported here illustrate the ability to form transient field effect transistors (FETs) with networks of purified single walled nanotubes (SWNTs). The nanoscale dimensions of the SWNTs, their ability to form percolating networks at low areal coverage, their excellent electrical properties, and the capacity of networks of them to disperse upon disappearance of a supporting substrate make this system attractive for transient electronics that operate by a combination of controlled disintegration and dissolution. Although SWNT networks have been widely explored in individual devices and integrated circuits,[8–10] their use with transient materials for the purpose of transient electronic systems has not been explored. This work combines SWNTs with water soluble dielectrics, metals, and substrates to yield transient bootstrapped SWNTs inverters, with improved noise margin and logic swing compared to previously described, non-transient counterparts.[11] Full swing electrical properties studied using both DC and pulsed mode techniques reveal the intrinsic properties as well as effects of contacts formed using transient metals. Demonstration vehicles serve to illustrate a mode of transience in which the SWNT networks disintegrate and all other constituent materials dissolve completely upon immersion in water.

Figs. 1(a)–1(d) summarize an overall fabrication scheme that involves processing of devices using transient materials (i.e., Mo for electrodes and interconnects; SiO_x and SiN_x for gate and interlayer dielectrics) on a temporary substrate followed by transfer to a water-soluble film of poly(vinyl alcohol) (PVA, $M_w \sim 31\,000$). The first step is electron beam evaporation of a layer of Ni (~300 nm) onto a silicon wafer with a layer of thermal oxide (300 nm) on its surface, followed by plasma-enhanced chemical vapor deposition (PECVD) of SiO_x (~100 nm) at 300 °C. Photolithographic patterning of Mo (~70 nm, electron beam evaporation) creates gate electrodes. Bilayers of SiN_x (~50 nm) and SiO_x (~30 nm) deposited by PECVD at 300 °C serve as gate dielectrics. Exposing the SiO_x to an O_2 plasma (~30 W, 10 min) yields a hydrophilic surface which, after solution casting with poly-L-lysine for 5 min, consecutively rinsing with deionized (DI) water, and drying under a stream of N_2, yields a surface that can be coated with SWNTs in a spatially uniform manner with controlled density.[10] This work used SWNTs, as-received, with 98% semiconductor content (IsoNanotubes-S from NanoIntegris, Inc.). Rinsing with DI water and isopropyl alcohol (IPA), and then drying again under N_2[10] prepares the substrate for deposition and patterning of Mo (~50 nm) (or Ti/Pd ~ 2/50 nm) after removal of SiO_x/SiN_x by reactive ion etching (RIE; O_2/CF_4) to create openings for contacts. The final step of the fabrication involves removal of SWNTs from the periphery by RIE ($O_2 \sim 100$ mTorr, 75 W, 1 min). Fig. 1(b) illustrates a cross sectional view of devices along the line from A to B

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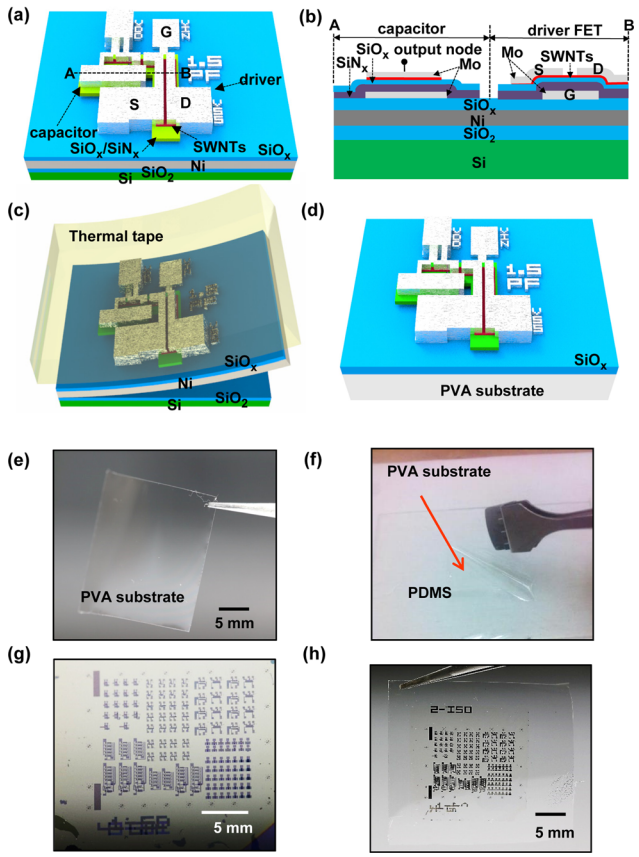

FIG. 1. Schematic illustrations and images of the process sequence: (a) fully formed SWNT devices fabricated on a substrate of SiO_x/Ni/SiO_2/Si (b) cross sectional view of devices along the line denoted by A and B in (a), (c) retrieving fully formed devices in water by using thermal tapes, (d) transferred devices on a PVA substrate after etching the residual Ni on the back side of SWNT devices/SiO_x. (e) PVA substrates prepared by drop casting of PVA solution (~10 wt. %) and (f) after laminating on a slide glass coated with PDMS for transfer printing process. An optical micrograph (g) for fully formed SWNT FETs on a Si substrate with trilayer coating of SiO_x/Ni/SiO_2 before retrieval and (h) for their devices after transferred to a PVA substrate.

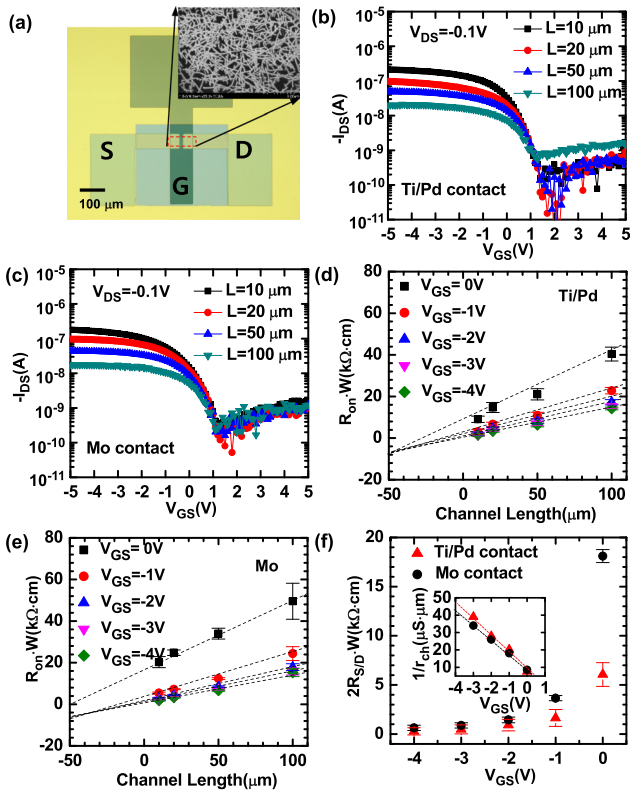

FIG. 2. (a) Optical micrographs for typical SWNTs FETs fabricated on SiO_x/Ni/SiO_2/Si (b) transfer characteristics at various channel lengths between 10 μm and 100 μm at $V_{DS} = -0.1$ V for devices with (b) Ti/Pd and (c) Mo contacts. Total on-resistance, i.e., $R_{on} \sim 2R_{S/D} + r_{ch}L$, of SWNTs FETs with (d) Ti/Pd and (e) Mo contacts at various channel lengths between 10 μm and 100 μm as a function of gate to source voltage (V_{GS}). (f) Contact resistance extracted from SWNT FETs with Ti/Pd (or Mo) contacts by using gated transmission line method. The inset indicates that the average value of the inverse of the unit channel resistance depends on V_{GS}. The slopes for Ti/Pd and Mo contact FETs as shown in the inset are similar within experimental error.

(Fig. 1(a)) at the location of a bootstrapped capacitor and a driver transistor. Baking on a hot plate (~110 °C) for 10 min, followed by electrical characterization with a semiconductor parameter analyzer (Agilent B1500A) combined with a waveform generator/fast measurement unit (WGFMU; B1530A) enables extraction of intrinsic properties.

A thermal release tape (Nitto Denko Co.) adhered to the devices, as shown in Fig. 1(c), facilitates release from the silicon substrate upon immersion in water.[12] Etching in ferric chloride solution (Sigma Aldrich) eliminates the Ni on the backside of the devices. Gently rinsing in water and drying under a stream of dry nitrogen prepare the structure for transfer. This process involves pressing the tape with circuits on its surface against a PVA film (Fig. 1(e); ~30 μm thickness, drop cast from solution (~10 wt. %) in a plastic container and dried in a convection oven at 80 °C), held onto a glass slide with a coating of poly(dimethylsiloxane) (PDMS) as shown in Fig. 1(f). Heating on a hot plate at 100 °C allows release of the tape. Peeling away the PVA (Fig. 1(d)) completes the process. Fig. 1(e) shows the PVA substrate before transfer printing. Fig. 1(h) shows fully formed SWNTs FETs and circuits fabricated on carrier substrates as in Fig. 1(g) after transfer to PVA.

Fig. 2(a) shows an optical micrograph of SWNTs FETs with Mo (or Ti/Pd) source and drain electrodes. The inset provides an SEM image of the SWNT network. Figs. 2(b) and 2(c) present transfer characteristics of SWNTs transistors with Ti/Pd contacts, as reference, and with transient Mo contacts, both for devices with various channel lengths between 10 μm and 100 μm. These measurements used a pulse mode technique[13] to suppress effects of hysteresis.[14] Comparison of the Ti/Pd with Mo cases suggests differences in contact properties. In the linear regime, the overall device resistance[15,16] (R_{on}) can be expressed as the sum of the channel resistance ($r_{ch}L$) and contact resistance ($2R_{S/D}$) according to

$$R_{on} = \frac{\partial V_{DS}}{\partial I_{DS}}\bigg|_{V_{DS}\to 0}^{V_{GS}} = r_{ch}L + 2R_{S/D} = \frac{L}{W\mu_{FEi}C_G(V_{GS} - V_{Ti})} + 2R_{S/D}, \quad (1)$$

where r_{ch} is the channel resistance per channel-length (L) unit and $2R_{S/D}$ is the combined contact resistance ($R_{S/D}$) associated with the source and drain electrodes. Here, μ_{FEi} and V_{Ti} are the intrinsic field effect mobility and threshold voltage, respectively. The contact resistance[15] ($2R_{S/D}$) and

the unit channel resistance[16] (r_{ch}) can be extracted from the intercept and slope, respectively, of linear fits to plots of $R_{on}\cdot W$ as a function of L for different gate voltages, as shown in Figs. 2(d) and 2(e). Fig. 2(f) summarizes width normalized contact resistances ($2R_{S/D}\cdot W$) for SWNT FETs with Ti/Pd and Mo contacts. The results indicate that the contact resistances for Mo are consistently higher (roughly three times) than those with Ti/Pd, ranging from ($\sim$18.00 $\pm$ 0.60 k$\Omega\cdot$cm) to ($\sim$0.64 $\pm$ 0.27 k$\Omega\cdot$cm) for Mo and from ($\sim$6.06 $\pm$ 1.21 k$\Omega\cdot$cm) to ($\sim$0.29 $\pm$ 0.37 k$\Omega\cdot$cm) for Ti/Pd, as the V_{GS} changes from 0 V to -4 V, respectively. These differences can be attributed, at least partly, to differences in Schottky barrier heights[17] (Φ_p), associated with the work functions of these two metals ($\Phi_{Pd} \sim 5.1$ eV, $\Phi_{Mo} \sim 4.6$ eV).

The dependence of the reciprocal unit channel resistance on V_{GS}, as shown in the inset of Fig. 2(f), can be utilized to extract intrinsic field effect motilities (μ_{FEi}) according to

$$\mu_{FEi} = \frac{1}{WC_G}\frac{\partial(1/r_{ch})}{\partial V_{GS}}. \quad (2)$$

The gate capacitance[10,18] (C_G) can be calculated by considering the electrostatic coupling between nanotubes using the analytical equation

$$C_G = \left\{ {C_Q}^{-1} + \frac{1}{2\pi\varepsilon_o\varepsilon_r} In\left[\frac{\Lambda_o}{R}\frac{\sinh(2\pi t_{ox}/\Lambda_o)}{\pi}\right]\right\}^{-1} {\Lambda_o}^{-1}, \quad (3)$$

where $1/\Lambda o$ stands for the density of nanotubes ($3/\mu$m), ${C_Q}^{-1}$ is the quantum capacitance (4 pF/cm), t_{ox} is the thickness of gate dielectrics (80 nm), R is the radius of nanotubes ($\sim$0.7 nm), ε_o is the vacuum permittivity, and ε_r is the relative dielectric constant (3.17) of the air/SWNT/SiO_x/SiN_x sandwich structure. The value of C_G and the slope of the linear fit to $(1/r_{ch})$ as a function of V_{GS}, as shown in the inset of Fig. 2(f), are 17.9 nF/cm^2, and 9.7 (Pd) and 8.47(Mo) $\mu S\cdot\mu m\cdot V^{-1}$, accordingly. The intrinsic field effect motilities for SWNT FETs with Ti/Pd and Mo contact are extracted as 17.3 and 15.7 cm^2/V s. (With C_G extracted using a simple parallel plate approximation (59.2 nF/cm^2), the field effect mobilities are 5.22 (Pd) and 4.77(Mo) cm^2/V s, respectively.) The results indicate that the intrinsic field effect mobilities are approximately the same for Mo and Ti/Pd contacts, as might be expected.

SWNT transistors typically have stable p-type behaviors in air. Operation in n-type mode is, by comparison, difficult to achieve reliably.[9] Therefore, basic logic elements such as conventional enhancement-load inverters,[10,19] which use diode connected loads, are commonly used. Although this scheme is simple, the threshold voltage drop at the source terminal can significantly reduce the logic swing and noise margins.[20] Here, we use bootstrapped SWNTs inverters, as shown in Figs. 3(a) and 3(b). The circuits include a driver transistor (W/L = 600/10 μm), a load transistor (W/L = 40/10 μm), a gated diode (W/L = 20/10 μm), and a bootstrap capacitor (5.2 pF). Fig. 3(b) shows a circuit schematic of the inverters, including the effects of probing load associated with the internal resistance and the capacitance of the oscilloscope. The voltage transfer characteristics (VTCs) and

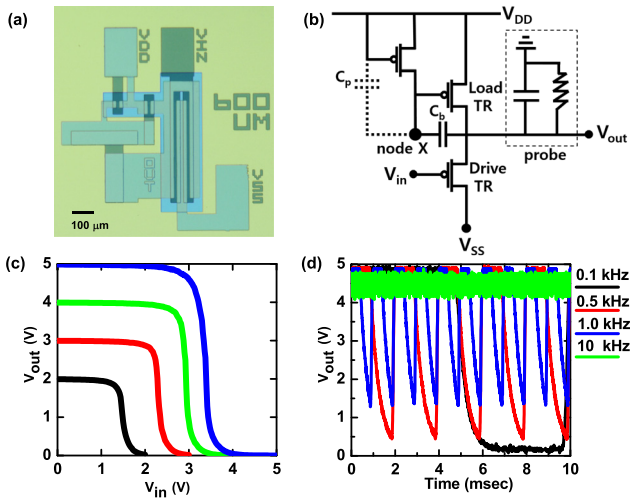

FIG. 3. (a) An optical micrograph, (b) a schematic illustration, (c) DC voltage transfer characteristics, and (d) AC dynamic responses for boot strapped inverters. The illustration includes effects of parasitic loading associated with probing contact pads, coaxial connection cables, and the internal load of a testing oscilloscope. Dynamic responses were characterized as the frequency of an input square pulse with 5 V amplitude increases from 0.1 KHz to 10 KHz.

dynamic switching behaviors appear in Figs. 3(c) and 3(d), respectively. The maximum gain ($(dV_{out}/dV_{in})_{max}$) is $\sim$30 for supply voltages (V_{SS}) between 2 V and 5 V at a fixed V_{DD} of 0 V. This operation follows from voltage bootstrapping and use of a high ratio of driving and load transistors.[20] Bootstrapping can compensate the voltage drop associated with V_{th} for the load transistor to reduce the magnitude of the voltage at output low (V_{OL}) during inverter operation. This function can boost the transition action during the period of transition from high to low, i.e., to reduce the fall time. The design for the ratio of the width of the driver FET to the width of the load FET is also important because this ratio (k) can determine both maximum gain and the voltage at output high (V_{OH}). The full swing behavior of circuits reported here benefits from both effects.

Figure 3(d) shows dynamic behaviors for the case of a square wave with 5 V amplitude (f = 100 Hz, duty cycle (DC) = 0.5) applied to the input node at a bias condition of V_{SS} = 5 V, V_{DD} = 0 V). As the frequency increases from 0.1 kHz to 10 kHz with fixed other parameters, the switching behavior gradually degrades due to the propagation delay.[21] Such limitations originate primarily from parasitic capacitances of the driver and load transistors as well as the electrical connections between the oscilloscope (Tektronix, TDS2012C; input capacitance of 13 pF) and the inverter output node. The rise and fall times at 100 Hz are 0.35 ms and 1.51 ms, respectively. These results suggest that low currents from the load FET (W/L = 40/10 μm) compared to those from the driver FET (W/L = 600/10 μm) lead to long dissipation times for charges stored in the parasitic capacitors[21] from the combined contributions of the device elements, the oscilloscope, and the connection lines. Increasing the size of the load FET, while maintaining k, can reduce the fall time.

All observed electrical characteristics are, to within uncertainties, the same before (Fig. 1(g)) and after (Fig. 1(h)) transfer from silicon to PVA. Fig. 4 shows a set of images collected in a time sequence during dissolution of

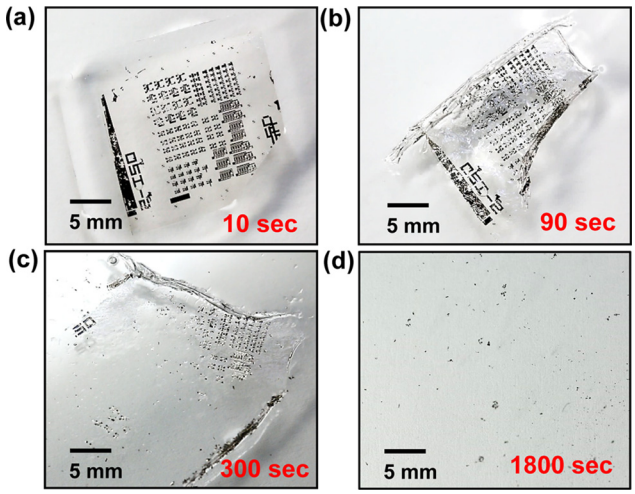

FIG. 4. Images of a various stages of dissolution and disintegration of SWNT FETs and boot strapped capped inverters on a PVA substrate in water, at (a) 10 s, (b) 90 s, (c) 300 s, and (d) 1800 s.

SWNT FETs and its circuits on PVA substrate in DI water at room temperature. The PVA substrate ($\sim$30 μm), for the formulation used here, slowly disappears within 30 min by simple dissolution. This process causes the device and circuit to physically disintegrate. Afterward, each remaining constituent material, including SiO_x, SiN_x, and Mo, disappears due to hydrolysis at different rates, as described in the previous reports.[1–6] The SWNTs disperse and aggregate into small bundles. The timeframes for dissolution and disintegration can be programmed not only by encapsulation and packing methods via film deposition or/and drop casting but also by selections of physical dimensions, film thicknesses, and configurations in the materials used for SWNTs circuits.

In summary, the results presented here indicate that networks of SWNTs can be combined with dissolvable dielectrics, electrodes, and substrates to yield transistors and bootstrapped inverters that offer transient behavior due to disintegration and dissolution in water. The findings illustrate that network type of active layers, in this example SWNTs, can be attractive candidates for semiconductors in disintegrating electronic systems.

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