

Electroassisted Transfer of Vertical Silicon Wire Arrays Using a Sacrificial Porous Silicon Layer

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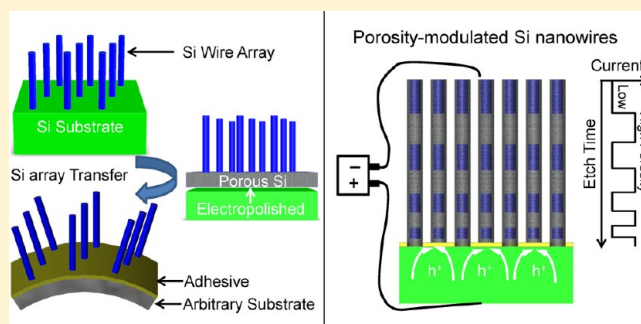
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S Supporting Information

ABSTRACT: An electroassisted method is developed to transfer silicon (Si) wire arrays from the Si wafers on which they are grown to other substrates while maintaining their original properties and vertical alignment. First, electroassisted etching is used to form a sacrificial porous Si layer underneath the Si wires. Second, the porous Si layer is separated from the Si wafer by electropolishing, enabling the separation and transfer of the Si wires. The method is further expanded to develop a current-induced metal-assisted chemical etching technique for the facile and rapid synthesis of Si nanowires with axially modulated porosity.

KEYWORDS: Vertical nanowire, porous silicon nanowire, transfer printing, metal-assisted chemical etching, electropolishing, flexible electronics



Because of their potential of surpassing conventional lithography limitations and tuning their chemical and physical properties at the nanometer scale during growth, silicon (Si) nanowires are attractive building blocks for future high-performing functional electronic devices.^{1–3} While extensive research has been devoted to developing methods to assemble and integrate Si nanowires into planar functional devices,^{4–6} limited efforts have been devoted to the device integration of vertical Si wire arrays (both nanowires and microwires) even though they are important for applications ranging from sensors,^{7–9} solar cells,^{10–13} thermoelectric devices,^{14–16} Li-ion batteries^{17–19} to vertical field-effect transistors.^{20,21} Si wire arrays with lengths of a few to tens of micrometers are usually formed by the deposition of vapor onto a Si wafer that is about 500 μm thick, rigid, and opaque, or by the chemical etching of such a wafer. Separation of the resulting Si wire arrays from the parent Si wafer allows the electrical, thermal, optical, and mechanical properties of the Si wire arrays to be isolated and harnessed in devices without being overshadowed by the properties of the thick parent Si wafer and enables the transfer of the Si wire arrays to other flexible, lightweight, low cost, or transparent substrates for enhanced device functionality. A key requirement for the separation and transfer of Si wire arrays is the preservation of their original properties and orientation.^{4–6} A range of methods have been developed for the separation of vertical Si wire arrays from their parent Si wafers, which rely on the mechanical breakage of the Si wires by the application of peeling forces,^{22–24} direct shear forces,^{25–27} or the creation of a horizontal porous crack within the Si wires.^{28,29} However, these methods require that the Si wires are held together during the mechanical breaking process

by encapsulation in a polymer host, the existence of which makes it difficult to use the separated Si wires for applications that require an exposed Si surface, such as for ohmic contacts to metal electrodes, sensors, or catalysts. In addition, some of these methods are only compatible with Si wires of certain geometries^{22–27} or those made by particular methods.^{28,29} To address these shortcomings, we have developed, and report herein, a new electroassisted transfer printing method for the transfer of vertical Si wire arrays from their parent Si wafers to other substrates without modification to the properties and orientation of the Si wires, without constraints on the Si wire geometry or fabrication method, and without the need for polymer encapsulation. The fundamental understanding gained from this new electroassisted transfer method also enabled us to develop a current-induced metal-assisted chemical etching method for the facile and rapid synthesis of Si nanowires with axially modulated porosity.

Our electroassisted transfer method relies on a sacrificial porous Si layer^{30,31} for the separation of vertical Si wire arrays (both nanowires and microwires) from their parent Si wafers by the general procedure illustrated in Figure 1. Si wires are first formed by either deep reactive ion etching (DRIE) or metal-assisted chemical etching (MACE) of a p-type Si wafer (boron dopant concentration of 10^{14} cm^{-3}) (Figure 1a for schematic and Figure 1f for scanning electron microscopy (SEM) image). An aluminum (Al) film is then deposited on the back of the Si

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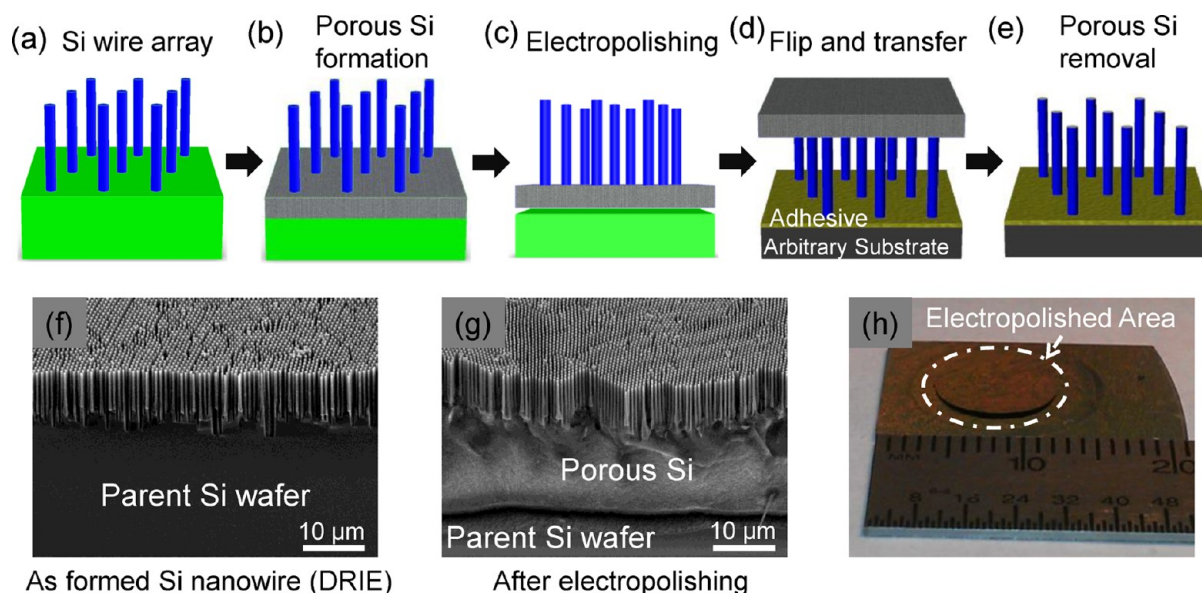


Figure 1. Schematic of the electroassisted transfer of vertical Si wire arrays. (a) A vertical Si wire array is fabricated on a parent Si wafer, (b) a sacrificial porous Si layer is formed beneath the Si wire array by electroetching the parent Si wafer, (c) the porous Si layer, together with the top Si wire array, is detached from the parent Si wafer by electropolishing, (d) the Si wire array supported by the porous Si is flipped over, attached and transferred to any flat substrate coated with an adhesive, and (e) the porous Si layer is etched away. SEM images of the Si nanowires (formed by DRIE) (f) before and (g) after the porous Si layer is electropolished from the Si wafer. (h) An optical image showing that the Si nanowire array held together by the porous Si layer is lifted off from the parent Si wafer after the electropolishing step.

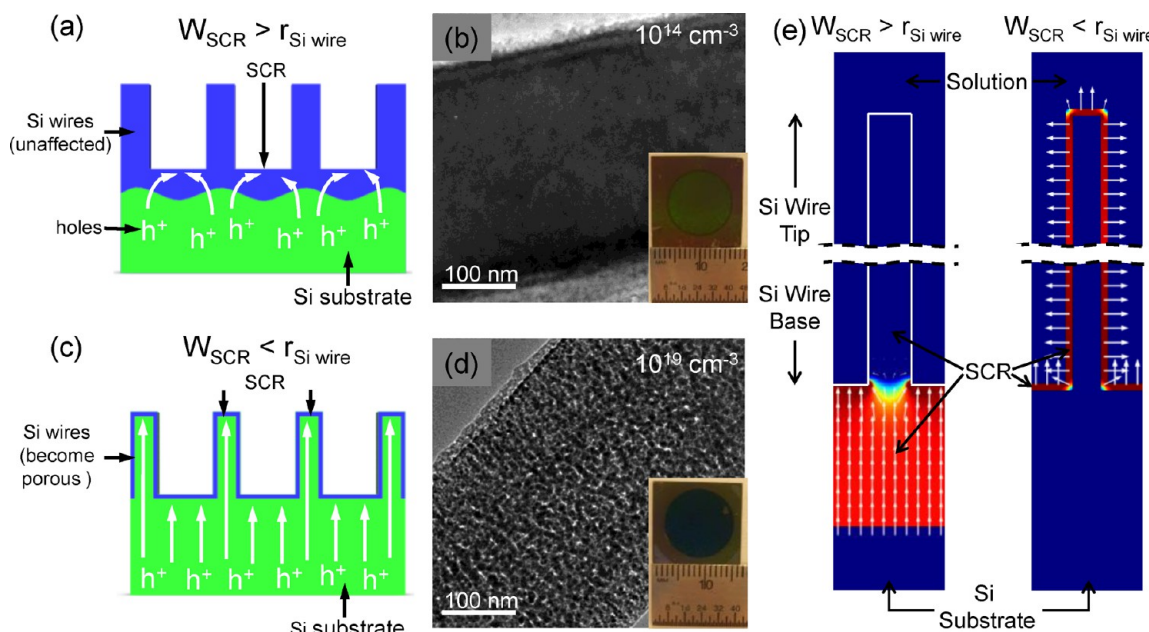


Figure 2. The location of the space-charge region determines the distribution of the electric field and therefore the location of the porous Si formation. Porous Si forms underneath the Si wires when the space-charge region (blue) width (W_{SCR}) is greater than the Si wire radius ($r_{Si\ wire}$) (a,b) and inside the Si wires when $W_{SCR} < r_{Si\ wire}$ (c,d). TEM and optical images (insets) show that the p-type Si nanowires with doping concentrations of (b) $10^{14}\ \text{cm}^{-3}$ and (d) $10^{19}\ \text{cm}^{-3}$ have different internal porosity after the porous Si layer formation step, supporting the schematics in (a,c), respectively. (e) The calculated electric field by COMSOL around a Si wire shows that the electric field directs holes away from the Si wire when $W_{SCR} > r_{Si\ wire}$ and through the Si wire $W_{SCR} < r_{Si\ wire}$.

wafer to serve as an electrode for the following electroetching process (see Experimental Methods). Then the parent Si wafer with the Si wire array on top is placed in a Teflon anodization cell filled with an ethanolic HF electrolyte solution (1:1 v/v mixture of 48% HF and 100% ethanol) (Supporting Information Figure S1). A constant current of $50\ \text{mA}/\text{cm}^2$ is applied for 20 min between the Al electrode on the back of the

Si wafer and a platinum (Pt) counter electrode submerged in the ethanolic HF solution, which leads to formation of a porous Si layer of about $15\ \mu\text{m}$ thickness beneath the Si wire array (Figure 1b). The porous Si layer, together with the Si wire array on top, is subsequently separated from the parent Si wafer by the standard electropolishing method (Figure 1c).^{32–36} The electropolishing is achieved by applying $50\ \text{mA}/\text{cm}^2$ between

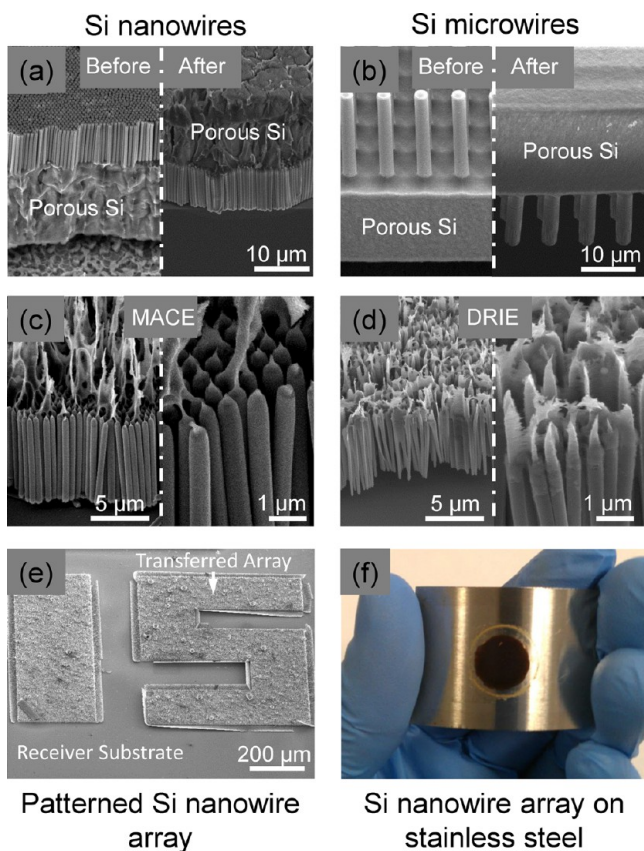


Figure 3. Generality of the electroassisted transfer method in transferring different Si wires to other substrates. SEM images of (a) Si nanowires and (b) Si microwires before (left images) and after (right images) the electroplating and transfer step. Low (left images) and high-magnification (right images) SEM images of transferred (c) MACE and (d) DRIE Si nanowire arrays after the sacrificial porous Si layer is etched away. (e) SEM image shows that a patterned Si nanowire array (in letter 15) is well preserved after being transferred to a different Si substrate and removal of the porous Si layer. (f) Optical image of a Si nanowire array transferred to a flexible stainless steel sheet.

the Al and Pt electrodes in a 1:3 v/v mixture of 48% HF and 100% ethanol for 15 s (Supporting Information Figure S1).^{35,37} The electroplating process has lower HF concentration (25% vol.) than that of the electroetching process (50% vol.). The smaller concentration of HF in the etchant reduces the diffusional flux of F^- ions to the Si surface. As such, the Si surface is oxidized to form a continuous oxide layer (instead of individual pores) and the entire oxide layer is subsequently removed as a “lift-off”. Figure 1g,h shows the SEM and optical images of the Si nanowires on top of the porous Si layer after the electroplating step, and both images show that the porous Si layer, together with the top Si nanowires, is separated from the parent Si wafer. Figure 1h shows a case where the porous Si layer (white dotted circle showing the size of the Si area exposed in the anodization cell) is already lifted off from the parent Si wafer by electroplating. The degree of electroplating can be tuned from slightly weakened to severely weakened by changing the electroplating time and applied current. Next, the entire Si wafer is gently removed from the anodization cell and dried in a critical point drier to prevent the porous Si layer from cracking. Subsequently, the porous Si layer with the top Si wire array is easily removed from the Si parent

wafer, flipped over and attached to an arbitrary flat substrate by an adhesive (e.g., polyvinyl alcohol, Ag epoxy) (Figure 1d). The porous Si layer is then etched away in a 0.03 M KOH solution containing 10% ethanol for 30 min, which is capable of removing the porous Si layer without causing much damage to the Si wires due to the low concentration of KOH (Figure 1e).^{30,31,34}

One key requirement for our electroassisted transfer method is that the formation of porous Si should be restricted to the Si underneath the Si wires, not within the Si wires, in order to preserve the original properties of the Si wires. Porous Si is formed only when holes (h^+), reach a Si surface that is exposed to hydrofluoric acid.³⁸ Therefore, in order to prevent the Si wires from becoming porous, the holes should be directed away from the Si wire surface. This can be accomplished by controlling the width of the space-charge region (SCR) at the Si surface that is in direct contact with the electrolyte. The SCR is depleted of mobile charge carriers, behaving as a nearly insulating region. Since the porous Si is formed under a forward bias condition, the current of holes has to pass the SCR region first and then reach to the Si surface; naturally the holes will select the least resistive pathway. When the width of the SCR (W_{SCR}) is larger than the radius of the Si wires ($r_{Si\ wire}$) (Figure 2a) and the conductivity of the ethanolic HF etchant solution (estimated to be $\sim 1\ S/cm$)^{37,39} is much larger than the conductivity of the depleted Si wires,⁴⁰ the least resistive pathway for holes is through the gaps between the Si wires, not through the Si wires, leading to little porosity formation within the Si wires (Figure 2b).^{40–42} On the other hand, when W_{SCR} is smaller than $r_{Si\ wire}$, the holes can go through the inside of Si wires (Figure 2c), leading to porosity inside the Si wires and in the Si underneath the wires (Figure 2d).

To illustrate the importance of the relative width of the SCR to the radius of the Si wires, the electric field around Si wires is simulated using COMSOL Multiphysics software (Comsol; Stockholm, Sweden) (see Experimental Methods). As shown in Figure 2e, when W_{SCR} is greater than $r_{Si\ wire}$, the electric field directs the holes to flow between the Si wire gap into the solution, not through the Si wires. When W_{SCR} is smaller than $r_{Si\ wire}$, the SCR only exists near the surface of the Si wires and the holes can readily reach to the surface of the Si wires. Experimentally, we vary the ratio of W_{SCR} to $r_{Si\ wire}$ by changing the doping concentration of the parent Si wafer. The W_{SCR} can be estimated from

$$W_{SCR} = \left(\frac{2\epsilon_r\epsilon_0V}{eN_A} \right)^{1/2} \quad (1)$$

, where ϵ_r is the relative dielectric permittivity, ϵ_0 is the permittivity of vacuum, V is the applied bias, e is the electron charge, and N_A is the number of ionized acceptors. When the Si wires are lightly doped with a boron concentration of $10^{14}\ cm^{-3}$, the estimated W_{SCR} is about $3\ \mu m$, which is much larger than $r_{Si\ wire}$ ($\sim 280\ nm$). In this case, the Si wire does not show signs of porosity in the transmission electron microscope (TEM) image in Figure 2b, taken after the porous Si formation step. On the other hand, when the Si wires are heavily doped with a boron concentration of $10^{19}\ cm^{-3}$, the estimated W_{SCR} is about $10\ nm$, much smaller than $r_{Si\ wire}$ ($\sim 280\ nm$). In this case, the Si wire is clearly porous after the porous Si formation step (Figure 2d) and the inset optical image shows that the Si wires are much darker after the porous Si formation step. Therefore, application of our electroassisted transfer method requires

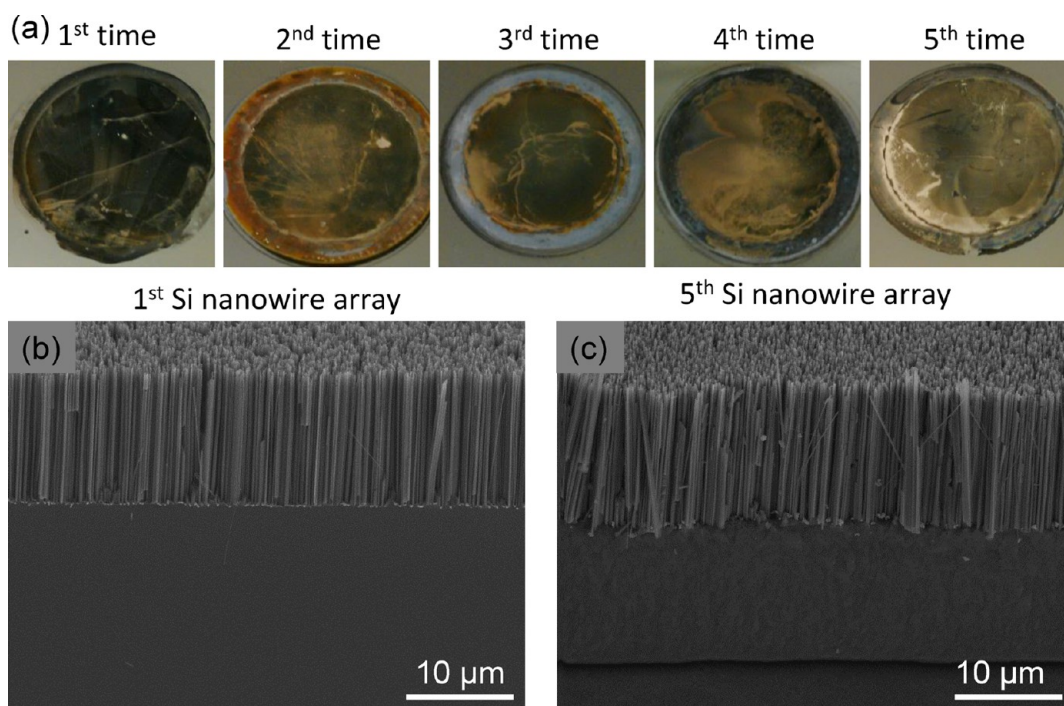


Figure 4. Recyclability of the parent Si wafer to form and transfer multiple Si wire arrays from a single substrate. (a) Optical images of five Si nanowire arrays that are consecutively formed by MACE and transferred. SEM images show that Si nanowires of similar morphology are formed by the electroassisted transfer method before the (b) first and (c) fifth time transfer.

W_{SCR} to be greater than $r_{Si\ wire}$ to limit the porosity formation inside the Si wires.

Our electroassisted transfer method has four key merits. The first merit is its generality for transferring Si wire arrays, regardless of their dimensions and the methods by which they are fabricated. The transfer of Si nanowires (diameter, 280 nm; length, 12 μm ; spacing, 650 nm) formed by the DRIE method has already been demonstrated in Figure 1. Figure 3a,b shows that this transfer method is equally applicable to Si nanowire arrays (diameter, 300 nm; length, 10 μm ; spacing, 400 nm) fabricated by the MACE method and Si microwires (diameter, 3 μm ; length, 18 μm ; spacing, 7 μm) formed by the DRIE method. The left SEM images in Figure 3a,b show the Si wires before the transfer step but after electropolishing (equivalent to Figure 1c). The porous Si layer is clearly visible below the Si wire array and has been separated from the parent Si wafer below. The right SEM images in Figure 3a,b show the Si wires after they are removed from the parent Si wafer and transferred to a receiver substrate. The Si wires look identical to those before the transfer. The porous Si layer can be removed after the transfer step by etching in a 0.03 M KOH solution containing 10% ethanol for 30 min. After the porous Si layer removal, the SEM images in Figure 3c,d show the remaining Si nanowire arrays formed by MACE and DRIE, respectively. There are still some porous Si strips on the ends of Si nanowires, which is consistent with the simulation results in Figure 2e in that a narrow strip of Si right underneath the Si wires is less porous due to the local electrical field. The second merit of this transfer method is that the alignment and structure of the Si wires are kept intact by the porous Si layer during the transfer. As such, even-patterned Si wire arrays can be transferred with high fidelity. Figure 3e shows that a prepatterned Si nanowire array (number: 15) is transferred to a different Si substrate while maintaining the patterned shape.

The third merit of the electroassisted transfer method is that Si wires can be transferred to any substrate, such as stainless steel sheets (Figure 3f), as long as the substrates are kept flat during the attachment of the Si wire array. The fourth merit is that Si wafers can be repeatedly used to form vertical Si wire arrays by etching and transferring Si wires to different substrates. Since the electropolishing step creates a new and relatively flat polished Si surface underneath the porous Si layer, it allows new Si wires to be etched on the same parent Si wafer. The recycling ability of the Si wafer is demonstrated in Figure 4 by forming Si nanowire arrays by MACE and transferring them five consecutive times. As shown in Figure 4a, new Si nanowire arrays can be formed after each transfer, though the uniformity decreases since the freshly exposed Si surface is not perfectly flat after electropolishing. The surface roughness of the Si can be improved by adding an intermediate surface polishing step. Even though there is some global surface roughness, the morphology of the first array of Si nanowires (Figure 4b) is similar to that of the fifth wire array (Figure 4c), showing the ability to recycle the parent Si wafer.

In our electroassisted transfer method, the holes are the oxidizing species and are supplied from inside the parent Si wafer. The local concentration of holes controls the local oxidation rate of the Si and its removal rate in HF. Holes play the same oxidizer role as the H_2O_2 commonly used in the MACE method, so we can replace H_2O_2 in the MACE method with an electrical current (equivalently a flow of holes) to synthesize Si nanowires. To illustrate this, we follow the same preparation steps of the MACE method by first patterning the Ag/Au catalyst on top of a Si wafer. Next, we place the Ag/Au coated Si wafer in a Teflon anodization cell fill with a modified MACE etchant (4.8 M HF solution but without H_2O_2). Then, we pass a current between the Al contact on the back of the Si wafer and a Pt counter electrode immersed in the etchant to

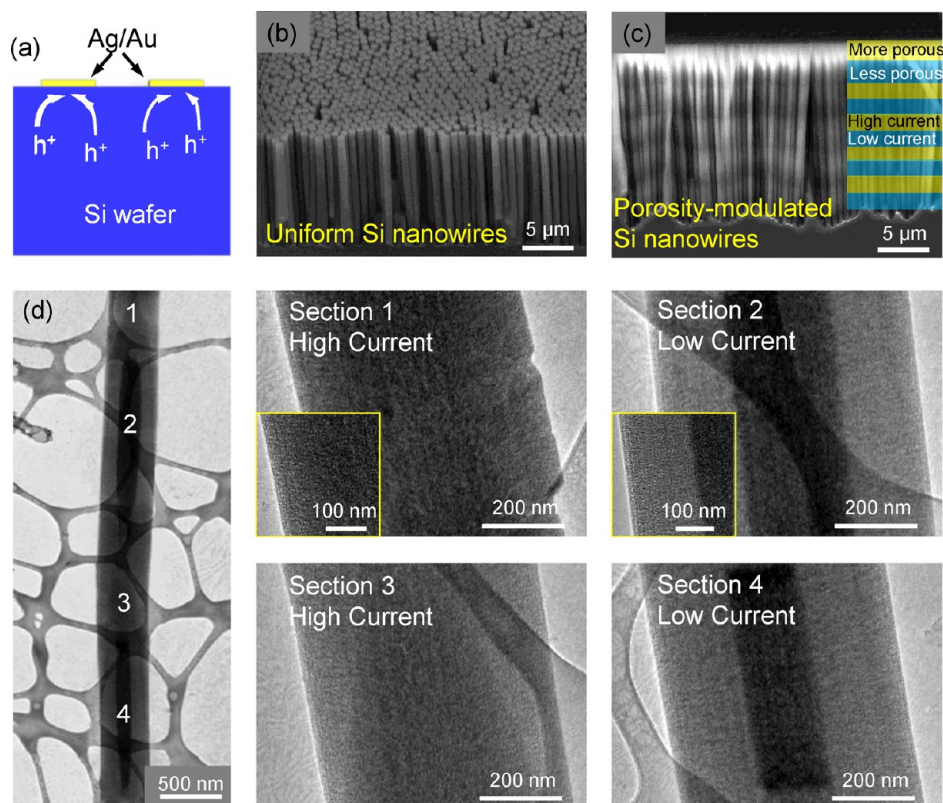


Figure 5. Synthesis of Si nanowires by the current-induced MACE for which the oxidizer, H_2O_2 is replaced by an applied current. (a) Schematic shows that the holes within the Si substrate preferentially oxidize Si beneath the patterned Ag/Au catalyst. (b) SEM image of an axial uniform Si nanowire array etched in a 4.8 M HF solution with a constant 15 mA/cm^2 applied current. (c) SEM and (d) TEM images of a Si nanowire array with axially modulated porosity etched in a 4.8 M HF solution by switching the applied current between 7 and 23 mA/cm^2 periodically in a 4.8 M HF solution. High-magnification TEM images show that the high current density (23 mA/cm^2) results in porous Si nanowire segments (center images, sections 1 and 3) and the low current density (7 mA/cm^2) results in nonporous/porous core/shell Si nanowire segments (right images, sections 2 and 4).

supply holes that mimic the role of H_2O_2 . The holes move toward the top Ag/Au film (Figure 5a), where the Si underneath the Ag/Au is subsequently oxidized and removed by HF, leading to the formation of Si nanowire arrays (Figure 5b, etching conditions: 15 mA/cm^2 for 20 min). The benefits of using current, instead of H_2O_2 , for MACE are most pronounced when synthesizing Si nanowires with (1) long lengths for which the poor transport of H_2O_2 onto Si nanowire surface leads to etching nonuniformity or (2) axially modulated porosity or zigzag shapes. With conventional MACE, the Si wafer needs to be switched between etchants of different concentrations of H_2O_2 to vary the porosity or control the etching direction.^{43–45} In our current-induced MACE, the Si wafer stays in the same etchant but the applied current is varied to instantaneously control the etching porosity or direction. For example, when the applied current is modulated between 7 and 23 mA/cm^2 periodically, the oxidation rates of Si are changed correspondingly, leading to the formation of Si nanowire arrays with axially modulated porosity as highlighted by the SEM and TEM images in Figure 5c,d. Specifically, the high current density (23 mA/cm^2) results in porous Si nanowire segments (Figure 5d, sections 1 and 3) and the low current density (7 mA/cm^2) results in nonporous/porous core/shell Si nanowire segments (Figure 5d, sections 2 and 4).

In summary, we have developed a general electroassisted transfer method for transferring Si wire arrays, regardless of their dimensions and fabrication methods, to any other flat

substrates while maintaining their original properties and vertical alignment. This transfer method relies on the formation of a sacrificial porous Si layer underneath the Si wire array. The porous Si layer, together with the Si wire array on top, is subsequently separated from the parent Si wafer by the electropolishing method, and the Si wire array is then transferred to other substrates. The key to this transfer method is to prevent the formation of porosity in the Si wires by controlling the electric field around the Si wire arrays through the formation of a space-charge region with greater width than the radius of the Si wire. We believe that this new transfer method can be applied to transfer other nanostructures fabricated or deposited on Si wafers as well. Finally, we extend the concept of controlling the oxidation location of Si and develop a current-induced MACE technique. The current-induced MACE technique replaces H_2O_2 with an applied current and allows easy and rapid control of the Si oxidation rate by variation of the current, providing a convenient means by which to form Si nanowires with axially modulated porosity.

Experimental Methods. Preparation of Deep Reactive Ion Etched (DRIE) Si Nanowires. The DRIE Si nanowires are patterned by nanosphere lithography.^{28,29} Then, the silica spheres ($\sim 650 \text{ nm}$) are reduced to $\sim 550 \text{ nm}$ by reactive ions in a mixture of O_2 and CHF_3 to form a nonclosed-packed monolayer.^{28,29} Next, the Si nanowires are etched using DRIE (cycles of 6 s etching with 130 sccm of SF_6 and 5 s passivation with 120 sccm of C_4F_8 in a 600W plasma power) with the silica

spheres acting as a masking layer until the desired length is achieved.^{11,12,29} The silica spheres are partly etched during the DRIE process, resulting in Si nanowire diameters around 280 nm. All the polymer byproducts from the DRIE process and the silica spheres are subsequently removed in a 3:1 (v/v) mixture of sulfuric acid (H₂SO₄) and hydrogen peroxide (H₂O₂) for 10 min, followed by a 10 min soak in 2% hydrofluoric acid (HF). A 200 nm Al contact is deposited on the backside of the Si wafer and annealed at 400 °C for 30 min, creating an ohmic contact to the Si wafer.

Preparation of Metal-Assisted Chemical Etched (MACE) Si Nanowires Using Nanosphere Lithography. MACE Si nanowires with controlled diameter and density are fabricated using nanosphere lithography and e-beam evaporated noble metals. First, a 200 nm Al backside contact is deposited and annealed on the Si wafer. Then, a monolayer of 400 nm silica spheres are deposited and reduced to 300 nm on the Si front surface (same general nanosphere lithography step as above). A 15 nm silver (Ag) film followed by 5 nm of gold (Au) is evaporated over the silica spheres, followed by the spheres removal via sonication. The Si wafer surface oxide between the patterned metal film is first etched by 2% HF solution for 2 min. The Si nanowires are subsequently formed by etching the Si wafer in a solution containing 4.8 M HF and 0.3 M H₂O₂ with the assistance of a stir bar until the desired length is achieved. Finally, the metal catalyst is removed by soaking in a 3:1 (v/v) mixture of hydrochloric acid (HCl) and nitric acid (HNO₃) for 10 min.

Preparation of MACE Si Nanowires Using Silver Salts. MACE Si nanowires with smaller but less controlled diameters used to demonstrate the recycling capability are fabricated using silver salts. First, the Al contact is deposited on the back of the Si wafer. Next, the exposed front side of the Si wafer is cleaned by soaking in a 3:1 (v/v) H₂SO₄/H₂O₂ for 10 min followed by 2% HF for 2 min. Then, a thin silver film is electrodeposited on the exposed Si wafer surface in a solution of 4.8 M HF and 0.005 M AgNO₃ for 45–75 s with the assistance of a stir bar. The residual AgNO₃ is removed with thorough rinsing in DI water. The Si nanowires are then etched using the above MACE solution until the desired length is achieved.

Modeling of the Electric Field Strength around the Si Wire. The finite element program, COMSOL Multiphysics 4.3a (COMSOL; Stockholm, Sweden) with the electric current physics package, is used to simulate the electric field around the Si wires. The computational domain contains a Si wire (diameter, 300 nm; length, 10 μm) that is attached to a Si wafer and in contact with an ethanol based solution. Periodic boundary conditions are used on the left and right sides of the computation domain to simulate periodic Si wire arrays. The SCR is modeled as an intrinsic silicon layer with a resistivity of 2.3 × 10⁴ Ω-cm and the layer width is estimated by eq 1. A constant current density of 50 mA/cm² is applied to the base of the Si wafer and the solution about 50 μm above the Si wire tip is set as a ground. The steady state electric field is simulated to determine the relative electric field strengths around the Si wire.

■ ASSOCIATED CONTENT

📄 Supporting Information

Additional figure. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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Notes

The authors declare no competing financial interest.

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