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Fabrication of Flexible and Vertical Silicon Nanowire Electronics

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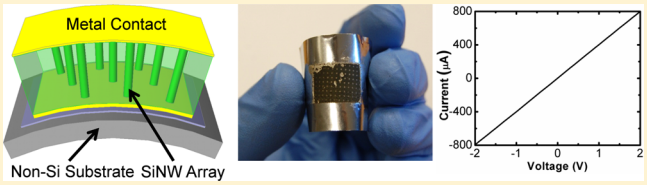
ABSTRACT: Vertical silicon nanowire (SiNW) array devices directly connected on both sides to metallic contacts were fabricated on various non-Si-based substrates (e.g., glass, plastics, and metal foils) in order to fully exploit the nanomaterial properties for final applications. The devices were realized with uniform length Ag-assisted electroless etched SiNW arrays that were detached from their fabrication substrate, typically Si wafers, reattached to arbitrary substrates, and formed with metallic contacts on both sides of the NW array. Electrical characterization of the SiNW array devices exhibits good current−voltage characteristics consistent with the SiNW morphology.



KEYWORDS: *Vertical nanowire transfer, nanowire array devices, PDMS etching, porous silicon, flexible nanowire devices*

Vertical silicon nanowire (SiNW) arrays, due to their anisotropic electronic and optical properties, large surface to volume ratios, abilities to orthogonalize light absorption and carrier transport directions and to reduce thermal conductivity by enhancing phonon scattering, are being considered as important building blocks for various applications, ranging from vertical surround-gate field-effect transistors,[1−3] biosensors,[4−6] solar cells[7−9] to thermoelectric devices.[10−12] Many of these applications desire vertical SiNW arrays to be fabricated on non-Si-based substrates in order to endow the final devices with the properties of flexibility, transparency, and lightweight.[13−15] Nevertheless, fabrication of vertical SiNW array devices on non-Si-based substrates faces three significant challenges: (1) detaching SiNW arrays with uniform length from their original fabrication substrates, typically Si wafers, while maintaining their vertical orientation; (2) attaching the detached SiNW arrays to any receiving device substrates, again retaining their vertical orientation; and (3) forming metallic contacts on both ends of the SiNWs with mechanical support and electrical insulation in between. Although a number of methods, such as dry transfer,[16,17] transfer printing methods (TPMs),[14,18,19] and water-assisted TPM,[20] have been developed to fabricate horizontal NW electronics on non-Si-based substrates, only a few methods have come close to fabricating vertical NW devices on Si- and non-Si-based substrates.[7,13,21] In one approach, vertical SiNW arrays with a low doping concentration were etched on a heavily doped Si wafer that was used as a contact, allowing the majority of the electrical resistance to occur through the SiNW layer,[7] but this method is only applicable for lightly doped NWs and cannot be used for non-Si-based substrates. In another notable approach, vertical CdS NWs were directly grown inside the pores of an anodic alumina membrane (AAM) that was formed on the surface of Al foil that automatically functioned as a metallic contact,[21] but this method is limited to only using Al foil as the substrate. An alternative approach, NW arrays were first embedded into a conductive polymer coated receiver substrate and subsequently detached from the original fabrication substrate by applying combined shear and bending forces to mechanically fracture and transfer the NW array from its original substrate to a low-cost carrier substrate while exposing the other NW side for contact,[13,22] and for which the NW vertical alignment, NW density, and the conductivity of conductive polymer need to be improved. Hence, new methods are still needed to be developed to fabricate vertical SiNW array devices with metallic contacts on both ends on arbitrary non-Si-based substrates.

Here, we report a new vertical TPM (V-TPM) that enables the fabrication of vertically aligned SiNW electronic devices with metallic contacts on both ends on arbitrary substrates, such as plastic sheets, metal foils, and glass slides. Our method essentially relies on the formation of a horizontal crack across the SiNW arrays, resulting in easy detachment of the NW arrays with uniform length from their fabrication substrates.[23] The fabrication process of the vertical SiNW array devices with this V-TPM is illustrated in Figure 1. First, vertically aligned SiNWs were formed on top of a p-type Si wafer (dopant concentration of $\sim 10^{14}$ cm^{-3}) by Ag-assisted electroless etching,[7,13,21] and a horizontal crack across the SiNWs was formed by inserting a water soaking step between two consecutive etching steps (Figure 1a).[23] The water soaking step causes the delamination and redistribution of Ag, leading to new horizontal etching pathways to form the crack.[23] Next, the SiNW array was filled with hexane diluted poly(dimethylsiloxane) (PDMS) (2:1), by spin coating, for mechanical support and electrical insulation purposes (Figure 1b), and then the PDMS was further dry etched by a plasma reactive ion etcher (a 3:1 CHF_3:O_2 gas mixture, 150 W, 50 mtorr) to expose the SiNW tips (Figure 1c). Then, metal contacts (Ti/Pd/Al: 5/200/500 nm) were deposited on the exposed SiNW tips with an electron beam evaporator after a

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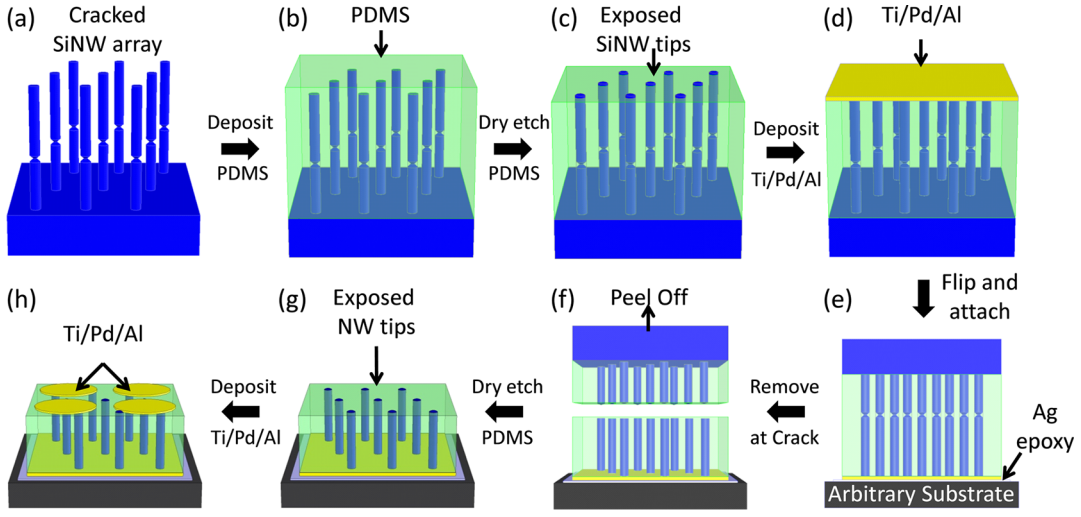

Figure 1. Schematic of the fabrication procedure for vertical SiNW array electronic devices on non-Si-based substrates with V-TPM. (a) Cracked vertical SiNW arrays are formed by inserting a water soaking step between two consecutive Ag-assisted chemical etching steps. (b) SiNWs are filled with hexane-diluted PDMS for mechanical support and electrical insulation. (c) SiNW tips are exposed after dry etching of PDMS. (d) Metal contact is deposited over the exposed SiNW tips. (e) The metal contact side of the Si wafer is attached to an arbitrary substrate with a thin layer of silver epoxy in between. (f) The vertical SiNW array is separated from the donor Si wafer at the crack location by peeling off. (g) The other side of SiNW tips is exposed after dry etching of PDMS. (h) The other metal contact is deposited on the exposed SiNW tips over a shadow mask with 300 μm diameter holes to complete the vertical SiNW array device.

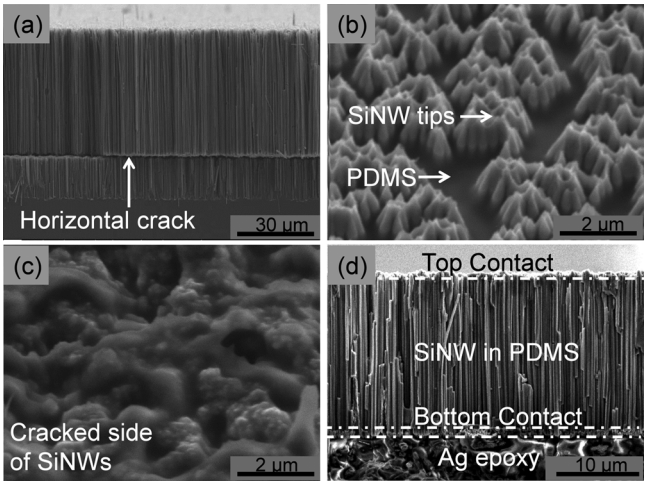

Figure 2. SEM images of (a) as-fabricated cracked SiNW array; (b) the exposed SiNW tips after the first PDMS etching; (c) the cracked end of the SiNWs embedded in PDMS right after separation from the donor Si wafer; and (d) the completed vertical SiNW array with metal contacts on both ends that are attached to an arbitrary receiver substrate by the Ag epoxy.

brief HF etching to remove the native oxide on the surface (Figure 1d). Subsequently, the sample was flipped over and attached to any arbitrary receiver substrate coated with a thin conductive silver epoxy (Ted Pella) layer (~50 μm) (Figure 1e). Once the silver epoxy was fully cured, the Si substrate was detached from the SiNW array at the horizontal crack line with the assistance of a gentle shear force, leaving behind the SiNW array embedded in PDMS on the receiver substrate (Figure 1f). The other metal contact (Ti/Pd/Al 5/200/500 nm) was deposited through a shadow mask with ~300 μm diameter holes on top of the SiNW tips after dry etching of PDMS for NW tip exposure and HF etching for native oxide removal. Finally, vertical SiNW arrays with metal contacts on both ends were fabricated on arbitrary substrates (Figure 1h).

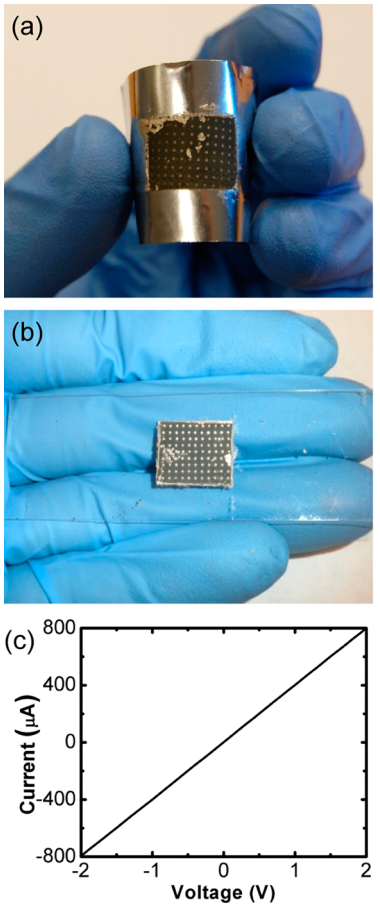

Figure 3. Optical images of vertical nonporous SiNW devices fabricated on (a) a stainless steel foil and (b) a transparent glass slide with the (c) $I-V$ curve of a typical vertical nonporous SiNW device. The linear $I-V$ characteristics demonstrate that the V-TPM forms ohmic contact to the SiNW tips on both sides of the array.

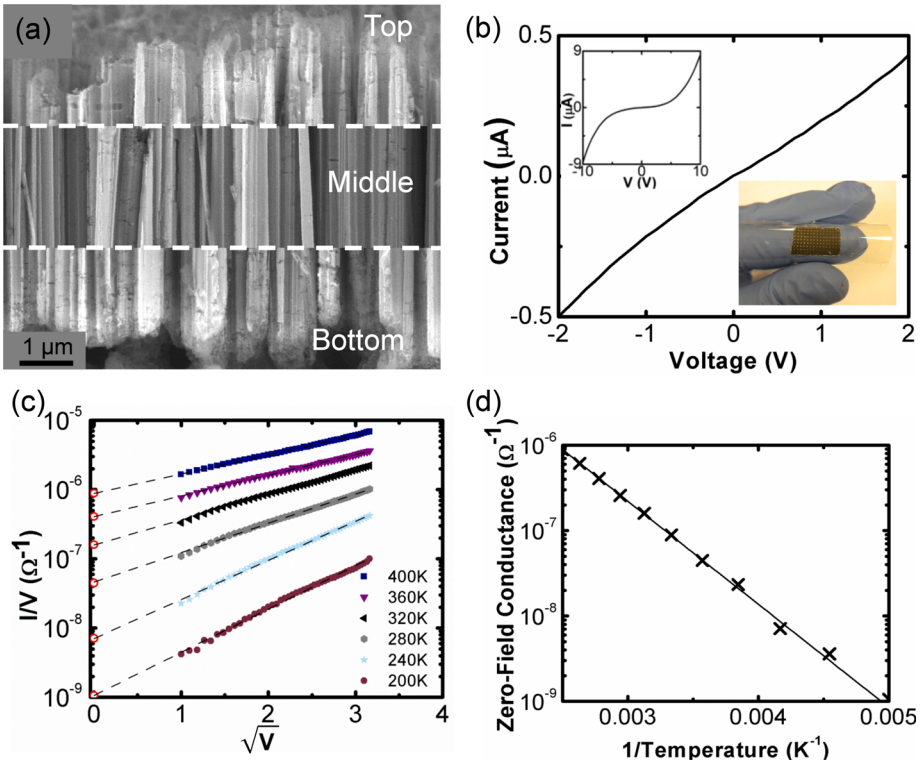

Figure 4. (a) Cross sectional SEM images of the top, middle, and bottom sections of an Ag-assisted electroless etched SiNW array clearly show that the SiNWs are porous. (b) $I-V$ curve of a vertical porous SiNW device fabricated on a plastic sheet. Insets show the device optical image and the $I-V$ curve over a large voltage range. (c) Measured conductance (I/V) of a SiNW array vs the square root of the applied voltage measured at various temperatures (symbols), which shows good agreement with the Poole–Frenkel transport relation in eq 1. The zero-field conductances (open red circles) were obtained by linearly extrapolating the measured conductance values to zero volt. (d) The zero-field conduction is plotted as a function of 1/temperature, where the slope is used to calculate the activation energy associated with releasing trapped carriers from Coulombic trap sites.

Figure 2 shows representative SEM images of SiNWs at different stages of the fabrication process as illustrated in Figure 1. Figure 2a shows that vertical SiNW arrays of uniform length (tens of μm) were etched on top of a Si wafer with a horizontal crack formed close to the base of the array (corresponding to Figure 1a). Figure 2b shows that, after PDMS infiltration and reactive ion etching (corresponding to Figure 1c), the SiNWs tips were fully exposed and ready for metal contact deposition and that PDMS nicely filled in between SiNWs, providing good mechanical support and electrical insulation. Figure 2c shows that the cracked end of the SiNW array, right after separating from the Si substrate, was covered by a thin layer of PDMS. Figure 2d shows the cross section of a final device that was composed of uniform and vertical SiNW arrays sandwiched between two metal contacts and attached to an arbitrary substrate by a conductive Ag epoxy layer (corresponding to Figure 1h).

With our V-TPM, vertical SiNW array devices were successfully fabricated over a range of non-Si-based substrates, including conductive and flexible metal foils (Figure 3a), transparent glass slides (Figure 3b), and transparent and flexible plastic sheets (inset of Figure 4b). The current–voltage ($I-V$) curves of the final devices exhibit characteristics that are similar among the various receiver substrates but different depending on the SiNW morphology. The SiNW morphology can be tuned by varying a few parameters during the etching process to reduce the excess Ag^+ ions in the etchant solution from depositing along the NW surface that generates porosity inside SiNWs. For example, nonporous SiNWs with relatively rough surfaces were fabricated by maintaining a low excess Ag^+ ion concentration in the solution throughout the etching process (e.g., adding Au on top of Ag to increase the metal's stability,[24] reducing the H_2O_2 concentration,[25,26] decreasing the etching time,[25,26] reducing the Ag thickness,[26] using a low wafer doping concentration,[26,27] and optimizing the Ag delamination step to reduce the SiNW sidewall etching). These nonporous SiNWs, as shown in Figure 3c, have linear $I-V$ curves with an average electrical conductivity value around 2.9×10^{-3} S/cm, demonstrating that our V-TPM forms good quality metal–Si contacts during the device fabrication process.

On the other hand, porous SiNWs are frequently formed during the Ag-assisted electroless etching process if the Ag^+ ion concentration in the etchant solution is not well controlled by the above-mentioned methods.[25−30] The porosity of these SiNWs is clearly shown throughout the length of the NW array in the cross-sectional SEM images in Figure 4a, where the porosity is particularly increased where an etching step is initiated (i.e., around both the NW tips), due to the initial local increase in the Ag^+ ion concentration. These porous vertical SiNW arrays fabricated by this V-TPM exhibit quasi-linear $I-V$ curves at low voltages (−2 to 2 V) but nonlinear $I-V$ curves at higher voltages (inset of Figure 4b). We believe that the nonlinear behavior under relative high voltages originates from the electron-transport properties in the porous SiNWs. Porous Si has been shown to have nonlinear $I-V$ characteristics[31−37] and resistivity values 5 orders of magnitude larger than crystalline silicon due to the depletion of free charge carriers.[31,38] Upon closer investigation of the porous SiNW

device $I-V$ curves, it was found that at higher voltages the conductance (I/V) shows an exponential dependence on the square root of applied voltage, as shown in Figure 4c, and such dependence is best described by the Poole–Frenkel relationship shown in eqs 1 and 2:

$$G(V, T) = G_o \exp\left[\frac{-E_A}{k_B T}\right] \exp\left[\frac{V}{V^*}\right]^{1/2} \quad (1)$$

$$\sqrt{V^*} = \frac{k_B T}{e} \Big/ \left[\frac{e}{\pi \epsilon d}\right]^{1/2} \quad (2)$$

Here, G is the conductance of porous Si, G_o is the conductance prefactor, E_A is the activation energy to release a trapped charge carrier from Coulombic traps, k_B is the Boltzmann's constant, T is the device temperature, V is the applied voltage, V^* is a parameter reflecting the material characteristic, e is the elementary electron charge, ϵ is the dielectric constant, and d is the length of the porous channel. The Poole–Frenkel relationship attributes the nonlinear $I-V$ characteristics to an electric-field-enhanced thermal excitation of charge carriers from Coulombic traps, for which the activation energy to release a trapped carrier is reduced with increasing electric fields, leading to the nonlinear voltage dependence.[31,32,39−41] At low voltages, the metal–porous Si contacts will exhibit a quasi-ohmic contact, corresponding to the low-voltage quasi-linear $I-V$ curves (inset of Figure 4b). The average conductivity values extracted from the $I-V$ curves between −2 V to 2 V, is 2.1×10^{-6} S/cm, which is roughly three orders of magnitude lower than the average sample in Figure 3 and five orders of magnitude lower than the conductivity calculated on the basis of the wafer property, indicating the porous nature of the SiNWs. The nonporous NWs are believed to have lower conductivity than the initial bulk wafer due to the increased surface charge carrier depletion from the rough surface inherently formed by the Ag-assisted chemical etching process.[25] Nevertheless, as the voltage is increased in the porous SiNWs, the electric field enhances the thermal excitation of charge carriers from Coulombic traps, causing the conductance (G) to increase with V in the form of $\exp(V^{1/2})$.[32,40] To confirm this behavior associated with porous SiNWs, we calculated the activation energy associated with releasing trapped carriers by the slope of the zero-field conductance values vs $1/T$ curve (Figure 4d) using the Arrhenius relation according to eq 1, where the zero-field conductances at any specified temperature were obtained by extrapolating the conductances measured under different bias to zero bias (Figure 4c, marked by the open red circles) at that temperature. As a result, the obtained activation energy is about 0.25 eV from Figure 4d and generally in the range of 0.23 − 0.32 eV, which is comparable to the 0.14–0.5 eV activation energies for bulk porous Si films formed by anodization using the same Poole–Frenkel relation.[31,32,41,42]

Our V-TPM can be also applied to axially modulated p–n SiNWs (Figure 5). The axial p–n SiNWs were fabricated by etching a p–n wafer with approximately a 10 μm thick n-type layer (dopant concentration of $\sim 10^{18}$ cm^{-3}) on top of a p-type wafer (dopant concentration of $\sim 10^{16}$ cm^{-3}). The location of the crack was controlled such that both the p and n segments exist above the crack. The axially modulated p–n SiNW array device was successfully transferred on a Kapton sheet (Figure 5b) and showed a clear rectifying behavior (Figure 5c), indicating the formation of a diode. Importantly, the rectifying $I-V$ curve remains almost the same under different bending radii (8–68 mm) of the Kapton sheet, demonstrating the good flexibility of the final vertical SiNW devices.

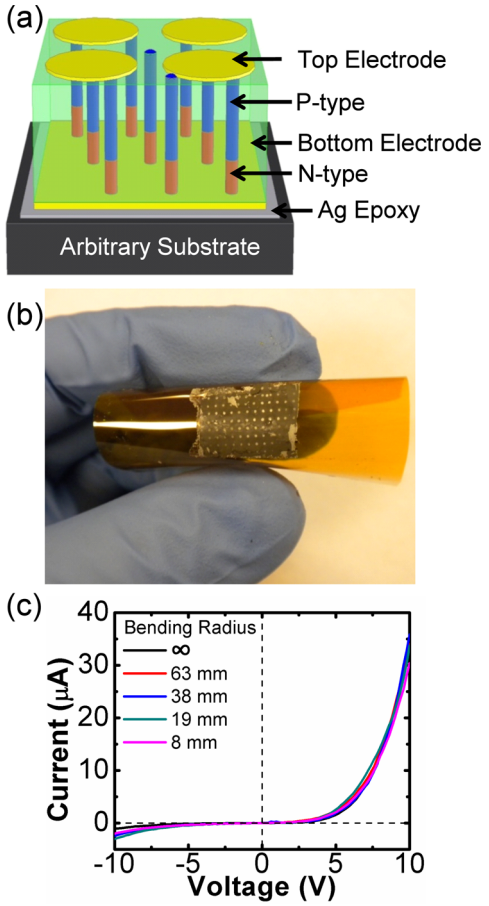

Figure 5. (a) Schematic and (b) optical image of axially modulated vertical p–n SiNW array devices fabricated on a Kapton sheet. (c) The corresponding $I-V$ curve shows nearly identical rectifying behavior under various bending radii.

In summary, we demonstrated a new V-TPM to fabricate vertically aligned SiNW array electronic devices on arbitrary substrates, including plastic sheets, metal foils, and glass slides. The V-TPM overcomes three major challenges of fabricating vertical NW devices: (1) detachment of vertically aligned SiNW arrays from Si substrates by forming horizontal cracks, (2) attachment of the vertical SiNW arrays to arbitrary substrates by using conductive Ag epoxy, and (3) formation of metallic contacts on both sides of the SiNW array by infiltrating PDMS in between SiNWs and etching the top PDMS layer to expose the SiNW tips. The $I-V$ curve characteristics of the completed vertical SiNW arrays are independent of the substrate materials but mainly depend on the porosity of the SiNWs. Nonporous SiNWs exhibit linear $I-V$ curves, demonstrating the good fabrication quality by the V-TPM. Porous SiNWs have quasilinear $I-V$ curves at low voltages and evolve to an $\exp(V^{1/2})$ dependence at higher voltages due to the Poole–Frankel effect in porous Si. The $I-V$ curves of the axially modulated p–n SiNWs exhibit clear rectifying behavior indicating the excellent control of the crack location and generality of this method TPM. We believe that our V-TPM will greatly facilitate the fabrication of large area, high density vertical SiNW devices on non-Si-based substrates for various applications.

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Notes

The authors declare no competing financial interest.

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REFERENCES

(1) Goldberger, J.; Hochbaum, A. I.; Fan, R.; Yang, P. D. *Nano Lett.* **2006**, *6* (5), 973−977.
(2) Lugstein, A.; Steinmair, M.; Henkel, C.; Bertagnolli, E. *Nano Lett.* **2009**, *9* (5), 1830−1834.
(3) Schmidt, V.; Riel, H.; Senz, S.; Karg, S.; Riess, W.; Gosele, U. *Small* **2006**, *2* (1), 85−88.
(4) Kim, D. R.; Zheng, X. L. *Nano Lett.* **2008**, *8* (10), 3233−3237.
(5) Li, Z.; Chen, Y.; Li, X.; Kamins, T. I.; Nauka, K.; Williams, R. S. *Nano Lett.* **2004**, *4* (2), 245−247.
(6) Patolsky, F.; Zheng, G. F.; Lieber, C. M. *Anal. Chem.* **2006**, *78* (13), 4260−4269.
(7) Garnett, E.; Yang, P. D. *Nano Lett.* **2010**, *10* (3), 1082−1087.
(8) Kelzenberg, M. D.; Boettcher, S. W.; Petykiewicz, J. A.; Turner-Evans, D. B.; Putnam, M. C.; Warren, E. L.; Spurgeon, J. M.; Briggs, R. M.; Lewis, N. S.; Atwater, H. A. *Nat. Mater.* **2010**, *9* (3), 239−244.
(9) Kim, D. R.; Lee, C. H.; Rao, P. M.; Cho, I. S.; Zheng, X. *Nano Lett.* **2011**, *11* (7), 2704−2708.
(10) Abramson, A. R.; Kim, W. C.; Huxtable, S. T.; Yan, H. Q.; Wu, Y. Y.; Majumdar, A.; Tien, C. L.; Yang, P. D. *J. Microelectromech. Syst.* **2004**, *13* (3), 505−513.
(11) Boukai, A. I.; Bunimovich, Y.; Tahir-Kheli, J.; Yu, J. K.; Goddard, W. A.; Heath, J. R. *Nature* **2008**, *451* (7175), 168−171.
(12) Hochbaum, A. I.; Chen, R. K.; Delgado, R. D.; Liang, W. J.; Garnett, E. C.; Najarian, M.; Majumdar, A.; Yang, P. D. *Nature* **2008**, *451* (7175), 163−167.
(13) Logeeswaran, V. J.; Katzenmeyer, A. M.; Islam, M. S. *IEEE Trans. Electron Devices* **2010**, *57* (8), 1856−1864.
(14) McAlpine, M. C.; Ahmad, H.; Wang, D. W.; Heath, J. R. *Nat. Mater.* **2007**, *6* (5), 379−384.
(15) Shiu, S. C.; Hung, S. C.; Chao, J. J.; Lin, C. F. *Appl. Surf. Sci.* **2009**, *255* (20), 8566−8570.
(16) Fan, Z. Y.; Ho, J. C.; Jacobson, Z. A.; Yerushalmi, R.; Alley, R. L.; Razavi, H.; Javey, A. *Nano Lett.* **2008**, *8* (1), 20−25.
(17) Fan, Z.; Ho, J. C.; Takahashi, T.; Yerushalmi, R.; Takei, K.; Ford, A. C.; Chueh, Y.-L.; Javey, A. *Adv. Mater.* **2009**, *21* (37), 3730−3743.
(18) Baca, A. J.; Meitl, M. A.; Ko, H. C.; Mack, S.; Kim, H.-S.; Dong, J.; Ferreira, P. M.; Rogers, J. A. *Adv. Funct. Mater.* **2007**, *17* (16), 3051−3062.
(19) Lee, C. H.; Kim, D. R.; Zheng, X. *Proc. Natl. Acad. Sci. U.S.A* **2010**, *107* (22), 9950−9955.
(20) Lee, C. H.; Kim, D. R.; Zheng, X. *Nano Lett.* **2011**, *11* (8), 3435−3439.
(21) Fan, Z.; Razavi, H.; Do, J.-w.; Moriwaki, A.; Ergen, O.; Chueh, Y.-L.; Leu, P. W.; Ho, J. C.; Takahashi, T.; Reichertz, L. A.; Neale, S.; Yu, K.; Wu, M.; Ager, J. W.; Javey, A. *Nat. Mater.* **2009**, *8* (8), 648−653.
(22) Logeeswaran, V. J.; Ombaba, M.; Katzenmeyer, A. M.; Islam, M. S. *Proc. SPIE* **2010**, 768313.
(23) Weisse, J. M.; Kim, D. R.; Lee, C. H.; Zheng, X. *Nano Lett.* **2011**, *11* (3), 1300−1305.
(24) Kim, J.; Han, H.; Kim, Y. H.; Choi, S.-H.; Kim, J.-C.; Lee, W. *Acs Nano* **2011**, *5* (4), 3222−3229.
(25) Qu, Y. Q.; Liao, L.; Li, Y. J.; Zhang, H.; Huang, Y.; Duan, X. F. *Nano Lett.* **2009**, *9* (12), 4539−4543.
(26) Zhong, X.; Qu, Y. Q.; Lin, Y. C.; Liao, L.; Duan, X. F. *ACS Appl. Mater. Interfaces* **2011**, *3* (2), 261−270.
(27) Qu, Y.; Zhou, H.; Duan, X. *Nanoscale* **2011**, *3* (10), 4060−4068.
(28) Hadjersi, T.; Gabouze, N. *Opt. Mater.* **2008**, *30* (6), 865−869.
(29) Huang, Z.; Geyer, N.; Werner, P.; de Boor, J.; Goesele, U. *Adv. Mater.* **2011**, *23* (2), 285−308.
(30) Li, X.; Bohn, P. W. *Appl. Phys. Lett.* **2000**, *77* (16), 2572−2574.
(31) Benchorin, M.; Moller, F.; Koch, F. *Phys. Rev. B* **1994**, *49* (4), 2981−2984.
(32) Benchorin, M.; Moller, F.; Koch, F. *J. Appl. Phys.* **1995**, *77* (9), 4482−4488.
(33) Burr, T. A.; Seraphin, A. A.; Werwa, E.; Kolenbrander, K. D. *Phys. Rev. B* **1997**, *56* (8), 4818−4824.
(34) Cho, K. S.; Park, N. M.; Kim, T. Y.; Kim, K. H.; Sung, G. Y.; Shin, J. H. *Appl. Phys. Lett.* **2005**, *86*, 071909.
(35) Giebel, G.; Pavesi, L. *Phys. Status Solidi A* **1995**, *151* (2), 355−361.
(36) Remaki, B.; Populaire, C.; Lysenko, V.; Barbier, D. *Mater. Sci. Eng., B* **2003**, *101* (1−3), 313−317.
(37) Zhang, Z. Y.; Jin, C. H.; Liang, X. L.; Chen, Q.; Peng, L. M. *Appl. Phys. Lett.* **2006**, *88*, 073102.
(38) Bisi, O.; Ossicini, S.; Pavesi, L. *Surf. Sci. Rep.* **2000**, *38* (1−3), 1−126.
(39) Frenkel, J. *Phys. Rev.* **1938**, *54* (8), 647−648.
(40) Zhou, X.; Uchida, K.; Mizuta, H.; Oda, S. *J. Appl. Phys.* **2009**, *105*, 124518.
(41) Zhou, X.; Uchida, K.; Mizuta, H.; Oda, S. *J. Appl. Phys.* **2009**, *106*, 044511.
(42) Yamamoto, A.; Takazawa, H.; Ohta, T. *Proc. 18th Int. Conf. Thermoelect.*, Baltimore, MD, Aug. 29−Sep. 2, 1999, pp. 428−431.

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