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Direct Growth of Nanowire Logic Gates and Photovoltaic Devices

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ABSTRACT Bottom-up nanowires are useful building blocks for functional devices because of their controllable physical and chemical properties. However, assembling nanowires into large-scale integrated systems remains a critical challenge that becomes even more daunting when different nanowires need to be simultaneously assembled in close proximity to one another. Herein, we report a new method to directly grow nanowire devices consisting of different nanowires. The method is based on the epitaxial growth of nanowires from the sidewalls of electrodes and on the matching of electrode design with synthesis conditions to electrically connect different nanowires during growth. Specifically, the method was used to grow silicon nanowire-based AND and OR diode logic gates with excellent rectifying behaviors, and photovoltaic elements in parallel and in series, with tunable power output.

KEYWORDS Direct growth of nanowire devices, epitaxial growth, nanowires, logic gates, photovoltaics

Semiconductor nanowires (NWs) synthesized by the bottom-up approach are promising building blocks for many electronic, photonic, and biosensing applications[1−9] because the chemical composition, structure, size and morphology of NWs can be precisely controlled and tuned at the nanoscale. In particular, when different NWs are integrated together, diverse functional devices, such as logic circuits and self-powered sensors, can be created.[8,9] However, in order to harness the full potential of integrating different NWs for functional devices, the NWs must be assembled and organized into hierarchical structures in wafer-scale systems. Several strategies, including flow-assisted alignment,[10] blow bubble film patterning,[11] contact printing,[12] vertical integration,[13] and electric field alignment,[14] have been developed for assembling and aligning NWs. Though useful, these methods generally cannot distinguish between different types of NWs during alignment, so that it is difficult to position different NWs in designated locations with high spatial resolution. Moreover, most of these methods require NWs to be separated from their growth substrates. As a result, the fragmented NWs are not of uniform length, making the device yield and uniformity difficult to control. The problem is especially acute for heterogeneous NWs with axially modulated doping because breakage can result in a mixture of p-type, n-type, and p-n elements on which it is challenging to position metal contacts at the desired locations. Finally, even after the successful alignment of different NWs, extensive and time-consuming fabrication processes are needed to form electrical connections between these NWs, hindering the wide application of NW devices.

Here, we report a novel and simple method for the direct growth of functional NW devices consisting of both homogeneous and heterogeneous NWs. The NWs are positioned at well-defined, predetermined locations with excellent uniformity and reproducibility. Our direct growth of nanowire devices (DGND) method is based on the epitaxial growth of SiNWs from the sidewalls of heavily doped Si electrodes and on the matching of the electrode patterns with the synthesis conditions to electrically connect different types of SiNWs during the NW synthesis step. Specifically, as shown in Figure 1a, the distances between the left electrode and the two right electrodes are different. Initially, both the top and bottom NWs grow epitaxially from the left electrode by the Au-catalyzed vapor−liquid−solid (VLS) growth mechanism.[15] The top NW stops growing once it reaches the top right electrode,[16] while the bottom NW continues to grow until it reaches the bottom right electrode, located further away. During this additional growth period, the synthesis conditions (e.g., precursor gases) can be changed to axially modulate the chemical properties of the bottom NW. For instance, an axially modulated p-i-n NW (diode) can be electrically connected with a p-type NW (resistor) with controlled spacing during the growth step (Figure 1a). The procedures of patterning electrodes and epitaxial growth of the SiNWs are described in detail in Supporting Information, Figure S1.

The scanning electron microscope (SEM) images in Figure 1b show the key features of our DGND method. First, one-sided growth of NWs from the left electrode was successfully realized, and the majority of NWs grew epitaxially along the ⟨111⟩ direction.[17,18] This one-sided growth is critical for devices made of NWs with asymmetric axial modulation because a mix of nanowires growing from opposite electrodes would disrupt the desired functionality. Second, the SiNWs between the top two electrodes (4 μm gap) have stopped growing, while those between the bottom two

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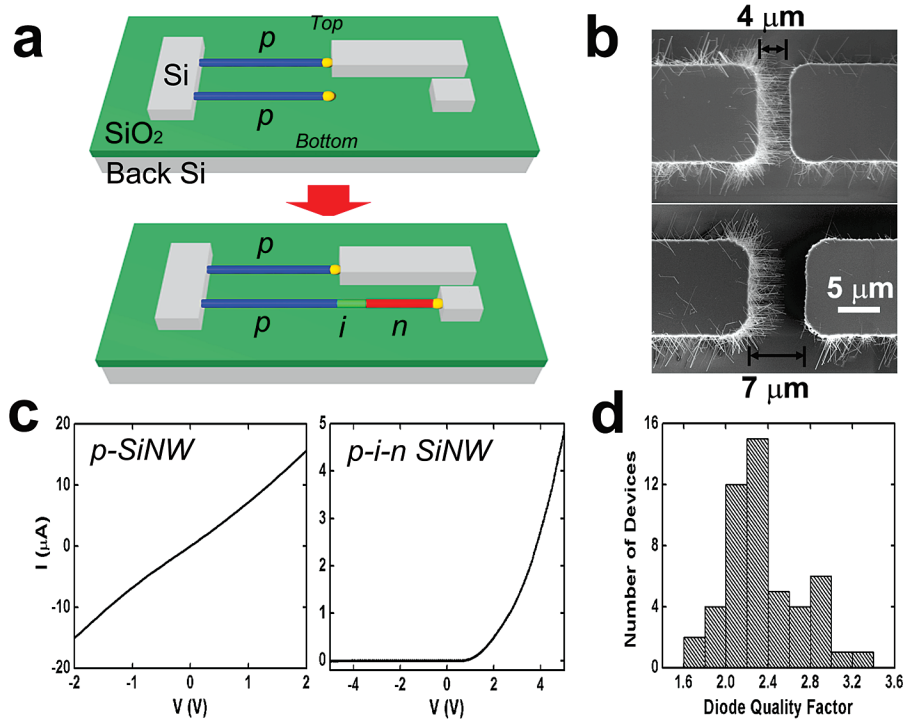

FIGURE 1. Direct growth of NW resistors and diodes. (a) Schematics illustrating the direct growth of (Top) a p-type NW resistor and (Bottom) a p-i-n NW diode; the top NW stops growing after reaching the right electrode, but the bottom NW can continue to grow until reaching its right electrode located farther away. The synthesis conditions can be changed to axially modulate the properties of the bottom NW. (b) SEM images of SiNWs bridging two electrodes of different gaps. The bottom SiNWs can continue to grow with axial modulation. (c) (Left) The $I-V$ curve of as-grown p-type SiNW resistors (4 μm long and 4000:1) shows ohmic behavior with a resistance of 139 kΩ. (Right) The $I-V$ curve of p-i-n SiNW diodes shows excellent rectifying behavior (p-type, 5 μm long and 4000:1; i-type, 0.5 μm long; n-type, 1.5 μm long and 500:1). (d) Histogram of the diode quality factor (n) summarized over 50 p-i-n SiNW diodes (p-type, 7 μm long and 4000:1; i-type, 2 μm long; n-type, 3 μm long and 500:1).

electrodes (7 μm gap) can continue to grow epitaxially with doping modulation, as illustrated in Figure 1a. Furthermore, the as-grown SiNWs were straight, with smooth surfaces and axially uniform diameters of 88 ± 15 nm when an 8 Å Au film was annealed and used as the catalyst (Supporting Information, Figure S2). Finally, p-i-n SiNWs were wet-etched in potassium hydroxide (KOH) solution to verify the success of the doping modulation. Because the etching rate for the n-type Si (500:1) is slower than that of the p-type (4000:1) and i-type SiNW segments,[6] the etched SiNWs show clear differences in diameter over differently doped segments (Supporting Information, Figure S2).

The results of the electrical characterization[19] of the as-grown SiNWs are shown in Figure 1c. First, the current–voltage ($I-V$) curve of the p-type SiNWs (4 μm long, 4000:1) was linear, indicating that ohmic contacts were formed at both interfaces between the SiNWs and Si electrodes, and that the contact quality is comparable to that previously reported for epitaxial, homogeneous SiNWs grown from sidewalls.[18,20,21] Second, the $I-V$ curve of the axially modulated p-i-n SiNWs (p-type, 5 μm long and 4000:1; i-type, 0.5 μm long; n-type, 1.5 μm long and 500:1) demonstrated well-defined reverse bias current rectification. It should be noted that both the p^+ Si electrodes (doping concentration >10^{19} cm^{-3}) and the n-type SiNW segments (500:1 atom feeding ratio of Si to P) were heavily doped to introduce a tunneling barrier to reduce the interfacial contact resistance. More than 70% out of over 200 tested p-i-n SiNW diodes showed good current rectification behavior. The diode quality factor (n), summarized over 50 SiNW diodes, had a normal distribution of 2.34 ± 0.37 (Figure 1d).[22] These results demonstrate the excellent controllability and reproducibility of our approach in growing axially modulated SiNWs between two electrodes. Finally, we fabricated p-i-n SiNW devices by sonicating these NWs, depositing them randomly onto a device substrate, and defining metal contacts by photolithography to identify the origin of the observed rectification behavior.[7] The $I-V$ curves of these p-i-n SiNWs (Figure 2a) also showed excellent rectification behavior, and their diode quality factors (n) were in the range of 2.49 ± 0.53, which is similar to those of the as-grown p-i-n SiNW diodes. This confirms that the rectifying behavior of the as-grown p-i-n SiNWs comes from the doping modulation, and not from the contact between the n region of the p-i-n SiNWs and the heavily p-doped Si electrode.

The capability of growing various types of functional NW elements, such as resistors and diodes, with simultaneous electrical connection can enable the direct manufacture of functional NW devices consisting of different electronic elements. To demonstrate these potentials, we have directly

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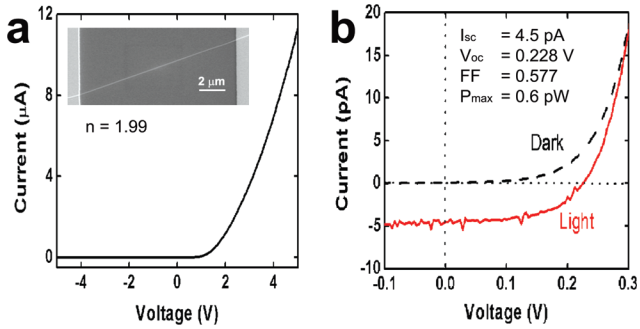

FIGURE 2. $I-V$ **curves of a p-i-n SiNW PV device fabricated by random deposition. (a) Dark** $I-V$ **curve of a p-i-n SiNW with a diode quality factor (**n**) of 1.99. The p-i-n SiNWs were sonicated off from their growth substrate and randomly deposited onto a device substrate. The device was fabricated by photolithography and metallization. (Inset) SEM image of the measured p-i-n SiNW PV device. (b) Dark and light** $I-V$ **curves of this p-i-n SiNW PV device.**

grown SiNW-based OR and AND diode logic gates. As shown in Figure 3, both logic gates consist of p-type SiNW resistors (4 μm long, 4000:1) and p-i-n SiNW diodes (p-type, 8 μm long and 4000:1; i-type, 0.5 μm long; n-type, 1.5 μm long and 500:1). For the OR logic gate (Figure 3a), the 5 V input for both V_{in1} and V_{in2} was supplied by an external power supply. When either of the input voltages was high (5 V), or both were high, the corresponding p-i-n diode was forward-biased and the output voltage V_{out} was high (logic 1) as shown in Figure 3b.[23] Likewise, for the AND logic gate (Figure 3c), the voltage inputs for V_c, V_{in1}, and V_{in2} were provided externally. Only when both inputs V_{in1} and V_{in2} for the p-i-n diodes were high (5 V), both diodes were reverse-biased and the output voltage V_{out} was high (logic 1) as shown in Figure 3d. The excellent rectifying characteristics observed for the OR and AND logic gates are comparable to those of previously reported NW-based logic gates,[9] for which the p-n junctions were realized by crossing p-type SiNWs and n-type GaN NWs. The fabrication of the crossed-NW devices not only requires locating each individual NW, but also needs time-consuming electron beam lithography to define the location of each and every metal contact. In contrast, our DGND method requires only a single photolithography step to pattern the electrodes, followed by a NW growth step. In addition, each NW circuit element can be precisely tuned by adjusting the physical and chemical properties of the NWs, such as the compositions of materials, the types of the dopants, and the doping concentrations, during the bottom-up growth process.

To further demonstrate the versatility of our DGND method, we have grown axially modulated p-i-n SiNW photovoltaic (PV) devices. NW-based PV elements have been characterized and demonstrated to have the potential to power nanoscale devices.[6,8,24,25] However, the reproducibility of fabrication of these PV devices and the ability to scale them up to meet power demands is severely limited because the fabrication typically involves expensive and time-consuming serial electron beam lithography to define metal contacts for the NWs that have been broken from their growth substrates, or complex fabrication schemes to define the top metal contacts for the vertical NW arrays.[25] Here, we have directly grown p-i-n SiNW PV devices with SiNWs of an average diameter of 88 nm, composed of 7 μm long p-type (4000:1), 2 μm long i-type, and 3 μm long n-type (500:1) Si segments (Figure 4a, Top), where the i-Si was included to reduce the leakage current in the p-n junctions.[6] The dark $I-V$ curve (Figure 4a, Bottom) showed well-defined

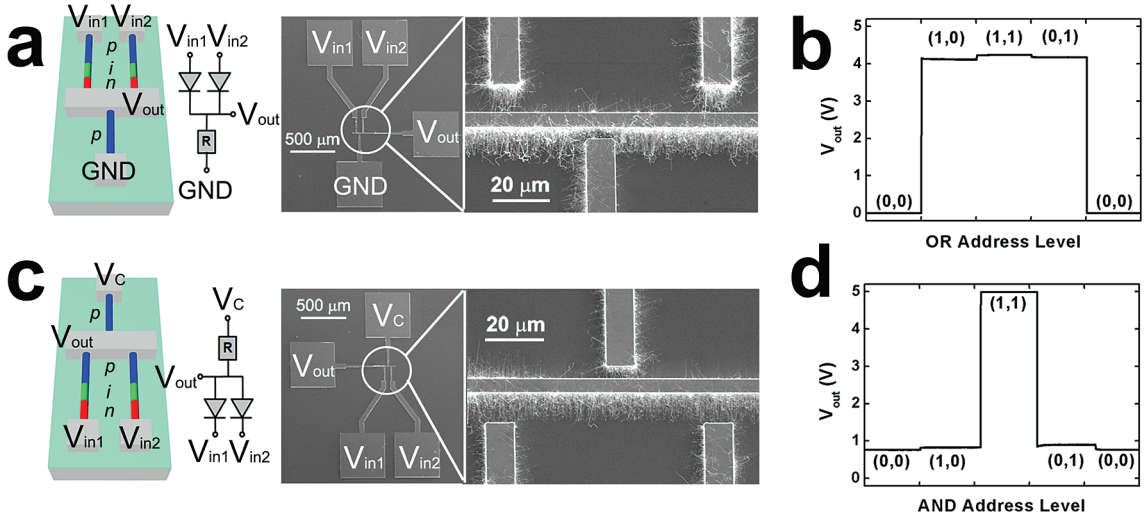

FIGURE 3. Direct growth of NW OR and AND logic gates. (a) (Left) Schematics and (Right) SEM images of an as-grown SiNW OR logic gate, which consists of two diodes and one resistor. V_{in1} **and** V_{in2} **are the two input voltages,** V_{out} **is the output voltage and GND is the grounded electrode. (b) The output voltage** V_{out} **is 1 when either** V_{in1} **and** V_{in2} **is 1, or both are 1, where logic 0 input is 0 V and logic 1 input is 5 V. (c) (Left) Schematics and (Right) SEM images of the as-grown SiNW AND logic gate, where** V_c **is the supply voltage. (d) The output voltage** V_{out} **is 1 only when both** V_{in1} **and** V_{in2} **are 1. Logic 0 input is 0 V, logic 1 input is 5 V, and the supply voltage is 5 V. A 25 MΩ external resistor was added for both OR and AND measurements to balance the diode resistance.**

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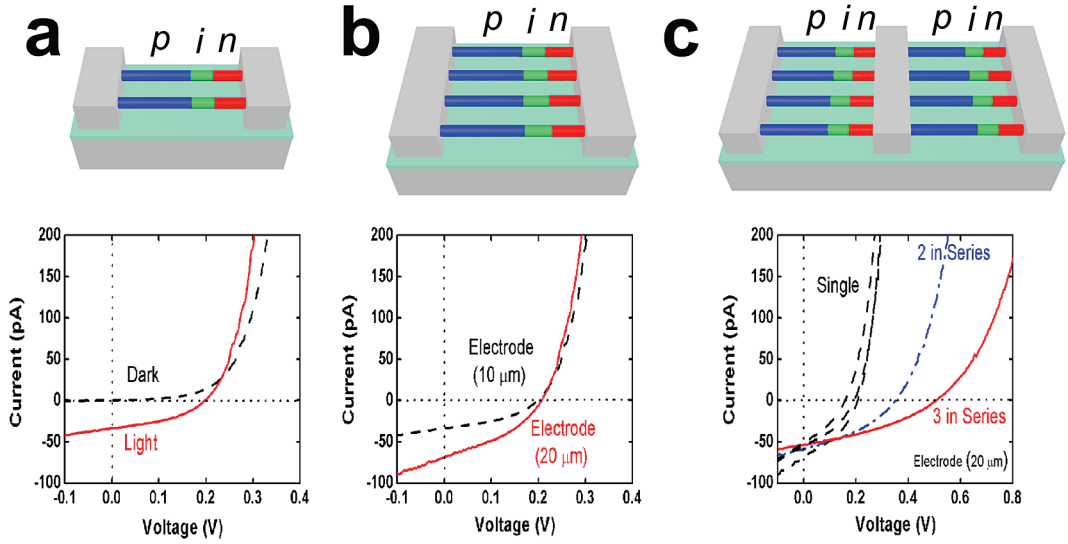

d

		a	b	c (2 in series)	c (3 in series)
Electrode Width		**10 μm**	**20 μm**	**20 μm**	**20 μm**
I_{sc}	(pA)	33.4	68.5	58.5	53.6
V_{oc}	(V)	0.196	0.208	0.352	0.508
FF	(-)	0.418	0.395	0.368	0.356
P_{max}	(pW)	2.7	5.6	7.6	9.7

FIGURE 4. Direct growth of SiNW photovoltaic devices in parallel and in series. (a) (Top) Schematics and (Bottom) dark (dashed line) and light (solid line) $I-V$ curves of the as-grown p-i-n SiNW PV elements (p-type, 7 μm long and 4000:1; i-type, 2 μm long; n-type, 3 μm long and 500:1). (b) (Top) Schematic and (Bottom) light $I-V$ curves of the SiNW PV elements with 10 μm wide and 20 μm wide electrodes respectively. Both I_{sc} and P_{max} were doubled by doubling the electrode width, which is equivalent to assembling two PV elements in parallel. (c) (Top) Schematic and (Bottom) light $I-V$ curves of the SiNW PV elements in single-, double- and tripleserial connections; the V_{oc} scaled with the number of series-connected PV elements. All electrodes are 20 μm wide. (d) Summary table of the photovoltaic properties of the as-grown SiNW PV elements in Figure 4a–c.

reverse bias rectification and a diode quality factor (n) of 2.05.[26] The photovoltaic properties of these p-i-n SiNWs were characterized under 1 sun air mass 1.5 global (AM 1.5G) illumination. The light $I-V$ measurement yielded a short circuit current (I_{sc}) of 33.4 pA, an open circuit voltage (V_{oc}) of 0.196 V, a fill factor (FF) of 0.418, and a maximum power output (P_{max}) of 2.7 pW. All the dark and light $I-V$ characteristics are comparable to those of previously reported p-i-n SiNW (ca. 250 nm diameter) photovoltaic devices fabricated by electron beam lithography.[6] Moreover, our p-i-n SiNW PV devices, when fabricated by random NW deposition and photolithography (Figure 2b), showed similar dark and light $I-V$ characteristics, suggesting that the NW PV devices grown directly over patterned electrodes are highly reliable and of high quality.

More importantly, as shown in Figure 4b,c, the p-i-n SiNW PV devices can be conveniently scaled up by integrating more PV elements in parallel and in series to provide enough power (a few nW), in principle, to drive NW- or nanotube (NT)-based electronic devices.[4,27] The parallel connection of the p-i-n SiNW PV elements was realized by doubling the width of the electrodes (Figure 4b, Top) and, as a result, both I_{sc} and P_{max} were doubled from those of the narrower electrodes under the same illumination (Figure 4b, Bottom). The parallel connection of the p-i-n SiNW PV elements was further compounded in a serial connection (Figure 4c, Top), and both V_{oc} and P_{max} scaled with the number of PV elements in series (Figure 4c, Bottom), while I_{sc} matched the lowest value of the individual PV element. The photovoltaic properties of these as-grown SiNW PV elements are tabulated in Figure 4d. Hence, in principle, the output I_{sc}, V_{oc}, and P_{max} of the SiNW PV elements can be further increased and tailored for specific applications by simply changing the electrode design. Moreover, since our approach can precisely control the properties of these PV elements during synthesis, it provides a well-controlled platform for the study and optimization of p-i-n SiNW PV elements in terms of the diameter of the SiNWs, the length and dopant concentration of the p-, i-, and n-type segments, the catalyst for the SiNW growth, and surface passivation of the SiNWs.

In summary, we have demonstrated a novel and simple DGND method to directly grow NW-based functional devices consisting of both homogeneous and axially modulated heterogeneous NWs with controlled spacing and electrical

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connections. With the DGND method, we have successfully grown several NW-based devices, including resistors, diodes, OR and AND diode logic gates, and scalable PV elements with high uniformity, reproducibility, and performance comparable to that of similar devices fabricated by severing NWs from their growth substrates. In addition, the DGND method can be extended to grow NW devices consisting of various materials, such as Si/SiGe, GaAs/GaP, and InAs/InP heterogeneous nanowires. As such, even more sophisticated functional devices can be realized by integrating diverse NWs during the growth step to realize large-scale NW-based electronic, photonic, and biosensing applications.

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Supporting Information Available. Description of detailed materials and methods used in this work. This material is available free of charge via the Internet at http://pubs.acs.org.

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