A SPICE Model of Resistive Random Access Memory for Large-Scale Memory Array Simulation

Haitong Li, Peng Huang, Bin Gao, Bing Chen, Xiaoyan Liu and Jinfeng Kang

***Abstract*—A SPICE model of oxide-based resistive random access memory (RRAM) for DC and transient behaviors is developed based on the conductive filament evolution model and is implemented in large-scale array simulation. The simulations of one transistor-one resistor RRAM array up to 16 kb with wire resistance (R_{wire}) and capacitance (C_{wire}) indicate that: 1) Resistance-capacitance delay during RESET and leakage current during SET have significant impact on write operations. 2) With array size enlarging, the power dissipation increases during RESET but decreases during SET. 3) The increased R_{wire} and C_{wire} lead to the degradation of high resistance state and the fluctuation of low resistance state, respectively.**

***Index Terms*—Circuit simulation, memory array, power dissipation, resistive random access memory (RRAM), SPICE model.**

I. Introduction

METAL-oxide bipolar resistive random access memory (RRAM) has been extensively studied as one of the most promising candidates for the next generation nonvolatile memory technology [1], [2]. Different from the operation of traditional charge-based memories, the write/read operation of novel resistive-based memories can be significantly influenced by the circuit-level factors such as operation modes and interconnect [1], [3]. For the design and optimization of RRAM-based memory circuits, an array-embeddable SPICE model is needed for the efficient simulation of large-scale array. Several models have been developed to describe resistive switching behaviors [4], [5]. However, these previous models are mainly based on equivalent circuits consisting of multiple components such as controlled sources. The complexity in terms of computation resources dramatically increases as the simulated array size expands. Therefore, these models may be inefficient for the analyses of large-scale array performance. In this letter, a SPICE model of RRAM aimed at efficient simulation of large-scale RRAM array is developed based on the conductive filament (CF) evolution model [6]-[8]. By employing Verilog-A [9] to behaviorally define RRAM cell as a two-terminal resistive element, the developed SPICE model can be easily invoked in HSPICE [10] simulation of large-scale array with efficiency and accuracy. Furthermore, the SPICE model is implemented in HSPICE to evaluate the performance of one transistor-one resistor (1T-1R) RRAM array up to 16 kb, including power dissipation, resistance-capacitance (RC) delay and the impact of interconnect wire resistance (R_{wire}) and wire capacitance (C_{wire}) on write operation.

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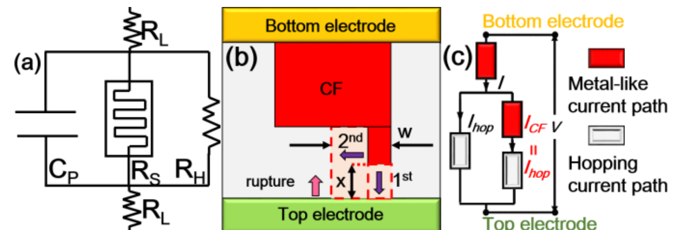

Fig. 1. (a) Equivalent circuit of RRAM cell composed of resistive switching element and parasitic elements. (b) Schematic of conductive filament evolution. (c) Equivalent circuit of resistive switching element modeling the metal-like and hopping current paths.

II. SPICE Model of RRAM

The SPICE model is developed based on the CF evolution model [6]-[8] by defining a two-terminal equivalent circuit of RRAM cell composed of the resistive switching (RS) element and parasitic RC elements, as shown in Fig. 1(a) and (b). To establish the equivalent I-V relationship with RS resistance, the CF and gap region are modeled as metal-like and hopping current paths respectively, as shown in Fig. 1(c). The nonlinear hopping current (I_{hop}) and current through CF (I_{CF}) associated with gap distance (x) and CF width (w) can be calculated [6] as:

$$I_{hop} = I_0\left(\pi w^2/4\right)\exp\left(-x/x_T\right)\sinh\left(V_{gap}/V_T\right) \quad (1)$$

$$I_{CF} = \pi w^2 V_{CF}/4\rho\left(x_0 - x\right) \quad (2)$$

where x_T (~0.4 nm) and V_T (~0.4 V) are the characteristic length and voltage in hopping, respectively. V_{gap} and V_{CF} are the voltage over the gap region and CF region, respectively. x_0 is the initial value of gap distance. The key variables are x and w, as indicated in Fig. 1(b). The inherent switching process is described by their evolving speed together with the impact of temperature (T) [6]:

1) SET Process: two-step extension of CF

$$dx/dt = af\exp\left(-(E_a - \alpha_a ZeE)/k_B T\right) \quad (3)$$

TABLE I
PARAMETER DESCRIPTIONS OF EQUATIONS AND DEVICE/ARRAY

Parameters And Values		Descriptions
I_0	10 μA/nm^2	hopping current density in the gap region
ρ	19.64 μΩ·m	resistivity of the CF
a	0.25 nm	distance between adjacent oxygen vacancy (V_O)
f	10^{13} Hz	vibration frequency of oxygen atom in V_O
E_a	1.2 eV	average active energy of V_O
E_h	1.0 eV	hopping barrier of oxygen ion (O^{2-})
E_i	1.2 eV	energy barrier between the electrode and oxide
α_a & α_h	0.75 nm	enhancement factor in lower E_a & E_h
γ	1.5	enhancement factor of external voltage
Z & e	1 & e	charge number & unit charge
Δw	0.5 nm	effective CF extending width
ΔE_r	0.8 eV	relaxation energy during recombination
R_{th}	5×10^5 K/W	effective thermal resistance
R_H	200 MΩ	parasitic resistance between electrodes
R_L	20 Ω	parasitic contact resistance of electrodes
C_P	20 fF	parasitic capacitance between electrodes
V_{TH0}	0.72 V	zero-bias threshold voltage of NMOS
C_G	1.42 fF	gate capacitance of NMOS
C_{GS}/C_{GD}	0.28 fF	overlap capacitance of NMOS
R_{wire}	12.78 Ω	wire resistance in the 1T-1R array [16]
C_{wire}	0.046 fF	wire capacitance in the 1T-1R array [16]

$$dw/dt = \left(\Delta w + \Delta w^2/2w\right) f \exp\left(-(E_a - \alpha_a ZeE)/k_B T\right) \quad (4)$$

2) *RESET Process: the slowest of three rupture processes*

$$dx/dt = af \exp\left(-\left(E_i - \gamma ZeV\right)/k_B T\right) \quad (5)$$

$$dx/dt = af \exp\left(-E_h/k_B T\right)\sinh\left(\alpha_h ZeE/k_B T\right) \quad (6)$$

$$dx/dt = af \exp\left(-\Delta E_r/k_B T\right) \quad (7)$$

$$T = T_0 + IVR_{th}. \quad (8)$$

E is the electric field in the gap region and T_0 is ambient temperature. The SPICE model is finally set up by defining I-V relationship through RS cell based on x and w together with T. The parameter descriptions of both the equations above and the device and array are shown in Table I.

We construct a typical 1T-1R configuration in HSPICE as an RRAM cell in series with an NMOS transistor. A memory array can then be simulated using our compact model for the cell [6] and the BSIM3v3 [11] model for the NMOS. The simulated DC I-V curves of this 1T-1R configuration during SET/RESET are shown in Fig. 2(a) and Fig. 2(b), respectively. These I-V curves are similar to those reported in [1], [12]-[14]. In our previous work [6], we had validated our compact model by comparing its predictions with I-V curves of RRAM cells measured using a current limiter. In this work, we do not have access to individual elements to repeat such a direct validation. Multi-level cell (MLC) operation is simulated by modulating either the gate voltage (V_G) on transistor during SET or maximum voltage of forward DC sweep (V_{stop}) during RESET. Besides, based on the extracted model parameters, the snapback phenomenon measured in 1T-1R cell [15] can be reproduced as an intrinsic I-V behavior, as shown in Fig. 2(c). This snapback effect can be revealed by the simulated time-domain voltage relationship between applied voltage (V_{APPL}) and the voltage merely over RRAM (V_{RRAM}), as shown in Fig. 2(d). During voltage sweep, V_{RRAM} equally increases with V_{APPL} since the MOSFET is biased in linear region and the resistance ratio between RRAM and MOSFET is large enough. When V_{RRAM} exceeds SET voltage, RRAM cell is switched to

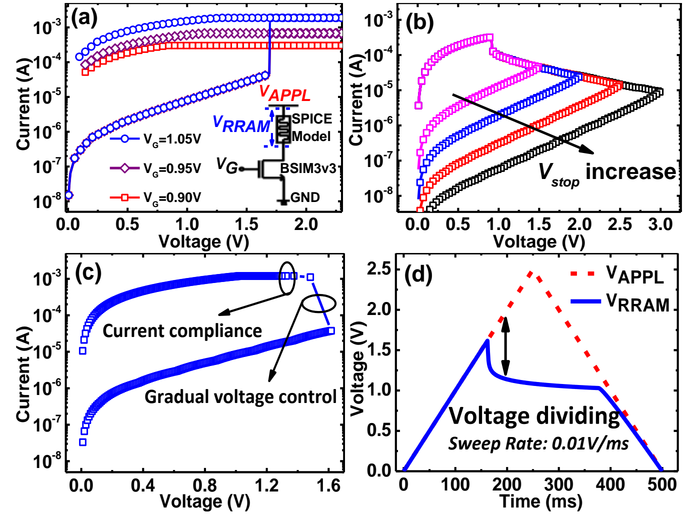

Fig. 2. Simulated DC I-V curves (a) during SET and (b) during RESET of 1T-1R cell, with V_G and $Vstop$ changing to perform MLC operation. The inset of (a) shows 1T-1R architecture. (c) Simulated intrinsic I-V curve of RRAM device in 1T-1R architecture. (d) Simulated time-domain voltage relationship between V_{RRAM} and V_{APPL} during DC sweep.

low resistance state (LRS) and meanwhile MOSFET is driven towards saturation region. Thereby the concurrence of a decrease in V_{RRAM} and a sharp increase in the current during SET leads to the snapback phenomenon of I-V curve.

III. ARRAY SIMULATION

The configuration of the 1T-1R array including parasitic effect of the interconnect R_{wire} and C_{wire} [16]-[17] is schematically shown in Fig. 3(a). All 1T-1R cells in the same column share the same vertical bit line (BL) and source line (SL) to perform bidirectional access by applying SET/RESET pulse signals, together with the horizontal word line (WL) to control the selected transistor [18]. The following simulations are based on the worst case scenario: the selected cell is located at the farthest corner and the other cells are in LRS [3]. The control voltage applied on the selected WL (V_{WL}) during SET is different from that during RESET, and bidirectional operation is performed with different pulse operation signals for SET/RESET, as shown in Fig. 3(a). The simulations show that the maximum current (I_{MAX}) of the selected cell decreases with array size, indicating that the increase in leakage current results in the degradation of gate-source voltage (V_{GS}) of the selected transistor, as shown in Fig. 3(b). Accordingly, the parasitic RC delay increases dramatically during RESET with array size, as shown in Fig. 3(c). The RC delay in the array is more significant during RESET than during SET, since the initial larger current flow in RC network leads to a larger latency feedback. Above results indicate that reducing the leakage current during SET and the RC delay during RESET is critical to enhance the array performance, especially for large-scale array. The average dynamic power dissipation during a 100 ns pulse operation period is also simulated, as shown in Fig. 3(d). With array size enlarging, the average power dissipation decreases during SET due to the degraded V_{GS} and I_{MAX} of the selected cell whereas increases during RESET due to the increased voltage drop along signal lines. Besides, the average power dissipation is associated with the V_{WL}. Furthermore, as

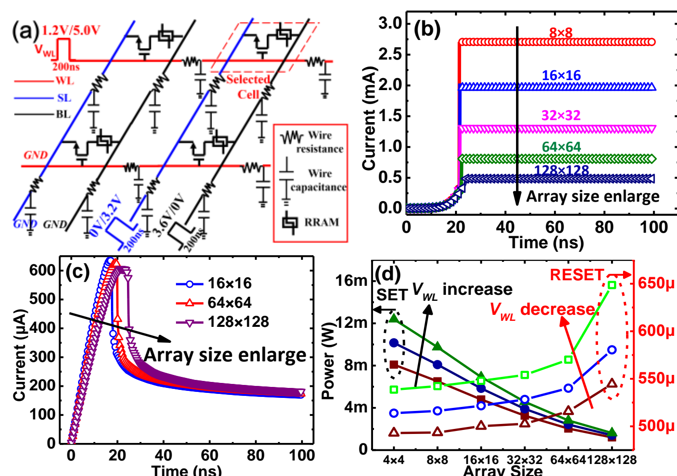

Fig. 3. (a) Diagram of 1T-1R array configuration. Transient response during (b) SET operation and (c) RESET operation of 1T-1R array, with the array enlarging from 8×8 to 128×128. (d) Simulated average dynamic power dissipation with V_{WL} changing during write operation of varisized arrays.

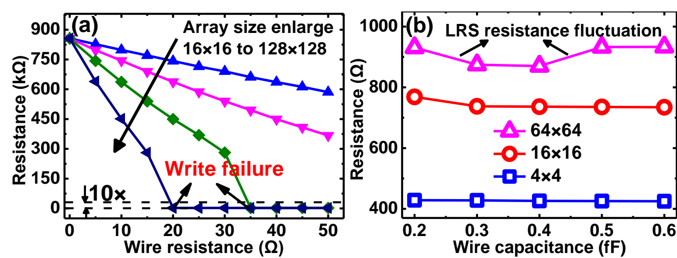

Fig. 4. Interconnect impact of (a) wire resistance on HRS resistance and (b) wire capacitance on LRS resistance during write operation, with the array size enlarging. The simulated interconnect impact manifests the critical role played by interconnector in reliability issues.

one of critical reliability issues [1], interconnect impact on 1T-1R array is studied by simulating the consecutive read-after-write operation with R_{wire} and C_{wire} changing. The degraded high resistance state (HRS) with R_{wire} after write operation implies the reduced access voltage with R_{wire} due to an increase in the voltage drop along signal lines. Also, the leakage current through unselected cells results in the V_G degradation of the selected transistor, which further leads to an increase in turn-on resistance of transistor and, therefore, a decrease in access voltage. Additionally, this degradation will be steeper leading to a write failure in the 16 kb array, as shown in Fig. 4(a). The results also reveal that the impact of C_{wire} on LRS resistance fluctuation will become significant in the large-scale array. As shown in Fig. 4(b), the C_{wire}-induced LRS resistance fluctuation in the 64×64 array is larger than that in 4×4 array. With C_{wire} increasing, the dominant signal line along which C_{wire} has more obvious impact on pulse voltage changes from the BL to the WL, which first results in a decrease and then an increase in LRS resistance after pulse operation. Reducing interconnect effect is critical to the reliable operations in the large-scale RRAM array, since the deviation from target resistance is detrimental to write reliability and read margin, especially for MLC design.

IV. Conclusion

A SPICE model of oxide-based RRAM has been developed for large-scale memory array simulation. The developed SPICE model can reproduce both extrinsic and intrinsic DC behaviors of RRAM in 1T-1R cell and the transient responses in large-scale array. The critical behaviors of the large-scale array such as power dissipation, RC delay, and read/write reliability can be simulated by HSPICE. The developed SPICE model can be applied in single-level and multi-level design and reliability verification of large-scale RRAM array and other RRAM-based function devices.

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