2D Molybdenum Disulfide (MoS_2) Transistors Driving RRAMs with 1T1R Configuration

Rui Yang[1,*], Haitong Li[1], Kirby K. H. Smithe[1], Taeho R. Kim[2], Kye Okabe[1],
Eric Pop[1,2], Jonathan A. Fan[1] and H.-S. Philip Wong[1,#]
[1]Department of Electrical Engineering, [2]Department of Materials Science and Engineering,
Stanford University, Stanford, CA 94305, USA
emails: [*]ruiy@stanford.edu, [#]hspwong@stanford.edu

***Abstract*—**We demonstrate the first 1-transistor-1-resistor (1T1R) memory cell using the atomically thin molybdenum disulfide (MoS_2) field-effect transistor (FET) and resistive random access memory (RRAM). This 1T1R demonstration realizes a key milestone for tight integration of memory with logic in a monolithic 3D integrated chip. The monolayer MoS_2 is grown by chemical vapor deposition (CVD), suitable for wafer-scale fabrication. The MoS_2 FETs have ON-state current of 190 μA/μm at $V_D = 2.5$ V, showing strong driving capability for RRAM. Metal-oxide RRAMs are fabricated at low process temperature, compatible with MoS_2 FET fabrication. 1T1R measurements show higher resistances, and less resistance and voltage variation compared with measurements using only the RRAM. The multiple resistance states obtained for pulsed reset measurements show promise for in-memory computing and neuromorphic computing applications.

I. Introduction

Two-dimensional (2D) MoS_2 FET is a promising candidate for monolithic 3D integrated circuits because the MoS_2 can be transferred and patterned at low temperatures, and it is atomically thin, providing excellent electrostatic control for scaling down to sub-10 nm gate lengths [1]. Metal-oxide RRAM is a strong candidate for future storage class memory [2-5]; in addition, RRAMs are fabricated at low temperatures and are suitable as on-chip memory for in-memory computing and neuromorphic computing [6-10]. For RRAM integration, access transistors or selectors are needed to suppress the sneak path leakage currents. 1T1R structure based on 1D carbon nanotube (CNT) FETs and RRAMs have been demonstrated [11]. An alternative method using 2D MoS_2 as the FET is advantageous because monolayer MoS_2 have larger band gaps and therefore MoS_2 FETs can achieve lower off-state current. The active device layer is also very thin so nanoscale vias can be used to connect the FETs with other layers toward a 3D chip with multiple logic and memory layers [12].

Here we demonstrate the first 1T1R structure using MoS_2 FETs and HfO_x oxygen-vacancy RRAMs. The MoS_2 FETs successfully drive the RRAMs, showing multiple cycles of set and reset, reset current as low as 50 μA, set/reset voltages < ±1.5 V, and large memory window over 10^4. Compared with measurements using only the RRAM (1R operation), 1T1R measurements show higher resistances which will result in lower leakage when integrated into an array, and less variation in resistance and set/reset voltages. We achieve multi-valued low resistance state (LRS) through control of the compliance current set by the FET. Multi-level high resistance state (HRS) is obtained using pulsed reset measurements.

II. Fabrication Process

Fabrication starts with CVD growth of monolayer (1L) MoS_2 on 300 nm SiO_2/Si substrate, using sulfur and MoO_3 as precursors [13], a process optimized to grow continuous 1L MoS_2 films with high mobility [14]. Electron beam lithography (EBL) defines the contacts to MoS_2, followed by e-beam evaporation of 20 nm Au. Then Ti (2 nm)/ Au (20 nm)/ Pt (15 nm) is deposited after EBL as the bonding pads to MoS_2 FETs and the bottom electrode (BE) of the RRAMs. Next, 5 nm of HfO_x is grown by atomic layer deposition (ALD), followed by EBL and sputter deposition of TiN (20 nm) and Pt (10 nm) as RRAM top electrode (TE). An optional 10-20 nm of HfO_2 or Al_2O_3 is grown with ALD, which together with the 5 nm HfO_x grown previously for RRAM serves as the dielectric for top gate (TG) of MoS_2 FETs. Finally, EBL defines the TG of the MoS_2 FETs. This 1T1R structure is part of the monolithic integration of logic and memory [Fig. 1 (a)], and the 1T1R structure we fabricate is shown in Fig. 1 (b), with the images of the cross sections shown in Fig. 1 (c) and 1 (d). While we use the as-grown MoS_2 film here, the growth process could be decoupled from the rest of the fabrication process through wafer-scale transfer processes of 2D materials [15]. The fabrication temperature for the 1T1R structure does not exceed 200 ºC. The maximum device layer thickness is 72 nm, measured from BE to TE of the RRAM region. The thickness of the RRAM stack (TE+HfO_x+BE) could be further scaled down to 25 nm [11,16,17], allowing nanoscale inter-level vias (ILVs). Another method of achieving dense integration is to use 3D vertical RRAM (VRRAM) array with 1T-nR configuration [3], with simulation shown in following sections. Fig. 2 (a) shows the optical images of a typical fabricated 1T1R memory cell with top-gated MoS_2 FETs. Fig. 2 (b) shows the CVD MoS_2 film, and the Raman spectrum in Fig. 2 (c) confirms that the MoS_2 is monolayer MoS_2.

III. RRAM Characterization

We first characterize the performance of the RRAMs using 1R operation, by probing directly on the TE and BE electrodes shown in Fig. 2, to verify that the RRAMs perform well and for comparison with later 1T1R operations. Fig. 3 shows the forming process, followed by set and reset operations for 42 cycles on a crossbar RRAM structure, showing typical memory characteristics for HfO_x-based RRAM [2-5]. The median set and reset voltages are 1.18 V and -0.9 V (Fig. 4). The DC sweeps (Fig. 3) show that the median HRS and LRS resistances

have ratio of ~148 (Fig. 5). The measured retention time at 125 ºC up to 10^4 seconds shows stable resistance states (Fig. 6).

IV. 1T1R Characterization

To integrate an array of 1T1R memory cells into a 3D memory system, we need every 1T1R cell to be individually addressable, and the MoS_2 access FETs must operate at low voltages, thus we have fabricated top-gated MoS_2 FETs. For 1T1R measurement, voltage is applied to TE, with source (S) grounded, drain (D)/BE floating, top gate voltage is applied at TG, and the back gate voltage (V_{BG}) is applied on Si to tune the top-gated FET characteristics. Fig. 7 shows the I_D-V_{DS} characteristics of a top-gated MoS_2 FET with S electrode grounded, and current saturation is observed. By applying positive V_{BG}, we electrically dope the MoS_2 channel and lower the contact resistances, and achieve current drive of ~190 μA/μm [Fig. 7 (b)]. High current drive of the MoS_2 FET in its ON-state is desirable as it allows the use of smaller width FET. Fig. 8 shows the I_D-V_{TG} curves (for various V_{BG}) of another MoS_2 FET, which turns ON and OFF at V_{TG} = ±2 V, with ON/OFF ratio = 10^6.

Fig. 9 shows 1T1R measurement for 100 cycles of set and reset, using the MoS_2 FET shown in Fig. 7. We effectively set and reset the RRAM while using the MoS_2 FET to set the current compliance. The distribution of the set and reset voltages for the 100 cycles of measurements is shown in Fig. 10. The median set voltage is 1.04 V, and reset voltage is -1.48 V, with smaller variation compared to those for 1R measurements. We perform pulsed measurements using 1T1R configuration (Fig. 11). Fig. 12 summarizes the distribution of the HRS and LRS resistances from pulsed measurements in Fig. 11, the resistance ratio from the median HRS and LRS resistances is ~93, and the ratio is ~10.3 if we include the tails in the distribution (worst case). The 1T1R results (Fig. 11 and Fig. 12) are better than the 1R results (Fig. 5) because: (1) the LRS and HRS resistance values are both higher for 1T1R, and this could result in smaller leakage current and thus less energy consumption when integrated into an array; and (2), for 1T1R configuration, the standard deviation (σ) of resistances normalized to the mean value (μ) is 31% (HRS) and 46.5% (LRS), and these are smaller than the corresponding values of 57.9% (HRS) and 53.0% (LRS) for 1R operation, due to better control of the current compliance.

We vary the V_{TG} and measure the 1T1R set and reset properties. When we decrease V_{TG} from 1 V to -1 V (Fig. 13), the set current generally decreases, due to higher resistance of the MoS_2 FETs, and the 1T1R operation fails to work properly if $V_{TG} \leq$ -1 V. The set and reset voltages at different V_{TG} are summarized in Fig. 14, showing that the absolute value of the reset voltage decreases with increasing V_{TG}. This is because the resistance of the FET acts as a voltage divider with the RRAM resistance, which is also explained in Fig. 15 (c)-(d). Fig. 15 (a)-(b) show that the LRS resistance decreases with larger V_{TG}. This occurs because larger V_{TG} results in lower FET resistance, which sets higher current compliance during set operation, leading to lower LRS resistance.

While we have shown that the resistance values of 1T1R operation is generally higher than 1R operation, it would be interesting to explore whether multiple resistance states could be achieved using the same 1T1R cell, which is important for electronic synapse applications. Reset measurements using a pulse train for both 1R and 1T1R operations achieve multiple levels of reset resistances for different pulse number and pulse voltages (Fig. 16). Using 1T1R configuration, we can achieve higher resistance values up to 350 MΩ resulting in HRS/LRS ratio > 10^4 [Fig. 16 (c)], compared to 13 MΩ using 1R measurement [Fig. 16 (a)]. Further, smaller resistance variation is observed from 1T1R measurements than with 1R measurements, consistent with results shown earlier. Multilevel resistances show the promise of the 1T1R cell for electronic synapse and neuromorphic computing applications.

We further evaluate the potential of building high-density 3D 1T-nR VRRAM arrays [3]. One of the key constraints for 3D VRRAM array size is the driving capability of the select pillar transistor [Fig. 17 (a)]. These FETs must provide enough drive current for the cell programming current plus the total leakage current during write operations. We incorporate the measured MoS_2 FET and HfO_x RRAM characteristics into full-size 3D array circuit simulations using HSPICE, and obtain the drive current requirement as a function of vertical layer number. "Taller" 3D arrays require larger drive current to ensure successful write operations [Fig. 17 (b)]. From the measured MoS_2 FET characteristic, we find that W/L = 1, 2 and 4 could already drive multiple device layers. Although our FET has $W/L \approx 50$, the width of the FET could be scaled down while still driving the RRAMs. Our MoS_2 FETs can thus help achieve high-density 3D memories with good driving capabilities.

V. Conclusions

In summary, we successfully demonstrate the first 1T1R structure using monolayer CVD MoS_2 FETs and HfO_x-based RRAM. Stable 1T1R operation for multiple cycles at low voltages is achieved. Further, multiple resistance levels of the 1T1R memory cells are demonstrated. The entire FET and RRAM fabrication process is performed below 200 ºC. This demonstration paves the way toward a technology platform that integrates memory with logic in a monolithic 3D computing system for in-memory and neuromorphic computing.

Acknowledgment

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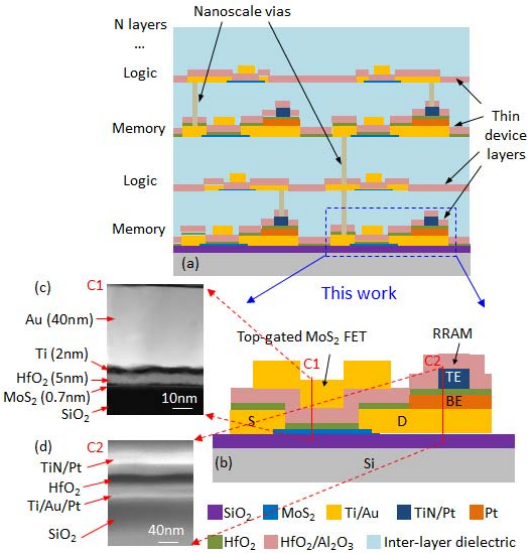

Fig. 1. (a) Illustration of the 3D monolithic integration of memory and logic layers, where the memory cells are 1T1R cells, and logic is made of 2D FETs. (b) The 1T1R structure we have accomplished that fits into the 3D integration. (c) Transmission electron microscopy (TEM) image of the cross section of the MoS_2 FET (C1). (d) Scanning electron microscopy (SEM) image of the RRAM cross section (C2).

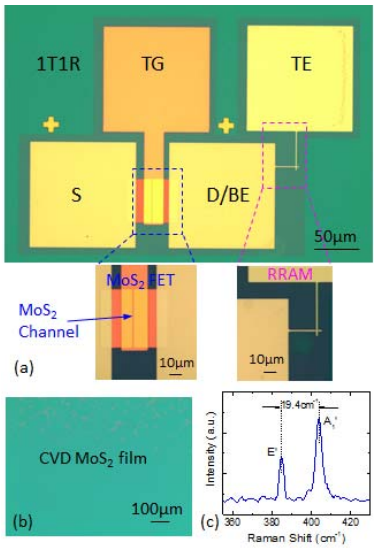

Fig. 2. (a) Optical image a typical top-gated MoS_2 1T1R memory cell, with the zoom-in images of the MoS_2 FET and RRAM regions. The MoS_2 FET has L=1 μm, W= 50 μm, and the RRAM has a switching area of 1 μm^2. (b) Optical image of a CVD MoS_2 film. (c) Raman spectrum of the monolayer MoS_2.

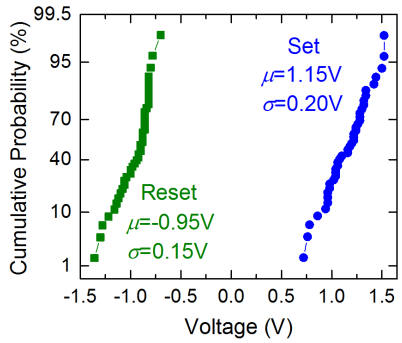

Fig. 4. Distribution of set and reset voltages for successive DC I-V sweeps as shown in Fig. 3, for 1R operation.

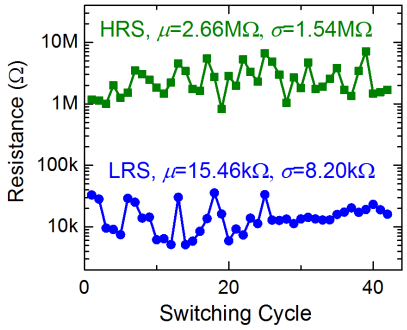

Fig. 5. The resistances of the RRAM at HRS and LRS for the 42 cycles of set and reset using DC sweeps shown in Fig. 3.

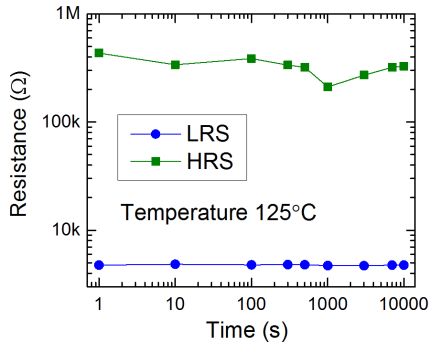

Fig. 6. Retention measurement for the RRAM with switching area of 1 μm^2 using 1R configuration, measured for 10^4 seconds at 125 ºC.

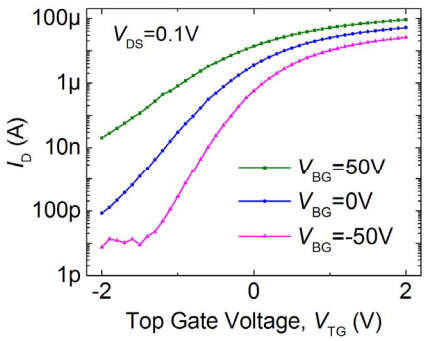

Fig. 8. I_D-V_{TG} curves of another top-gated MoS_2 FET with W=50 μm, and L=1 μm, and top-gate dielectric of 5 nm HfO_2, measured at different V_{BG}.

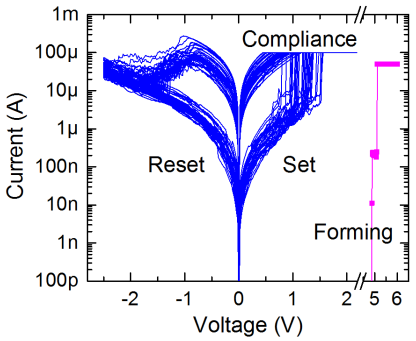

Fig. 3. DC I-V sweeps of the RRAM only (1R operation) without using MoS_2 FET. The device shows forming at ~5 V. Shown here are 42 cycles of set and reset cycles. The compliance current during set operation is 100 μA, and gradual reset is observed. The switching area is 1 μm^2.

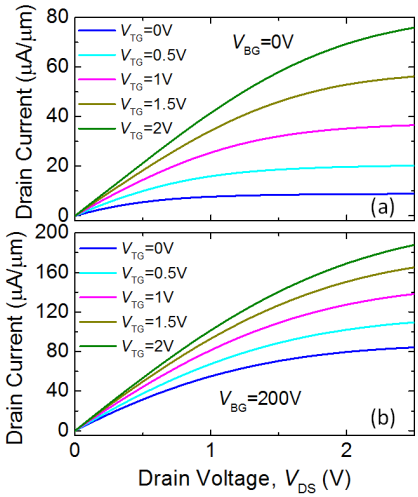

Fig. 7. I_D-V_{DS} characteristics of a top-gated MoS_2 FET with W=50 μm, and L=1 μm, and top-gate dielectric of 5 nm HfO_2, measured at different top gate voltages (V_{TG}), for (a) V_{BG}=0 V, and (b) V_{BG}=200 V.

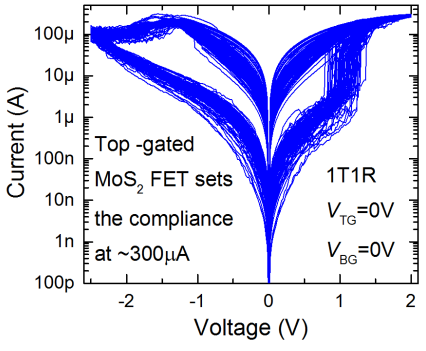

Fig. 9. 1T1R measurement using the top-gated MoS_2 FET shown in Fig. 7, for 100 cycles of set and reset. The MoS_2 FET has 5 nm HfO_2 as top gate dielectric, with W=50 μm, and L=1 μm.

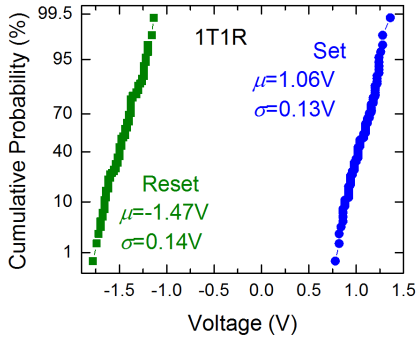

Fig. 10. Distribution of set and reset voltages during 1T1R operation for the DC sweep measurements shown in Fig. 9, showing good uniformity.

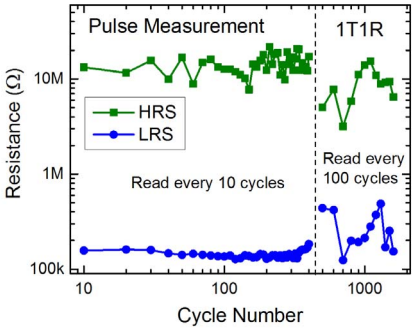

Fig. 11. Pulse measurements using 1T1R configuration for the same device in Fig. 9, using pulse width of 200 ns and V_{TG}=0 V. The HRS/LRS resistance ratio is 93 from the median values.

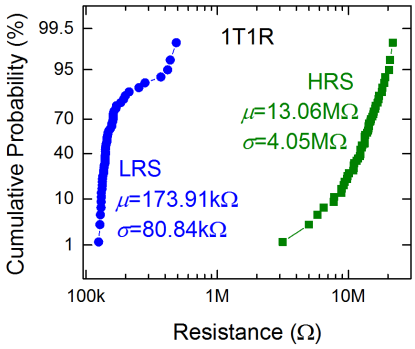

Fig. 12. Distribution of HRS and LRS resistances during 1T1R operation for the pulse measurements shown in Fig. 11.

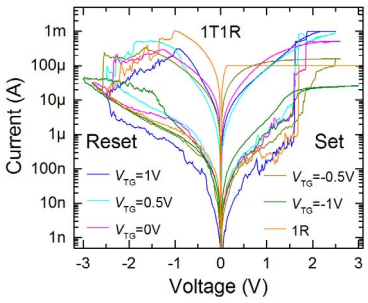

Fig. 13. 1T1R measurements using another top-gated MoS_2 FET also with W=50 μm, L=1 μm, and 5 nm HfO_2 as TG dielectric, showing set and reset at different V_{TG}, with V_{BG}=0 V, and with comparison with 1R.

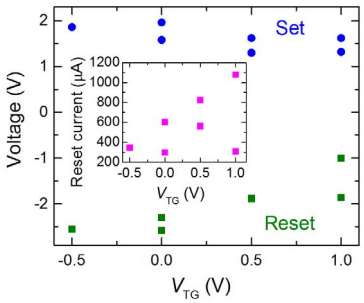

Fig. 14. Summary of set and reset voltages with different V_{TG} for measurements in Fig. 13, showing decrease in absolute value of reset voltages with V_{TG}. *Inset*: reset current that increases with higher V_{TG}.

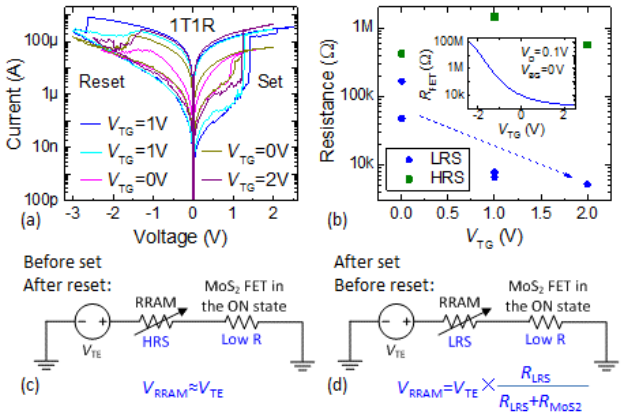

Fig. 15. 1T1R measurement, showing the effect of different V_{TG} on LRS and HRS resistances. (a) and (b): Top-gated MoS_2 FET with W=50 μm, L=1 μm, and with 15 nm HfO_2 as top gate dielectric, showing (a) set and reset at different V_{TG}, and (b) extracted LRS and HRS resistances at different V_{TG}, showing decreasing LRS resistance with increasing V_{TG}. The reset current at V_{TG}=0 V is only ~50 μA. *Inset* in (b): MoS_2 FET resistance at various V_{TG}. (c) and (d): Illustration of the resistances of the RRAM and MoS_2 FET, and the voltage on the RRAM during set and reset operations. The MoS_2 FET is turned on with low resistance.

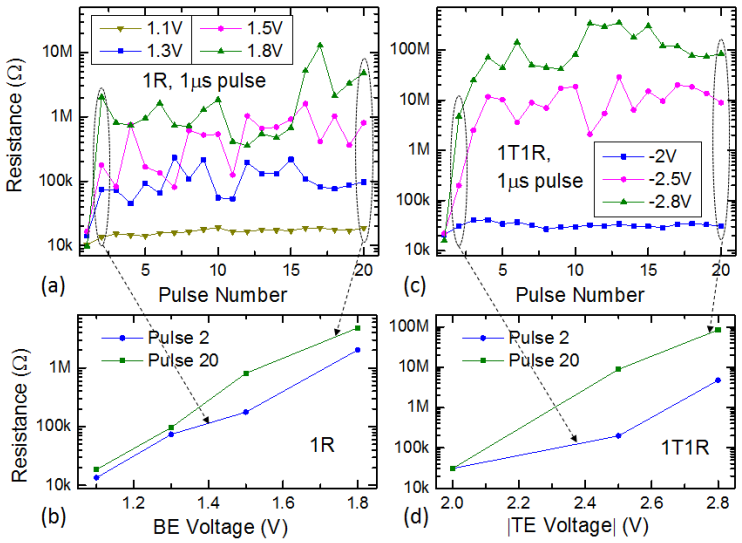

Fig. 16. Pulse reset measurements at various pulse voltages, showing multi-level reset resistances. (a) and (b): 1R measurement, showing (a) resistances with increasing pulse numbers. Resistance values before each pulse is applied is shown, and resistance at pulse 1 corresponds to the LRS value. (b) Summary of reset resistance with pulse voltage for 1R measurement in (a). (c) and (d): Corresponding plots as in (a) and (b) for 1T1R pulse measurements, showing large range and multiple levels of resistance values. The MoS_2 FET here has W=50 μm, L=2 μm, and top gate dielectric of 25 nm HfO_2. The FET is turned on at V_{TG}=5 V, and V_{BG}=20 V, with resistance of ~11.3 kΩ.

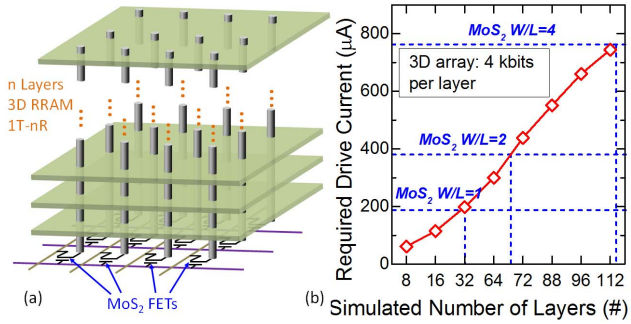

Fig. 17. SPICE-simulated drive current requirement for large-scale 1T-nR arrays formed by MoS_2 FET and 3D RRAM with increasing number of RRAM layers. (a) Schematic of the structure. (b) Driving capabilities of the fabricated MoS_2 FETs can drive high-density 3D RRAM arrays with large number of layers. The horizontal dashed blue lines show the current values obtained from our measurement data of MoS_2 FETs in Fig. 7.