3-D Resistive Memory Arrays: From Intrinsic Switching Behaviors to Optimization Guidelines

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***Abstract*— 3-D resistive switching random access memory (RRAM) is a promising candidate for high-density nonvolatile memory applications, as well as for monolithic 3-D integration interleaved with logic layers. In this paper, we develop a methodology for assessing and optimizing large-scale 3-D RRAM arrays. A systematic study on the intrinsic switching behaviors and optimization of 3-D RRAM arrays is performed, combining device measurements and 3-D array simulations. The dependence of programming voltage on array size, cell location and pulse parameters, statistical properties of operating 3-D RRAM arrays, and subthreshold disturbance on RRAM cells is experimentally investigated. Optimization guidelines for the performance and reliability of 3-D RRAM arrays from device level to architecture level are presented: 1) an optimized 1/*n* architecture for 100-kb 3-D RRAM arrays can improve write margin by 69.6% and reduce energy consumption by 75.6% compared with a conventional full-size array design; 2) a strategy of prioritizing storage location for reliable operation is presented; and 3) an optimal hopping barrier of oxygen ions is found to improve array immunity to disturbance.**

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***Index Terms*— 3-D array, optimization, reliability, resistive random access memory (RRAM), variability.**

I. Introduction

DATA-CENTRIC computing will benefit from a reoptimized memory hierarchy enabled by emerging nonvolatile memories, such as phase-change memory, spin-transfer-torque magnetic random access memory, and resistive switching random access memory (RRAM) [1]–[8]. Among these, RRAM stands out due to its excellent scalability, compatibility with CMOS process, high write/read speed together with a bit-alterable random access, and simple architectures for 3-D integration in a bit-cost scalable manner [9]–[13]. 3-D RRAM devices with a variety of materials and structures have been experimentally demonstrated [13]–[18]. Furthermore, monolithic 3-D integration of RRAM and FETs interleaved in vertical layers has been implemented as 3-D ICs [19]. Compared with 2-D memory arrays, 3-D RRAM arrays introduce complex issues regarding device behaviors, variability, and reliability [20], [21]. To assess the benefits of 3-D RRAM arrays, it is necessary to quantify the relationship between intrinsic cell characteristics and RRAM cell operation in the context of a 3-D array circuit [15]. In this paper, we present an assessment methodology for 3-D RRAM arrays that uses the electrical measurements coupled with 3-D array simulations. This methodology enables us to project the performance of various full-size 3-D RRAM arrays based on experimentally measured cell behaviors, as well as to provide guidelines toward optimizing overall performance and reliability for 3-D RRAM arrays.

II. Assessment Methodology for 3-D RRAM

The most previous studies on 3-D RRAM perform either electrical measurements on individual memory devices or resistor–capacitor (RC) network simulations using SPICE simulators [13]–[16], [21]. Circuit simulations of RC network can consider architecture effects, such as interconnect routing and parasitic components, but may lose essential information directly related to resistive memory cells. In contrast, device-level experiments can reflect the performance of devices with

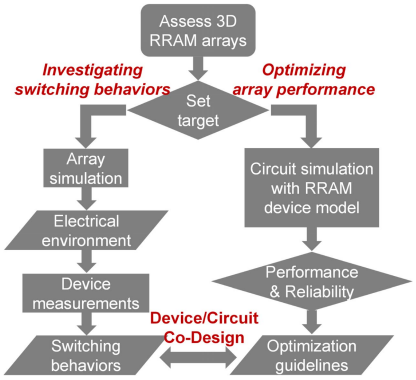

Fig. 1. Methodology and procedure for assessing 3-D RRAM arrays.

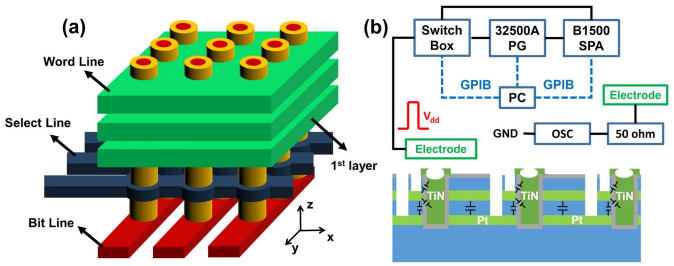

Fig. 2. (a) Schematic of the 3-D vertical RRAM array assessed in this paper. (b) Schematic of the electrical measurement setup [2 (WL) × 2 (BL) × 2 (SL) 3-D RRAM arrays were measured].

a 3-D geometry, but may lack insights into how memory cells will behave under a 3-D array operation. Here, we integrate both device measurements and large-scale array simulations to assess 3-D RRAM arrays, as shown in Fig. 1. Array simulations generate the electrical environment for the targeted memory cells within the array, where the electrical environment depends on the location of the memory cell within the 3-D array. These bias conditions are used to perform electrical measurements on individual 3-D RRAM devices or small-size arrays to study their intrinsic switching behaviors. Finally, through circuit simulations with the experimentally validated RRAM SPICE model, the 3-D RRAM design space can be optimized to meet performance and reliability targets.

III. Intrinsic Switching Behaviors

The 3-D vertical RRAM arrays assessed in this paper consist of Pt/HfO_x/TiN memory cells, vertical select transistors, wordlines (WLs), bitlines (BLs), and select lines (SLs) [20], as shown in Fig. 2(a). The array half-pitch (F) is 30 nm. Array simulations are based on a SPICE framework for 3-D RRAM arrays that accounts for the impact of interconnect routing and parasitic components, such as metal plane resistance, wire resistance along pillar electrodes and signal lines, and parasitic capacitance [20]. An experimentally verified RRAM SPICE model is employed in the simulations [22], [23]. The electrical measurement setup is given in Fig. 2(b). Here, external current compliance is applied to emulate the function of select transistors. The following assessment combines array simulations and electrical measurements to provide insights into the inherent characteristics of 3-D RRAM arrays.

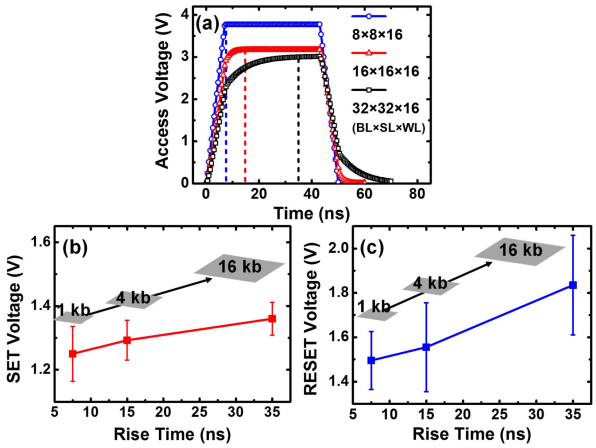

Fig. 3. (a) Simulated access pulses on the farthest selected cell located at the top layer of arrays of different sizes. (b) Measured relationship between SET voltage and pulse rise time for various array sizes. Selected cells in larger arrays face longer rise times in the access pulses, which leads to an increase in SET voltage for the selected cells. (c) Measured relationship between RESET voltage and pulse rise time for various array sizes. Higher voltage is required for RESET programming for larger array sizes.

A. Programming Voltage Dependency

The functionality of 3-D RRAM arrays is not merely determined by the individual memory cells, but is also strongly related to the array architecture and interconnect components due to the voltage drop along the interconnect. Therefore, the programming voltage for the selected cells in 3-D RRAM arrays may reflect the joint impact of array architecture, operation conditions, and device properties. The programming of arrays of different sizes is assessed in Fig. 3. To determine the influence of the RC network, array simulations were carried out using pulses with 4.2 V amplitude, 5-ns rising edge, and 50-ns width. Access pulses were then monitored on the selected cell located on the top layer at the corner farthest from V_{dd}. Fig. 3(a) shows that the shape of the access pulses becomes distorted in larger arrays, which can be attributed to the increasing impact of interconnect RC delay for larger arrays. Parameters of the pulse rising edge were extracted from the simulations and were set up for electrical measurements on 3-D RRAM devices. In this way, the devices that are measured using the electrical environment from the 3-D RRAM arrays can represent the selected cells during the array-level operation. Fig. 3(b) and (c) shows that for larger arrays, the increase in the pulse rise time leads to a measured increase in SET and RESET programming voltage. For oxide-based RRAM, the formation and recombination of oxygen vacancies (V_O) in the switching layer lead to the conductive filament (CF) evolution during SET and RESET [24]–[28]. During transient evolution of CF, SET and RESET processes are triggered by the cumulative effect of voltage and biasing time, which can be reflected by the voltage–time (V–t) dilemma of RRAM pulse operation [5], [10], [23]. With shorter pulse rise time for the same pulsewidth, the integral area under the V–t curve becomes larger. The V–t cumulative effect is thus stronger in configuring conductive paths within the RRAM, resulting in a lower SET/RESET voltage. This implies that for programming large-scale 3-D RRAM arrays,

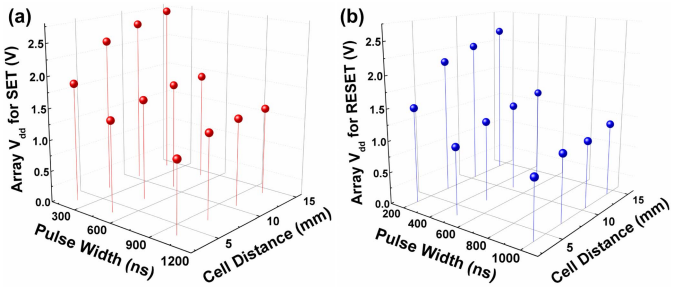

Fig. 4. Measured required V_{dd} supply for (a) SET and (b) RESET programming as a function of the pulsewidth and the cell distance to the voltage source.

the optimization of interconnects may lead not only to a higher speed, but also to a lower requirement for the triggering voltage and ultimately reduced energy consumption.

The V_{dd} requirement for 3-D RRAM arrays is assessed experimentally. Fig. 4 shows the dependence of SET and RESET operation on pulsewidth and the distance of the selected cell from the voltage source. At the largest distance, 60 b-cells were involved in the measurements. Here, it is shown that a higher V_{dd} is required to program a cell farther from the voltage source during SET and RESET operations, as the different distances that pulses travel cause different access pulse rise times. Furthermore, the voltage supply requirement is also dependent on the choice of pulsewidth. Longer pulses lower the minimum V_{dd} for SET and RESET operations. With a fixed pulse amplitude, shorter pulses may not successfully trigger a switching process. In this case, the pulse amplitude has to be increased to program the cell. The key message is that suitable programming pulses for a 3-D RRAM array must be determined from both array size and cell location.

B. Statistical Behaviors of 3-D RRAM Arrays

Variability is an inherent feature of many resistive switching memories, regardless of the specific materials, structures or fabrication processes [30]–[33]. Here, we assess the statistical properties of 3-D RRAM arrays. First, 3-D array simulations are performed to generate a specific electrical environment for the selected cell in 3-D RRAM arrays of various sizes. The RESET operation for 8-layer 3-D RRAM arrays is simulated with planes ranging from 64 (BL) × 64 (SL) to 256 (BL) × 256 (SL), totaling 32–512 kb. Fig. 5(a) shows the relationship between the access voltage (defined as the voltage across the selected cell) and the plane size. As in 2-D RRAM arrays, sneak leakage paths also cause access voltage degradation in 3-D RRAM arrays [31]. The sneak current in 3-D RRAM arrays and interconnect wire resistance jointly contribute to the undesired voltage drop along the path to the selected cell. Therefore, larger arrays exhibit lower access voltages. SET operation is also simulated with array size ranging from 32 (BL) × 32 (SL) × 8 (layer) to 32 (BL) × 32 (SL) × 24 (layer), totaling 8–24 kb. As shown in Fig. 5(b), additional layers cause a lowered ON-current from the bottom transistor for the selected cell. This stems from the increase in interconnect resistance along the selected vertical pillar and, thus, the decrease in the drain–source voltage across the transistor. Array simulations for the SET and RESET operations are used to set up the electrical measurement of the individual RRAM to emulate the effect of a 3-D array. Fig. 5(c) shows the measured statistical distributions of programmed cell resistances after the SET or RESET operations for various array configurations. After the RESET operation, the selected cell is programmed to high-resistance state (HRS). For larger BL × SL plane size, the access voltage for the RESET operation decreases due to IR drop, resulting in a weaker reset of the cell and thus lower HRS resistance values. After the SET operation, the selected cell is programmed to low-resistance state (LRS). With more 3-D layers, the spread of LRS moves toward higher resistance level resulting from the decrease in the ON-current. The statistical data were then analyzed to obtain the coefficient of resistance variation, as shown in Fig. 5(d). 3-D RRAM arrays with more vertical layers or smaller plane sizes have more variations, because for either cases, the spread of programmed resistance becomes wider with higher deviation (σ) from the mean value (μ). In addition, the interaction between SET and RESET operation was also measured. Fig. 5(e) shows that with smaller array sizes, the SET voltages shift upward. This results from the statistical behaviors of HRS resistances after programming. Deeper RESET states from higher access voltages will induce wider gaps in the RRAM for the following SET operations [27]. Thus, a higher voltage is required to generate sufficient V_O for a successful SET process. The statistical properties of HRS and LRS originate from the variability of CFs [30]. For the memory cells in 3-D RRAM arrays, the factors causing the stochastic behaviors include the variations in the geometry and location of the filaments formed around pillar electrodes of 3-D RRAM, and in the gap distance during cycle-to-cycle programming. Variability of energy barriers related to the generation and recombination of V_O may account for the stochastic behaviors of SET and RESET voltage variations [31]. The measured correlation between SET and RESET operations from cycle to cycle [Fig. 5(e)] indicates that the behaviors of RRAM are strongly dependent on the switching history.

C. Subthreshold Disturbance

Reliability is a major concern for RRAM arrays [5]. Typically, selected cells receive more focus. However, the reliability of unselected cells throughout an array should also be considered for reliable design, as the state of any memory cell, whether selected or unselected, will impact the overall reliability of the memory array. Fig. 6(a) shows the simulated distribution of the voltage drop on the 1-kb unselected cells at the top layer of a 32 (BL) × 32 (SL) × 16 (layer) 16-kb array. Under the $V/2$ bias scheme for 3-D RRAM arrays [34], memory cells that are closer to the V_{dd} source in the selected layer face higher voltage, slightly less than half of V_{dd} due to voltage drop on the interconnect. For the long-term write operations when consecutive pulses are applied to RRAM arrays, the bias on the unselected cells may disturb their states [35]. A large number of consecutive pulses with amplitudes between 1.1 and 1.3 V were applied,

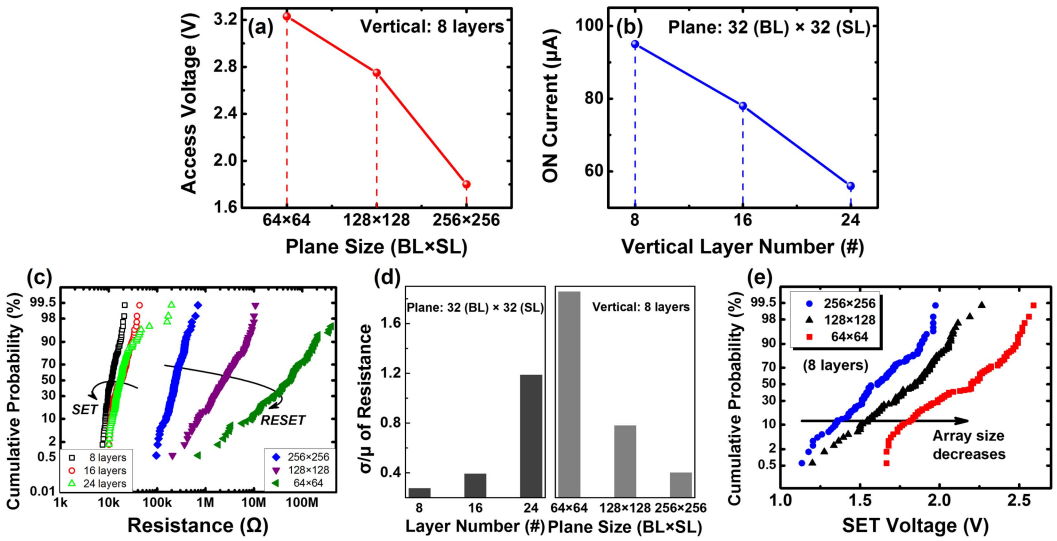

Fig. 5. (a) Simulated access voltage on the selected cell for different array 2-D plane sizes during RESET operations. (b) Simulated ON-current through the selected cell in LRS as a function of layer number during SET operations. (c) Measured statistical distributions of programmed cell resistance after SET and RESET operations, for different array configurations. The electrical environment for programming RRAM cells is extracted from the array simulations to use in the measurement. Each spread of resistance is obtained from 100-cycle operations. (d) Variation coefficient of measured resistance distributions under various array configurations. (e) Measured statistical distributions of SET programming voltage for the selected cell with varying array size. Each spread of SET voltages is collected from 100-cycle operations.

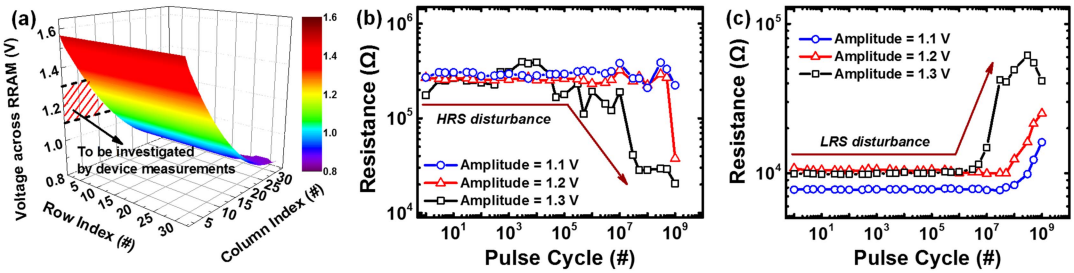

Fig. 6. (a) Distribution of the voltage across the 1-kb unselected cells located at the top layer in a 16-layer 3-D RRAM array. V_{dd} source is applied at Column #0 of the selected metal plane. The voltage distribution is obtained by the SPICE simulation, where the unselected cells that are closer to V_{dd} supply have higher voltage drop. The reliability of a group of cells under the bias ranging from 1.1 to 1.3 V is investigated by device measurements. (b) Measured subthreshold HRS disturbance on the unselected cells under various bias conditions. (c) Measured subthreshold LRS disturbance on the unselected cells under various bias conditions.

and device resistance was measured as a function of the number of pulses applied, as shown in Fig. 6(b) and (c). Within thousands of positive pulse cycles, the HRS resistance of the measured cell remains steady, since the pulse amplitude (1.1 to 1.3 V) is in the subthreshold region for SET operation. Following continuing pulse measurements, the HRS resistance dropped, thus disturbance on the cell state occurs. This resistance drop was found to occur earlier under higher pulse amplitudes. Similarly, subthreshold disturbance on the cells in LRS was measured, and a gradual increase in the cell resistance was observed after a number of pulses. These unselected cells tend to be disturbed earlier under higher pulse amplitudes as well. As shown in Fig. 6, programming the selected cell in a 3-D RRAM array leads to undesired disturbance on the unselected cells of the array. This deviation from the programmed HRS or LRS resistance results from the subthreshold CF evolution under consecutive pulses, and therefore, is a cumulative process relevant to the long-term reliability of 3-D RRAM arrays [36].

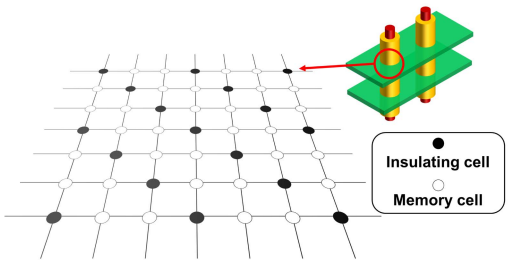

Fig. 7. Optimized array architecture for layers in 3-D RRAM arrays where insulating cells are uniformly distributed.

IV. Optimization Guidelines

A. Performance Optimization

Sneak leakage paths in 3-D RRAM arrays lead to the degradation of array performance, including write margin (defined as access voltage normalized by V_{dd}) and energy consumption. We design an improved array architecture for higher write margin and lower energy consumption by reducing sneak leakage paths, as shown in Fig. 7. For a certain layer in

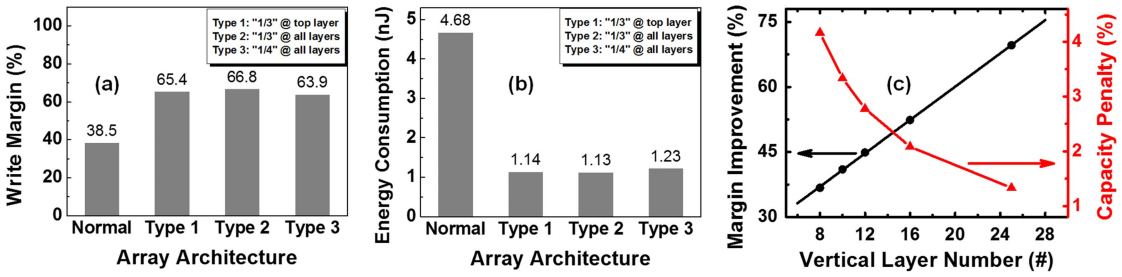

Fig. 8. (a) Write margin and (b) energy consumption of operating 25-layer 100-kb 3-D RRAM arrays constructed in different array architectures, with or without optimization. (c) Comparing the conventional full-size architecture and Type 1 architecture, the improvement of write margin can be even more effective with a larger number of vertical layers. The memory capacity penalty due to insulating nodes is also reduced with more vertical layers.

a 3-D RRAM array, insulating cells with much higher resistance are uniformly distributed in the layer. The fabricated devices that are left unformed with the as-fabricated high resistance can be regarded as the insulating cells. In a certain layer of this 1/*n* array configuration, there is one insulating cell among *n* devices, in both the row and the column directions. In this way, the topology of the high-resistance network is universally applicable to suppressing randomly distributed sneak current. Array performance, including write margin and energy consumption for the 1/*n* configuration, is quantitatively studied via simulating the operation of a 64 (BL) × 64 (SL) × 25 (layer) 100-kb 3-D RRAM array. There are three optimized configurations here: 1) Type 1 is 1/3 configuration only for the top-layer 2-D array of a 3-D RRAM array; 2) Type 2 is 1/3 configuration for a 3-D array; and 3) Type 3 is 1/4 configuration for a 3-D array. Fig. 8(a) shows that the optimized architecture improves the write margin significantly. Comparing Type 2 and Type 3 architecture, a higher proportion of insulating nodes raises the write margin due to the reduced sneak current, but also sacrifices more memory capacity. Comparing Type 1 and Type 2 architecture, the array with 1/3 configuration only for the selected top layer has a similar write margin as the array with 1/3 configuration across all layers. This is because the dominant sneak leakage paths are located at the top layer. The energy consumption of operating 3-D RRAM arrays was also assessed, as constraining sneak leakage paths also allow for a low-energy operation. As shown in Fig. 8(b), Type 1 architecture can reduce the energy consumption by 75.6% with 1.3% capacity penalty (due to unusable cells that remain in the as-fabricated high resistance), as compared with the conventional full-size architecture. For Type 2 architecture, the energy consumption is close to that of Type 1 architecture, but the capacity penalty increases to 33.3%, since the insulating cells are distributed throughout all the layers in the 3-D array. The effectiveness of energy savings using Type 1 architecture also confirms that the top layer faces more severe sneak path issues under the worst case scenario. We next evaluate the impact of the vertical dimension of 3-D RRAM arrays on the effectiveness of the optimized array architecture. Type 1 configuration is evaluated as an example. Keeping the plane size unchanged and increasing the number of vertical layers, the write margin improvement over the conventional architecture increases. This may be attributed to the interaction between the sneak paths in different layers. For a larger number of vertical layers, the sneak current becomes more significant. Therefore, by constraining the dominant leakage paths at the top layer, the undesired interconnect voltage drop can be reduced, and the write margin is improved. In addition, Fig. 8(c) shows that the memory capacity penalty diminishes with additional vertical layers, since only the top layer employs Type 1 architecture. Using Type 1 architecture for a 25-layer 100-kb 3-D RRAM array, the write margin is improved by 69.6%, and the energy consumption is reduced by 75.6%, with only a capacity penalty of 1.3% as compared with the conventional design of a full-size 3-D RRAM array, where all the RRAM cells are used for data storage [15]. Hence, building taller vertical RRAM arrays using the optimized architecture will improve the overall performance.

B. Reliability Optimization

A disturbance on the unselected cells in 3-D RRAM arrays is a function of the array architecture, since the statistical spread of cell resistance states in a 3-D array will lead to the changing of data pattern, which alters the following array operation. Disturbance-in-array behaviors are simulated in a 32 (BL) × 32 (SL) × 16 (layer) array. Looking into the resistance of the unselected cells located along the selected pillar across multiple layers, both the HRS disturbance [Fig. 9(a)] and the LRS disturbance [Fig. 9(b)] show the layer-dependent behaviors. Cells in the bottom layers are easier to disturb, and the layers closer to the selected top layer are more robust against consecutive pulses. The behaviors of the unselected cells located in the selected vertical layer are shown to be location dependent, as shown in Fig. 9(c) and (d). RRAM devices near the selected cell can tolerate more pulses, since the voltage across the unselected cells decreases from the voltage source to the selected node. The impact of memory cell location on the reliable operating cycles is quantified in Fig. 10(a). A location of unselected cells is normalized to its position relative to the selected cell. The location-dependent behaviors shown in Fig. 10(a) provide opportunities for prioritizing storage location for critical data requiring more robust memory bits. Cells far away from the selected node along the pillar and cells close to the selected node along the metal plane are more tolerant to disturbance. Therefore, data mapping algorithms can be developed accordingly to store critical or frequently visited data in the robust location.

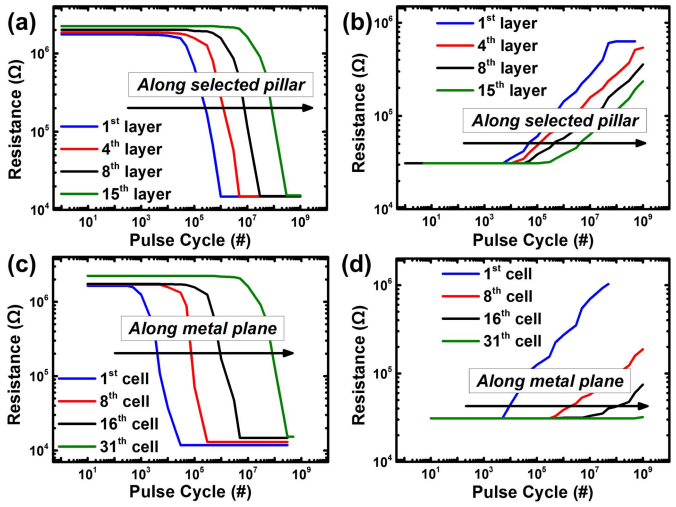

Fig. 9. Simulated layer-dependent (a) HRS disturbance and (b) LRS disturbance along the selected pillar, together with location-dependent (c) HRS disturbance and (d) LRS disturbance on the unselected cells in the selected metal plane.

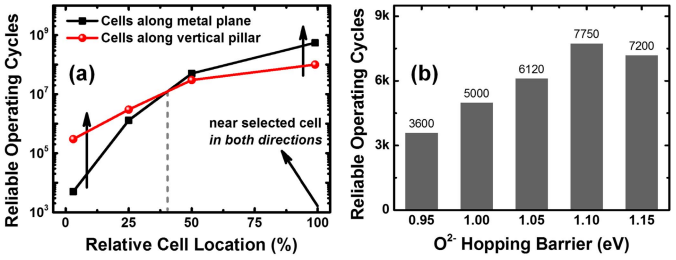

Fig. 10. (a) Impact of storage location in plane and vertical dimensions on the reliable operating cycles. A location of unselected cells in both dimensions is linearly normalized to the selected cell. Memory cells that are closer to the selected device in the metal plane (xy plane), or are located farther from the selected device along the vertical pillar (z-direction), are found to be more robust with higher tolerance to disturbance. (b) Impact of switching-related hopping barrier of devices on the reliable operating cycles. Tuning RRAM with an optimized switching layer may lead to improved tolerance to disturbance.

From a device perspective, a subthreshold disturbance is related to the cumulative CF evolution processes. The physics-based simulation reveals that tuning O^{2-} hopping barrier can lead to improved reliability in the array level, as shown in Fig. 10(b). However, for the O^{2-} hopping barrier energy that is larger than the optimal value, a higher voltage bias is required to program the selected cell, resulting in increasing voltage drop on the unselected cells in a 3-D array. These two competing factors suggest an optimal point found by the physics-based SPICE simulation. Therefore, appropriate tuning of device switching layer and interface is beneficial for the reliability of 3-D RRAM arrays.

V. Conclusion

We present an assessment methodology that combines the use of 3-D RRAM array simulations and electrical measurements. This methodology allows us to investigate the programming voltage dependence, statistical behaviors of memory cells, and subthreshold disturbance in 3-D RRAM arrays. Array dimensions and cell location are revealed as the important factors for the programming functionality and array reliability. Inserting high-resistance cells every n cells in a 3-D array (the $1/n$ array architecture) can suppress the dominant sneak leakage paths in the selected layer, achieving low-energy consumption and high write margin. Optimizing for robustness against disturbance requires a deep understanding of the strong interaction between device and circuit. Featuring device-architecture codesign and optimization, this paper may pave the way toward better understanding of design challenges and opportunities for 3-D RRAM-based systems.

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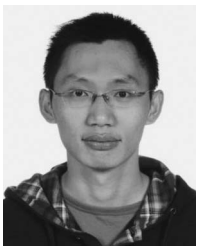

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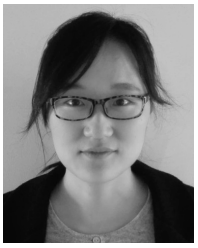

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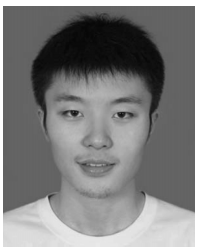

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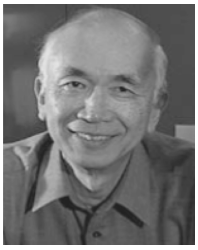

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