Nonvolatile Logic and *In Situ* Data Transfer Demonstrated in Crossbar Resistive RAM Array

Haitong Li, Zhe Chen, Wenjia Ma, Bin Gao, Peng Huang, Lifeng Liu, Xiaoyan Liu, and Jinfeng Kang

***Abstract*— For the first time, nonvolatile logic, memory, and communication are experimentally demonstrated all within a crossbar resistive random access memory (RRAM) array through the state interaction among RRAM cells. With all the array cells initialized to high resistance states, OR and NOT logic are measured as a proof of functional completeness for computation, with input and output data directly stored in the array. Following the same computation paradigm, *in situ* data transfer within the crossbar RRAM array is realized. The cell-to-cell communication is proved efficient by the measured resistance evolution of a row of RRAM cells during consecutive data transfer. Reliability characteristics, including endurance, retention, and disturbance are scrutinized for the robust computing systems.**

***Index Terms*— Resistive random access memory (RRAM), nonvolatile logic, communication, crossbar array.**

I. Introduction

RADICAL modifications to the current transistor-based computing architecture are required to meet the increasing need of low-power and high-density data-centric information processing [1], [2]. To solve the scaling and leakage issues faced by the complementary metal-oxide semiconductor (CMOS) logic, nonvolatile memory devices are leading the way towards more efficient computing by functioning as logic devices in a nonvolatile manner [3], [4]. Following this technology path, several exciting explorations have been reported with diverse emerging memories, such as spin-based magnetic random access memory (MRAM) [5], [6], phase change memory (PCM) [7], and resistive random access memory (RRAM) [8]–[10]. Among these novel logic solutions, RRAM-based computing attracts much attention due to its high switching speed, low operation power, and compatibility to CMOS fabrication process [11]–[14]. More importantly, the simple structure of RRAM enables the realization of highly compact crossbar RRAM arrays with 4 F^2 cell area (F is the minimum feature size) [15]–[17], which is critical for the goal of localized massive data processing [1]. In addition, the direct communication in memory, which has been reported in MRAM [18], is also required to fully develop the potential of RRAM-based computing and thereby boost memory-centric information processing. However, the feasibility demonstration of nonvolatile logic and communication in crossbar RRAM arrays is still lacking. In this letter, we experimentally demonstrate nonvolatile logic, memory, and direct communication along a row of RRAM cells within a 4 F^2 crossbar array. From an architecture perspective, the 'integration' of memory, logic and communication in a nonvolatile system provides boundless possibilities for non-von Neumann computing architecture, in contrast to the previous works where the logic aspect was mainly addressed [5]–[10], [19], [20]; from an implementation perspective, the operations are demonstrated based on 4 F^2 crossbar RRAM arrays of the highest possible density, without series resistors or transistors involved [8], [10], [19], and the mismatch between volatile input and nonvolatile output mentioned in [9] is intrinsically eliminated for the cascadable computation.

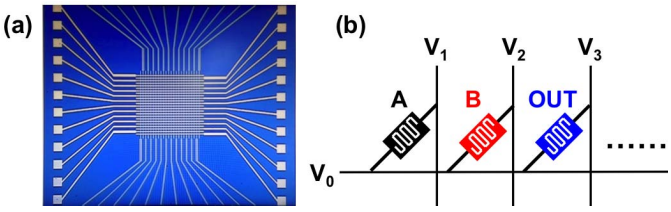

Fig. 1. (a) Photo image of the 24 × 24 crossbar RRAM array used for the demonstration in this work. (b) Computation paradigm based on crossbar RRAM arrays. Resistance of RRAM cells (R_{LRS} & R_{HRS}) serves as the state variable ('1' & '0') for both input and output of logic operations, which enables logic cascading. Computation is performed under pulse operations.

II. Nonvolatile Logic

A 24 × 24 Pt (100 nm)/HfO_x (3nm)/TiN (40 nm) crossbar RRAM array was fabricated for the demonstration in this work. The cell size is 2×2 μm^2. The photo image of a crossbar array is shown in Fig. 1(a), where the up/down pads for vertical lines are of the same structure and area with left/right pads, but are not captured in the image due to facility limit. More details about fabrication process and array functionality can be found in [21]. Electrical measurements were carried out using Agilent B1500A semiconductor parameter analyzer and Agilent B1530A waveform generator/fast measurement unit. A step-by-step forming procedure (with over 90% success rate) was employed to minimize the sneak leakage current, and the already formed devices were switched from low resistance (R_{LRS}) to high resistance (R_{HRS}) [22]. Computation paradigm based on the crossbar RRAM array is shown in Fig. 1(b), which will be used to illustrate the following

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TABLE I
OR LOGIC: EXPERIMENTAL OPERATION PROCEDURE
(PULSE WIDTH = 500 ns & RISE TIME = 50 ns)

	V0	V1	V2	V3
#1		0 V		3 V
#2			0 V	3 V
Read	0 V			0.1 V

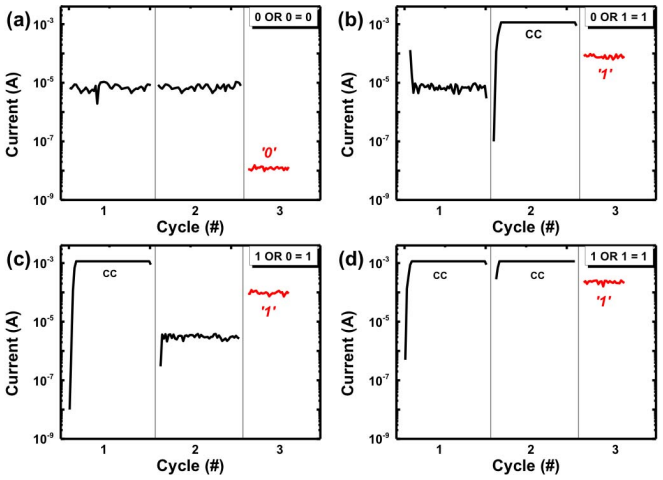

Fig. 2. Measured current through the OUT cell during *OR* logic operation under all input combinations: (a) A = B = 0, (b) A = 0 & B = 1, (c) A = 1 & B = 0, and (d) A = B = 1. Compliance current (CC) is 1 mA. Cycle #1 and #2 are computing cycles, after which *OR* logic is completed with results stored *in situ*. Data in OUT cell are then read out during cycle #3.

logic operations. The state variable for logic operations is cell resistance, where R_{LRS} is assigned to '1' and R_{HRS} is assigned to '0'. Along the crossbar array, logic operations are performed via 'state interaction' between input and output RRAM cells, before which the operating cells are initialized to '0' by RESET operations. Such 'state interaction' is triggered by the pulses applied at vertical bit lines (BLs) and horizontal word lines (WLs). Since inherently both input and output of logic operations are cell resistance, therefore logic cascading is enabled in a nonvolatile manner. Here we show the experimental results of *OR* and *NOT* logic operations. {*OR*, *NOT*} is a functionally complete set which supports arbitrary Boolean expressions [23]. 500-ns pulse width and 50-ns rise time are setup for pulse operations, and read pulses are 250-ns wide. Table I shows the experimental operation procedure for *OR* logic. Cycle #1 and #2 aim to trigger the 'state interaction' between input (A & B) and output (OUT) cells under pulse operations. Initially, OUT cell is in R_{HRS}, and later the result *in situ* stored in OUT cell depends on the input states of A and B. The current through the OUT cell during the whole procedure is measured, as shown in Fig. 2 with all input combinations considered. The compliance current (CC) is 1 mA. The developed computation paradigm creates interaction path for input and output RRAM cells during each cycle, which leads to the difference in the observed current through the OUT cell. In Fig. 2(a) where the

TABLE II
NOT LOGIC: EXPERIMENTAL OPERATION PROCEDURE
(PULSE WIDTH = 500 ns & RISE TIME = 50 ns)

	V0	V1	V2	V3
SET	0 V	3 V		
#1		0 V	1.5 V	3 V
Read	0 V			0.1 V

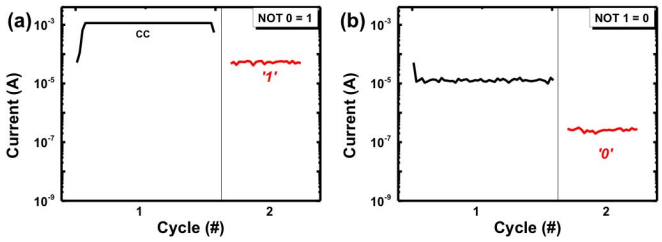

Fig. 3. Measured current through the OUT cell during *NOT* logic operation under all input combinations: (a) B = 0 and (b) B = 1. Cell A is preliminarily configured to R_{LRS} by SET operation. Compliance current (CC) is 1 mA. *NOT* logic is completed after cycle #1 and results are read out during cycle #2.

input A = B = 0, the current through OUT cell is relatively low for both cycle #1 and #2, since the high-resistance A or B is in series with OUT cell and thereby OUT remains '0'. For the cases where A or B is '1', one SET process will be triggered during pulse operations, as shown in Fig. 2(b) and Fig. 2(c). When in series with an input cell in LRS, SET operation is performed on the OUT cell, which results in the abrupt current jump limited by CC (no noise is shown after reaching CC level due to measurement setup). For A = B = 1, SET operation is also triggered during cycle #1, and the current through OUT in R_{LRS} is limited by CC during cycle #2. Read cycles in these cases verify the computation results. As shown in Fig. 2(b)-(d), '1' is stored in OUT cell after 'state interaction'. *NOT* logic is also measured. Table II shows the experimental operation procedure for *NOT* logic. As an assisting cell, cell A is preliminarily configured to R_{LRS} a by SET cycle. Then, V_{dd} and half V_{dd} pulses are applied on corresponding BLs to perform the 'state interaction' between B and OUT. Fig. 3 shows the measured transient current through the OUT cell during *NOT* and read operations. Due to voltage dividing between input B and assisting cell A, the electrical potential on the WL will vary with the state of B. For the case where B = 0, the electrical potential on the WL is relatively low, resulting sufficient voltage across OUT cell to trigger SET operation, as shown in Fig. 3(a). For the case where B = 1, the conductive path from B to A leads to an increase in the electrical potential on the WL. Hence, OUT remains '0', as shown in Fig. 3(b).

III. *In Situ* DATA TRANSFER

Alongside nonvolatile logic and memory functions, direct in-memory communication is also demonstrated following the same computation paradigm. Fig. 4 illustrates how *in situ* data transfer occurs between two RRAM cells in a crossbar array.

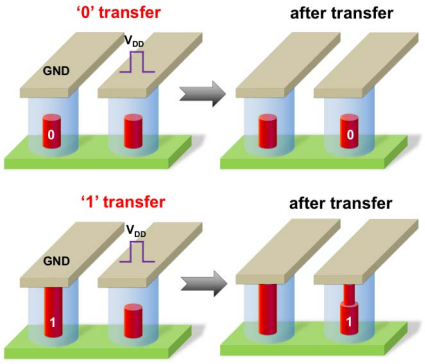

Fig. 4. Schematic of *in situ* data transfer between two RRAM cells under pulse operation. The efficient one-step cell-to-cell communication does not require extra readout and write-back processes.

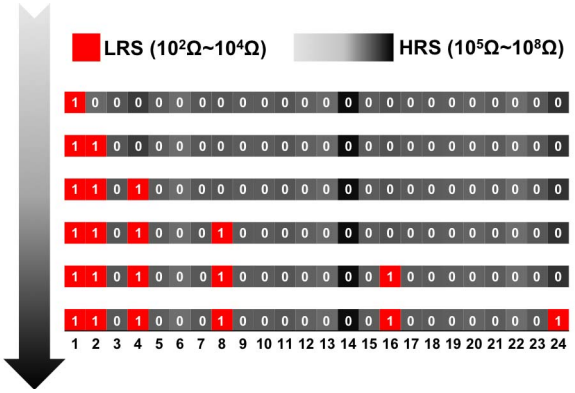

Fig. 5. Measured resistance evolution of all the 24 cells in a certain row during consecutive data transfer. Initially, the #1 cell stores '1' and the rest of the cells store '0'. Through pulse-train operations, the data in #1 is transferred *in situ* to #2, #4, #8, #16, and #24.

Operating cells are initialized to '0', which is consistent with the configuration of logic mode. V_{dd} pulse is used to 'select' the transmission target, and the BL of the data source cell is grounded during the operation. '1' transfer is a result of SET operation while '0' transfer is not. The data transfer process is efficient involving only one step in memory. Following this principle, *in situ* data transfer is demonstrated in the crossbar RRAM array. Fig. 5 shows measured resistance evolution of all the 24 cells in a certain array row during consecutive data transfer. Source data is '1' stored in cell #1. Under pulse-train operations, the data is transferred from #1 to #2, #4, #8, #16, and #24 successively, without extra buffer and transmission circuits involved. During each transfer, the data is written into the target cell and stored in a nonvolatile form, and can be read out or re-written via normal memory operations. The one-step data transfer from #1 to #24 along the array row indicates that direct in-memory communication in crossbar RRAM arrays is feasible.

IV. Reliability

For the implementation of large-scale robust computing systems based on RRAM, reliability metrics should be examined and discussed. The endurance of the OUT RRAM cell is given in Fig. 6(a), where there is no significant degradation

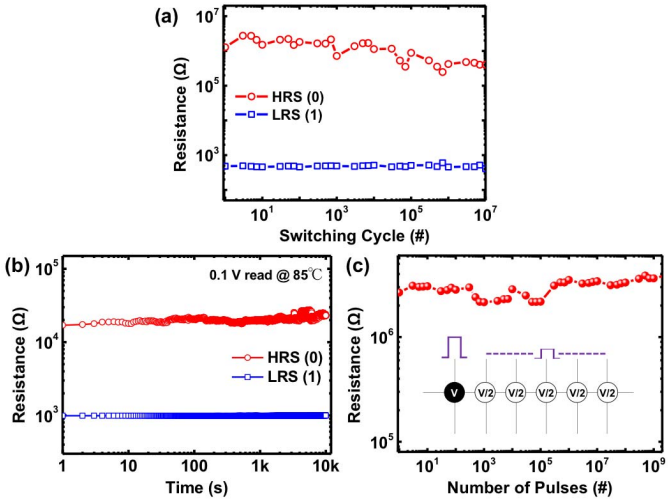

Fig. 6. (a) Measured endurance characteristics of the OUT RRAM cell with no significant degradation after 10^7 cycles. (b) Measured retention characteristics for both LRS and HRS up to 10^4 seconds at the temperature of 85 °C. (c) Measured disturbance immunity of an unselected cell under $V_{dd}/2$ bias as a general case. The inset shows a simplified diagram of bias conditions.

after 10^7 cycles. Material selection and structure optimization can further lead to endurance improvement [12], [24], [25]. For the traditional von Neumann architecture where data movement is intensive [2], the logic and cache modules may undergo a considerable amount of operations. However, thanks to the nonvolatile nature, the computation paradigm here inherently eliminates the excessive switching of RRAM by storing and reusing the logic operations for the repeated tasks. Thereby, the requirement of device endurance can be greatly relieved. Fig. 6(b) shows the retention behaviors for LRS and HRS. Good retention characteristics are beneficial for the robust nonvolatile operations, where read operation is dominant. In this proof-of-concept work, the relatively small array size and HRS configuration of un-addressed rows jointly help to minimize the risks of disturbance and sneak leakage issues during computing mode [22]. However, for large-scale array implementation, protection voltage (V_{PRO}) applied at unselected BLs is required [26], [27], which can be described as [26]:

$$V_{PRO} = \frac{1}{1+2\alpha}\left(V_{half} + \alpha V_{dd}\right) \quad (1)$$

where α is R_{HRS}/R_{LRS} ratio, and V_{half} is the voltage applied at the half-selected BL. To simplify peripheral circuitry, V/2 bias scheme used for write operation may also serve as the protection [28]. Fig. 6(c) shows the disturbance immunity of unselected cells to over 10^9 $V_{dd}/2$ pulses. Last, although the balanced array data pattern formed by Boolean '0's & '1's helps to avoid severe sneak paths due to HRS network [29], [30], selectors with asymmetric behaviors and updated bias schemes may be required to suppress sneak leakage current for large-scale system demonstration.

V. Conclusion

Functionally complete nonvolatile logic and *in situ* data transfer are experimentally demonstrated in a crossbar

RRAM array. As a promising architecture for RRAM circuits, crossbar arrays are proved feasible to implement computation in memory with the data density higher than other array topologies. Efficient *in situ* data transfer provides more flexibility for the cascadable logic operations, and is able to boost memory-centric data processing. As the first demonstration of the 'integration' of logic, memory, and direct communication within a nonvolatile system, this work helps pave the way towards highly efficient, high-density and ultra-low-power RRAM-based information processing systems.

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