# Mechanism of vertical Ge nanowire nucleation on Si (111) during subeutectic annealing and growth

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(Received 11 April 2011; accepted 19 August 2011)

The direct integration of Ge nanowires with silicon is of interest in multiple applications. In this work, we describe the growth of high-quality, vertically oriented Ge nanowires on Si (111) substrates utilizing a completely sub-Au–Si-eutectic annealing and growth procedure. With all other conditions remaining identical, annealing below the Au–Si eutectic results in successful heteroepitaxial nucleation and growth of Ge nanowires on Si substrate while annealing above the Au–Si eutectic leads to randomly oriented growth. A model is presented to elucidate the effect of the annealing temperature, in which we hypothesized that sub-Au–Si-eutectic annealing leads to the formation of a single and well-oriented interface, essential to template heteroepitaxial nucleation. These results are critically dependent on substrate preparation and lead to the creation of integrated nanowire systems with a low thermal budget process.

## I. INTRODUCTION

Semiconductor nanowires have attracted substantial interest in recent years due to their wide range of potential applications, including nanoelectronics, thermoelectrics, solar energy conversion, and biosensing.[1–5] Germanium nanowires are of particular interest for their high intrinsic hole and electron mobilities when compared to silicon,[6,7] relatively low-growth temperature (below 400 °C), and compatibility with current silicon VLSI technology.

The widely accepted growth mechanism for the creation of Ge nanowires is the vapor–liquid–solid (VLS) mechanism. During VLS nanowire growth, a vapor phase precursor for Ge—such as $GeH_4$ or $Ge_2H_6$—decomposes catalytically at the surface of a metal nanoparticle (most often one with which it forms a binary eutectic) and then dissolves into the metal nanoparticle to form a molten alloy. The continuous supply of Ge from the vapor phase results in supersaturation of Ge within the liquid alloy nanoparticle, and leads first to nucleation and then axial growth of the nanowire. Proper epitaxial growth requires that the initial nucleation event occurs via the formation of an epitaxial interface with the substrate, which provides the template by which the nanowire selects its growth direction.

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DOI: 10.1557/jmr.2011.313

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Conceptually, the formation of liquid alloy droplets requires that the growth process be carried out at temperatures above the binary eutectic melting point, 361 °C in the case of Au–Ge studied here. Recently, several studies have shined the light in the mechanism of VLS Ge nanowire growth below the Au–Ge eutectic point.[8–10] McIntyre et al. postulated that the liquid can be stabilized below the eutectic temperature by two phenomena: first the barrier associated with homogeneous nucleation of solid Au, and second the excess saturation of Ge required to drive the transfer of Ge atoms from the liquid droplet to the growing solid nanowire.[9] Growth via the VLS mode below the eutectic temperature was confirmed via direct observations in the work of Kodambaka et al.[8] These observations are important because the ability to grow uniform epitaxial Ge nanowires at low-growth temperatures is of strong interest, enabling a decrease in the overall thermal budget during semiconductor device processing.

Heteroepitaxial integration of Ge nanowires on Si substrates is of particular interest as this offers a direct, bottom-up assembly approach with control of orientations and compatibility with current silicon-based industrial manufacturing processes. A two-step strategy is commonly utilized. Either a nucleation step with Ge precursor provided or an annealing step without the presence of Ge precursor is performed typically at a temperature different from the growth temperature before the growth step. To achieve reproducible epitaxial growth, numerous factors, such as substrate preparation, growth temperature, total pressure, partial pressure of the reactive gas, and metal catalyze size, need to be optimized.[11–16] For example, the underlying substrate orientation influences the crystallographic orientation of the epitaxially grown nanowires. Generally, the highest quality Ge nanowires are grown on (111) oriented substrates, with Au catalysts larger than 20 nm, and result in <111> oriented, single crystalline nanowires which grow vertically from the substrate. Moreover, growth quality can be affected by the annealing of the substrate prior to growth.[12,14] In prior work, high temperature annealing (above Au–Si eutectic point) of the substrate prior to the introduction of the gas precursor has been found to facilitate a high density of epitaxial Ge nanowires grown ranging between 320 and 380 °C. Kamins et al.[12] suggested that this annealing step removes any residual solvent and thereby improves the contact of the Au nanoparticles with the Si substrates, which probably enhances the ability of the nanowires to template epitaxially at the onset of nucleation.

In this work, we demonstrate the growth of dense, epitaxial Ge nanowires on a (111) silicon substrate using annealing and growth steps both carried out at as low as 280 °C. These results allow us to form high-quality Ge nanowires on silicon with a further low-thermal budget process, a substantial improvement towards incorporation into conventional VLSI processing.

## II. EXPERIMENTAL SECTION

Prior to growth, the substrate was etched with a buffered hydrofluoric acid solution to remove the surface oxide. A well-mixed solution containing 200μl of 40 nm gold colloidal nanoparticles and 2 ml of 10% $HF/H_2O$[15] was then dispersed on the substrate. The substrate was then rinsed, dried, and loaded in a chemical vapor deposition system. The substrates were annealed between 280 to 400 °C for 5 min in 100 Torr of flowing $H_2$. The time between the particle deposition and the onset of annealing was of the order of 10 min and was crucial to successful nanowire growth. Immediately after the annealing, Ge nanowire growth was carried out using 10 sccm of $GeH_4$ (5% diluted in $H_2$) and 40 sccm of $H_2$ at a total pressure of 100 Torr and a substrate temperature of 280 °C. This growth temperature was chosen because it was the minimum growth temperature at which nanowire growth could be achieved, as determined by systematically increasing the temperature from 265 °C. To investigate the effect of annealing, all Ge nanowires were grown in the same conditions, following only a variation in the annealing temperatures.

## III. RESULTS AND DISCUSSION

Figures 1(a) and 1(b) present scanning electron microscopy (SEM) images of Ge nanowires grown on a Si (111) substrate using annealing temperatures of 280 and 320 °C, respectively. The results are essentially the same for both conditions. The nanowires show uniform diameters without significant tapering along an average length of ~2.2 μm. Significantly, a majority of nanowires are found to be oriented perpendicular to the substrate, indicating epitaxial growth along the <111> growth direction. Additionally, a small fraction of nanowires which grew along other <111> directions were also observed: these as nanowires present at an angle of approximately 70° to the substrate normal in a cross-sectional view and have an angle of 120° between them when projected in plan-view.[14] Figures 1(d)–1(f) present transmission electron microscopy analysis of the Ge nanowires grown following annealing at 320 °C. These images confirm that the Ge nanowires are defect free over their entire length. The inset electron diffraction pattern—taken along the $\{\bar{1}12\}$ zone-axis orientation—indicates a <111> growth direction, consistent with the growth direction observed from SEM images. Collectively, these results demonstrate that Ge nanowires are heteroepitaxially grown on a Si (111) substrate successfully with both annealing and growth at deep subeutectic temperatures. In contrast, when the substrate was annealed above the eutectic temperature of 363 °C for Au–Si, in our case 400 °C, there was no successful nanowire growth, as shown in Fig. 1(c). This comparison suggests that an annealing temperature below

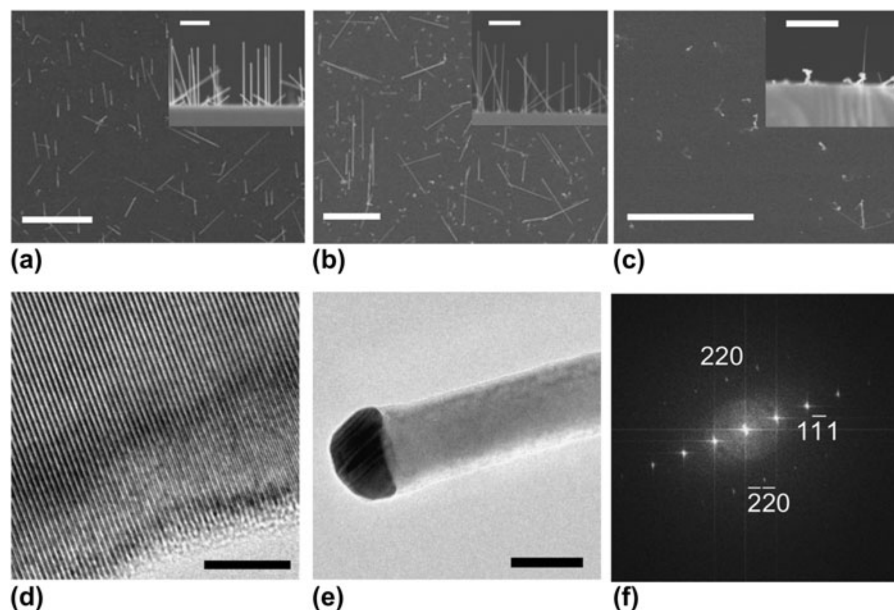


FIG. 1. Scanning electron microscopy (SEM) and high-resolution transmission electron microscopy (HRTEM) images of Ge nanowires grown on Si (111). Growth was carried out at 280 °C, with annealing at (a) 280, (b) 320, and (c) 400 °C. SEM images were taken with a 25° inclination from the plan-view (in a, b, and c) and in cross-sectional view (insets to a, b, and c). Scale bars are 5 μm in (a)–(c) and 2 μm in (a)–(c) insets. (d) HRTEM image, (e) bright-field TEM image, and (f) electron diffractogram of a Ge nanowire produced following annealing at 320 °C. Scale bars are 2 and 100 nm in (d) and (e), respectively.

the Au–Si eutectic temperature is critical for successful epitaxial growth of Ge nanowires on Si (111) substrates at a growth temperature of 280 °C.

Figure 2 illustrates our explanation of the mechanism by which annealing affects nanowire nucleation and the selection of nanowire orientation. It is known that the precleaning of Si substrates with buffered HF not only removes the native oxide but also creates a hydrogen-terminated surface that is stable in air for several minutes.[17] We postulate that the combination of substrate precleaning in buffered HF and the deposition of the colloidal Au nanoparticles in a dilute HF solution leads to intimate contact between the Au particles and the growth substrate in addition to enhanced deposition of Au colloid particles and removal of native oxide.[15] During subsequent annealing below the Au–Si eutectic temperature [Fig. 2(a)], one would expect very little reaction between the solid Au and the Si substrate, as Au is nearly insoluble to Si below the eutectic temperature, based on the equilibrium phase diagram. However, this low temperature anneal must be leading to the formation of a well-defined, homogeneous and planar <111> oriented interface between the Au solid and the Si substrate prior to introduction of the Ge growth precursor. This allows proper templating for the subsequent Ge nanowire nucleation event, consistent with our observations of predominantly vertically oriented nanowires. In comparison, annealing above the eutectic temperature (e.g., 400 °C) will result in the formation of a Au–Si eutectic liquid alloy (with approximately 19% Si), which develops facets below the substrate surfaces

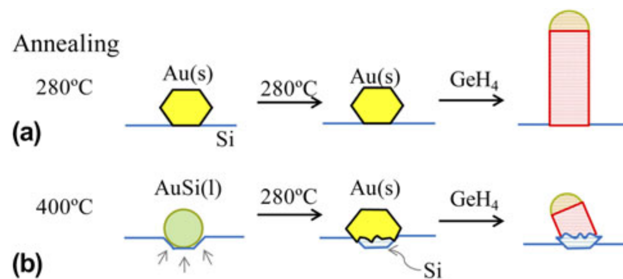


FIG. 2. Schematic illustration of the mechanism of Ge nucleation and growth on Si following annealing (a) below and (b) above the Au–Si eutectic temperature.

[the so-called "alloy-in" effect—Fig. 2(b)].[18,19] Upon subsequent lowering of the temperature below the eutectic temperature for growth (280 °C), a significant amount of Si will be rejected to the substrate during solidification, presumably templating onto the facets formed during annealing. Subsequent provision of Ge to the now-solidified Au–Si droplet via the $GeH_4$ precursor will result in nanowire nucleation with growth observed in arbitrary directions because of the nonuniform nature of the catalyst/substrate interface.

To confirm the critical role of a well-formed Au–Si interface prior to subeutectic Ge nanowire growth, we replicated these growth studies on substrates with a thick surface oxide (600 nm). Although presence of the oxide prevents the formation of Au–Si alloy during annealing above the eutectic temperature, the oxide will prevent the

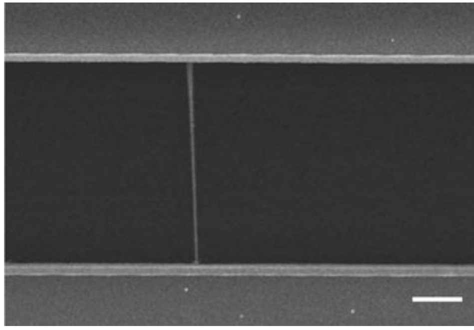

FIG. 3. SEM image of a Ge nanowire grown across a Si trench structure. Scale bar is 1 μm.

formation of a <111> Au/Si interface. As expected, similar results were observed following annealing both below and above the Au–Si eutectic temperature (Supplemental Information). The orientation of the Ge nanowires was found to be random, clearly indicating the failure of heteroepitaxial templating.

The improved understanding of the fundamental mechanisms of low temperature nanowire growth can be used to create novel and potentially useful structures. As shown in Fig. 3, we can utilize this same approach to growth nanowires in-plane. Si microtrenches with exposed {111} planes were fabricated following the method developed by He et al.[20,21] Heteroepitaxial growth of Ge nanowires in a <111> direction from the sidewalls of these trenches was achieved utilizing a 280 °C growth, following a 280 °C annealing, completely bridging the trench and leading to intimate contact (as determined via electrical measurements, not shown). These results demonstrate that this growth approach provides a nanowire device fabrication method requiring a low thermal budget and yet potentially offering the superior electronic properties of germanium.

## IV. CONCLUSIONS

In summary, our work demonstrates that it is possible to grow vertical, integrated Ge nanowires on silicon substrates with a two-step process, including annealing and growth, both at temperature of 280 °C, lower than previously reported. This is based on the creation of a single, ordered <111> interface between the Au and the Si, prior to Ge introduction. This work indicates that careful but relatively simple control of both substrate preparation and annealing and growth procedures can lead to heteroepitaxial growth of oriented, single crystalline Ge nanowires on Si completely below the eutectic temperature, with important ramifications for device creation.

## ACKNOWLEDGMENT

The work was supported by the Defense Advanced Research Project Agency award N66001-08-1-2037. S. J. P. thanks the support by the Korean Research Foundation Grant funded by the Korean Government (KRF-2007-357-D00022).

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## Supplementary Material

Supplementary material can be viewed in this issue of the *Journal of Materials Research* by visiting http://journals.cambridge.org/jmr.