

Laser direct synthesis of silicon nanowire field effect transistors

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Abstract

We demonstrate a single-step, laser-based technique to fabricate silicon nanowire field effect transistors. Boron-doped silicon nanowires are synthesized using a laser-direct-write chemical vapor deposition process, which can produce nanowires as small as 60 nm, far below the diffraction limit of the laser wavelength of 395 nm. In addition, the method has the advantages of *in situ* doping, catalyst-free growth, and precise control of nanowire position, orientation, and length. Silicon nanowires are directly fabricated on an insulating surface and ready for subsequent device fabrication without the need for transfer and alignment, thus greatly simplifying device fabrication processes. Schottky barrier nanowire field effect transistors with a back-gate configuration are fabricated from the laser-direct-written Si nanowires and electrically characterized.

Keywords: nanowire, laser chemical vaport deposition, field effect transistor

(Some figures may appear in colour only in the online journal)

1. Introduction

Since Si and Ge nanowires were first synthesized via the vapor–liquid–solid mechanism [1], semiconductor nanowires have attracted a great deal of attention due to their demonstrated potential for high-performance nanoscale devices such as transistors [2], sensors [3], solar cells [4], and thermoelectric systems [5]. The ultra-thin bodies of nanowires allow excellent electrostatic control which is required for high-performance electronic devices. The one-dimensional morphology of nanowires enables straightforward implementation of semicylindrical gate or gate-all-around architectures. However, despite these advantages, the difficulty in controlling the placement and orientation of these nanowires remains an obstacle for widespread applications of nanowire devices. Since ‘bottom-up’ nanowires are often produced as entangled mesh, additional fabrication procedures are required to position them for device fabrication. Various alignment techniques [6–9] have been attempted and achieved successful integration of nanowires into individual devices or small-scale circuits, but none of them has demonstrated the capability to create the high density and precision required for integrated

circuit manufacturing. Metal contamination from catalysts used for nanowire growth is another drawback. Alternative ‘top-down’ approaches do not have these shortcomings, but require complex, multiple fabrication steps for nanowire patterning, etching, and doping. Therefore, it will be meaningful to develop a simple and precise method to synthesize and position nanowires.

Material synthesis by laser heating has been demonstrated for photonic metamaterials [10], semiconductor pattern deposition [11], microelectronic [12, 13] and sensing applications [14]. Although these methods have advantages of flexibility and possible three-dimensional fabrication, the critical dimensions remained in the range of hundreds of nanometers due to the diffraction limit of light. On the other hand, it has been shown that direct writing of laser-induced periodic surface structures (LIPSS) can form feature sizes below the processing laser wavelength in nearly all kinds of materials [15–17], but the application of LIPSS has been limited to surface modification and material removal [18, 19].

In this work, we demonstrate a single-step method to fabricate doped silicon nanowires for silicon nanowire field effect transistors (SiNW FETs). Boron-doped silicon

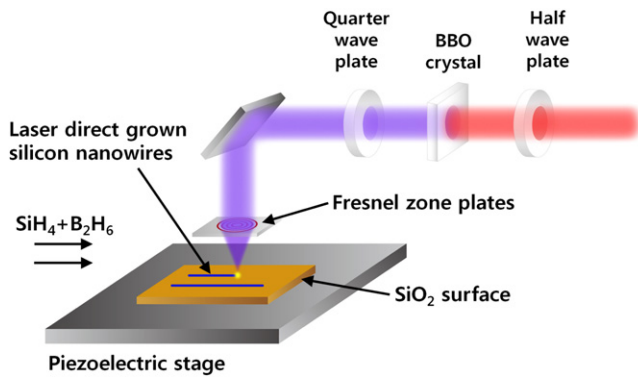


Figure 1. Schematic diagram of the laser-direct-write method. A laser beam is focused on a localized spot where a silicon nanowire is synthesized. Fresnel phase zone plates are used as a focusing element and there is a flow of silane and diborane in the laser CVD chamber.

nanowires are fabricated using a laser-direct-write chemical vapor deposition (CVD) method which we previously reported [20]. By combining laser synthesis of materials with the sub-diffraction feature sizes of LIPSS, our method overcomes scaling limitations of traditional laser-based CVD, resulting in nanowire diameters as small as 60 nm, far below the diffraction limit of the 395 nm laser wavelength we used. The method has advantages of both CVD and laser direct writing—*in situ* doping, catalyst-free growth, and precise control of nanowire position, orientation, and length. The silicon nanowires are directly deposited on an insulating SiO₂ surface and therefore ready for subsequent device fabrication without the need for transfer and alignment. SiNW FETs are fabricated from the laser-direct-written nanowires using standard micro-fabrication techniques. We characterize the electrical properties of fabricated FETs and demonstrate that our approach offers a simple and promising way to fabricate SiNW FETs.

2. Experimental details

Figure 1 shows a schematic diagram of the laser-direct-write CVD method. A laser beam is focused on a substrate to locally heat the surface and the thermal energy of the laser decomposes reactive gases on the laser spot. During the growth, the underlying substrate is translated by a piezoelectric stage to create silicon nanowires in a desired pattern. We used a femtosecond Ti:Sapphire laser which was frequency-doubled to 395 nm and Fresnel phase zone plates to focus the laser beam. Note that because the zone plates are flat and compact, they can be packed together in a small area and have potential for parallel writing of nanowires. The writing speed was 0.5–2 $\mu\text{m s}^{-1}$. The chamber pressure was 2.5 Torr with a flow rate of 10 sccm of 10% silane in argon and a flow rate of 0.025 sccm of 500 ppm diborane in hydrogen. The substrates used for nanowire growth were a 200 nm thick silicon dioxide top layer over a 200 nm thick polycrystalline silicon (poly-Si) layer on quartz. The silicon dioxide top layer

provides electrical isolation of nanowires for easy fabrication of electrical devices, while the underlying poly-Si layer serves as a back gate. The poly-Si layer was heavily doped with phosphorus using ion implantation in advance for high conductivity. Further details of nanowire growth as well as the methods of zone plate fabrication can be found in [20].

Once silicon nanowires are synthesized using the laser-direct-write CVD method, the nanowires were annealed at 800 °C for 6 h in N₂ to crystallize. Fabrication of nanowire FETs follows common micro-fabrication procedures. A contact hole was defined and etched on the 200 nm thick SiO₂ layer using buffered oxide etch (BOE) to create a contact to the underlying poly-Si layer which is used as a back gate. Ni source and drain contacts were then patterned and deposited by electron beam evaporation. Immediately before Ni evaporation, the patterned device chip was etched in BOE for 5 s to remove native oxide on the surface. The metallized devices were annealed at 350 °C in forming gas (4% H₂/96% N₂) for 1 min using rapid thermal annealing in order to form nickel silicide at the interfaces between the nanowires and the Ni electrodes. Electrical properties of the fabricated FETs were measured at ambient conditions with a Keithley 4200-SCS semiconductor parameter analyzer.

3. Results and discussion

Figure 2(a) shows a scanning electron microscope (SEM) image of a Si nanowire synthesized using the laser-direct-write CVD method. The diameter of the nanowire is 60 nm, which is less than 1/6 of the laser wavelength of 395 nm. A horizontally polarized laser light was used because nanowires form parallel to the direction of laser polarization. We emphasize that our nanowire formation process is not a conventional laser CVD which is limited by the diffraction limit of light, but involves the interference effect between the incident laser beam and the surface scattered laser radiation within a diffraction limited spot, which causes spatially confined, periodic heating needed for nanowire synthesis. The mechanism of the nanowire synthesis has been described previously [20]. The nanowire has a semicircular cross-section with a height of around 30 nm as shown in the transmission electron microscopy (TEM) image in figure 2(b). No periodic atomic structure is observed in figure 2(b), indicating that the as-synthesized nanowire is amorphous. The silicon oxide layer under the nanowire is completely intact which demonstrates that laser irradiation during the nanowire formation causes no damage on the oxide surface. The platinum layers over the nanowire were deposited for TEM sample preparation. Figures 2(c) and (d) show cross-section TEM images of nanowire annealed in N₂. Unintended oxidation of the outer shell of nanowire is observed in figure 2(c). To avoid oxidation, a nitrogen purge step was added before annealing and little oxidation in the nanowires was observed by comparing the diameters of nanowire before and after BOE etching. Grains of a few nanometers in size are observed in the annealed nanowire and this indicates that the nanowire was crystallized to poly-crystalline silicon.

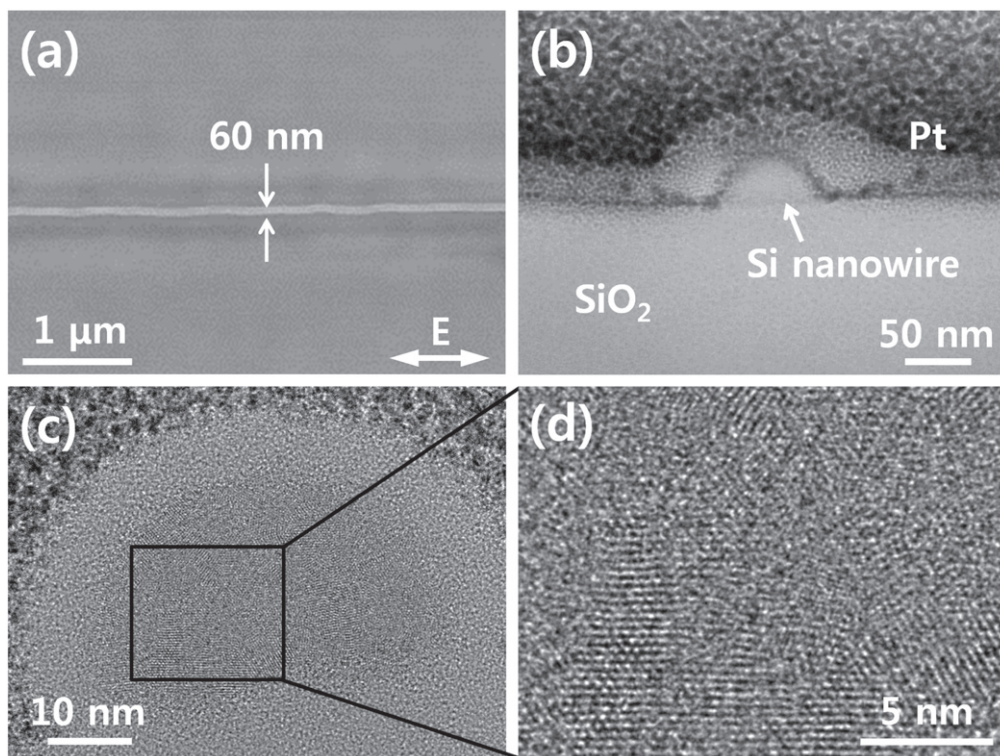


Figure 2. (a) SEM image of a laser-direct-written Si nanowire. The white arrow indicates the electric field polarization direction of the incident laser. (b) Cross-section TEM images of an as-deposited nanowire and (c), (d) annealed nanowire. The annealed nanowire was crystallized to polycrystalline silicon with grain sizes of a few nanometers. The Pt layers over the nanowire were deposited for TEM sample preparation.

Crystallization of amorphous silicon to single-crystalline silicon is unlikely to occur unless the annealing temperature increases significantly [21].

The electrical resistivity of the nanowire annealed at 800 °C is measured to be 66 Ωcm using a four-point measurement which minimizes the effect of contact resistance. The resistivity corresponds to the doping concentration of $2 \times 10^{14} \text{ cm}^{-3}$ in single-crystalline silicon [22]. However, the resistivity of poly-Si depends not only on doping concentration, but also on grain size, deposition method and temperature, and can be a few orders of magnitude greater than that of single-crystalline silicon due to carrier trapping states and dopant atom segregation in grain boundaries [23, 24]. Therefore, the doping concentration of $2 \times 10^{14} \text{ cm}^{-3}$ is the lower limit of the doping concentration of our nanowire and the actual doping concentration can be as high as 10^{17} cm^{-3} [23, 24]. Note that the diborane/silane ratio during the nanowire synthesis was 1:80 000 and this ratio corresponds to the boron concentration of $10^{17} \sim 10^{18} \text{ cm}^{-3}$ if considering the ratio of boron and silicon atoms.

Figure 3 shows an SEM image of a fabricated SiNW FET. In our work, Ni was chosen as a contact metal because nickel silicides are widely used as contacts for semiconductor nanowires [25–27] and are considered as midgap metals with a hole Schottky barrier (SB) height of 0.39–0.49 eV [26–28]. Since Ni is the dominant diffusing species in the Ni–Si reaction [27], the growth of nickel silicide along the nanowire is observed adjacent to the Ni electrodes in figure 3. The Ni

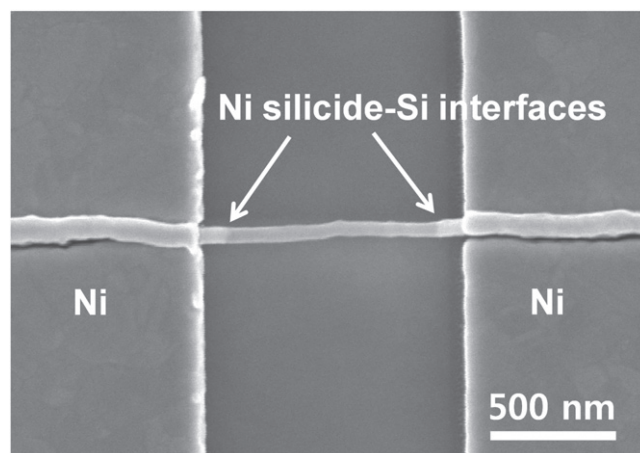


Figure 3. SEM image of a SiNW FET. Ni source/drain contacts are deposited on a laser-direct-written Si nanowire. Rapid thermal annealing leads to the axial diffusion of Ni along the nanowire and nickel silicide forms near the Ni pads.

silicide areas are brighter than the remaining Si nanowire area. Elongation of a Si nanowire which is often caused by the incorporation of Ni in Si was not observed in our work due to the relatively short lengths of nickel silicide.

Figure 4(a) shows the transfer characteristics of a laser-direct-written SiNW FET with a channel length of 1.8 μm. The drain current of the p-type device increases as a higher negative gate voltage is applied. Since the threshold voltage V_T is –0.91 V, determined by the linear extrapolation method,

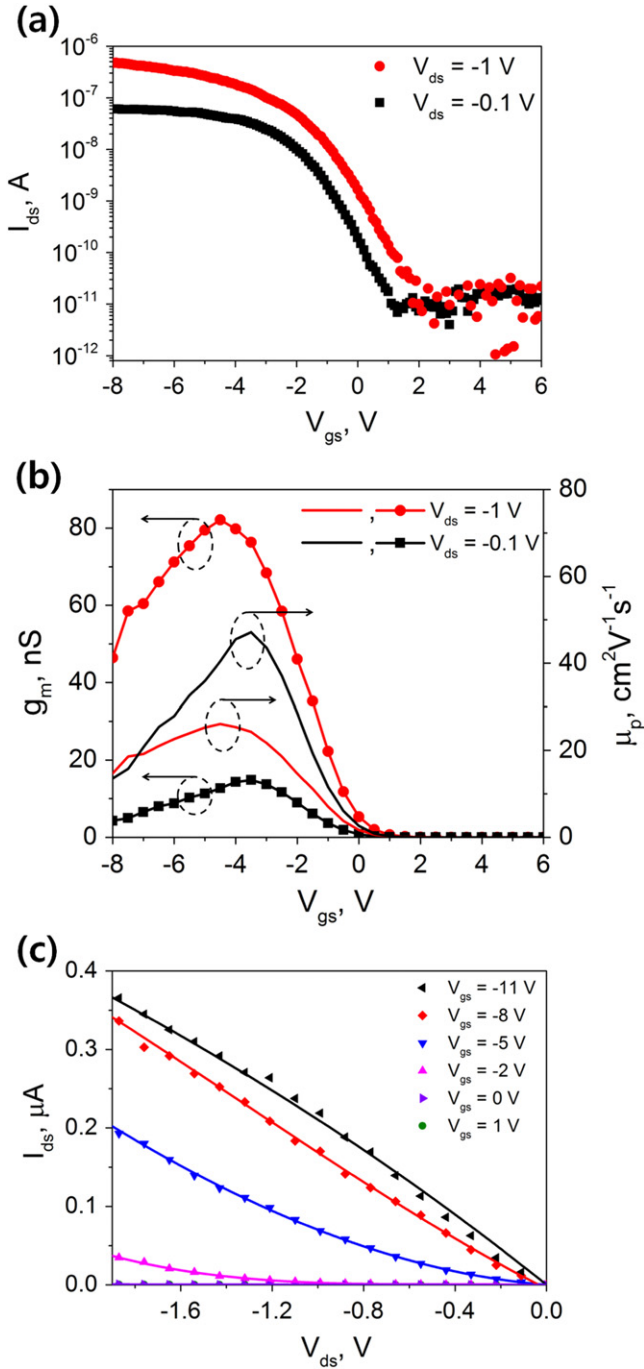


Figure 4. (a) Transfer (I_{ds} – V_{gs}) characteristics, (b) transconductance (g_m) and field-effect mobility (μ_p) versus gate voltage (V_{gs}), and (c) output (I_{ds} – V_{ds}) characteristics of a laser-direct-written SiNW FET with a channel length of $1.8 \mu\text{m}$. Solid lines are a guide for the eye.

the device is mainly operated in accumulation-mode. No inversion-mode characteristic is observed with a positive gate voltage, which is most likely due to the much higher SB height between the p-type Si nanowire and the Ni silicide for electrons (0.66–0.75 eV) than for holes (0.39–0.48 eV) [26–28]. The on–off ratio is larger than 10^4 and the on-current reaches $7.9 \mu\text{A} \mu\text{m}^{-1}$ at $V_{ds} = -1 \text{ V}$, which is within the same order of magnitude as on-current values previously reported in poly-Si NW FETs (12 – $40 \mu\text{A} \mu\text{m}^{-1}$) [29, 30]. The on-

current of our device is normalized by the diameter of the semi-circular nanowire. The maximum transconductance is 81.2 nS ($1.35 \mu\text{S} \mu\text{m}^{-1}$) at $V_{ds} = -1 \text{ V}$ and 15 nS ($0.25 \mu\text{S} \mu\text{m}^{-1}$) at $V_{ds} = -0.1 \text{ V}$ as shown in figure 4(b). The drain-induced barrier lowering (DIBL), which is defined as $\Delta V_{gs}/\Delta V_{ds}$ at $I_{ds} = 10^{-9} \text{ A}$, is measured to be 898 mV V^{-1} and the subthreshold swing (SS) is 860 mV dec^{-1} . The large DIBL and SS are in part attributed to the thick gate dielectric and SB transistor nature of the device.

The low-field mobility (μ_p) is calculated to be $47.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at $V_{ds} = -0.1 \text{ V}$ using the equation $\mu_p = g_m L^2 / C_{ox} V_{ds}$ with g_m as the maximum transconductance of the device, L as the channel length, and C_{ox} as the gate capacitance. The ‘metallic cylinder on an infinite metal plate model’ is often used to calculate the gate capacitance in typical back-gate NWFET geometries, yielding an analytical equation for the gate capacitance [31]:

$$C_{ox} = \frac{2\pi\epsilon_0\epsilon_{r,\text{eff}}L}{\ln(2t_{ox}/r)}, \quad (1)$$

where $\epsilon_{r,\text{eff}}$ is the effective dielectric constant of SiO_2 , t_{ox} is the thickness of the gate oxide, and r is the radius of the nanowire. However, equation (1) is inaccurate with the dielectric constant for SiO_2 of $\epsilon_r = 3.9$ unless an infinitely long, metallic nanowire is completely surrounded by the gate oxide. Therefore, we use an effective dielectric constant of $\epsilon_{r,\text{eff}} = 2.65$, which is calculated for a triangular nanowire on SiO_2 [31], and the gate capacitance is calculated to be 102 aF . Note that although the extracted mobility is comparable to a previously reported value of $52.7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in poly-Si NW transistors [29], the intrinsic mobility value of our device should be even higher if we consider the contact resistance induced by the SBs at the silicon/silicide interfaces. Hence, the electrical performance of the SiNW FET can be further improved by either heavily doping the source/drain regions or using low SB silicides. For example, platinum silicide provides a low SB of 0.23 eV for holes [32] while erbium silicide has a low barrier height of 0.28 eV for electrons [33].

Figure 4(c) shows the drain current I_{ds} versus drain voltage V_{ds} characteristics of the SiNW FET. The device shows an enhancement-mode operation and non-saturated drain current is observed, indicating the presence of Schottky source/drain contacts. The non-saturated drain current can be explained using the thinning of the SB width induced by drain voltage [33, 34]. With a negative gate voltage, the SB width at the source contact becomes thinner as a drain bias increases. The thinner SB allows more tunneling of holes across the barrier and the increased number of holes injected from the source results in the increase of drain current without saturation. This non-saturation behavior of drain current in SB SiNW FETs has been previously reported [26, 34].

4. Conclusion

In this work, we have demonstrated fabrication of SiNW FETs using a laser-direct-write CVD method. Nanowires far

below the diffraction limit with widths of 60 nm were synthesized using our single-step, laser-based approach and fabricated into SiNW FETs using standard micro-fabrication techniques. The direct deposition of Si nanowires at a desired location on an insulating surface as well as *in situ* doping greatly simplify device fabrication processes and thus facilitate integration of Si nanowires into FET devices. The fabricated device functioned as a SB transistor and enhancement-mode, p-type characteristics were demonstrated. We believe that our approach could be an alternative to fabricate future nanowire electronics.

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