KAUSHIK ROY

Roscoe H. George Professor of Electrical & Computer Engineering
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RESEARCH INTERESTS:

Nano-elctronic devices, Spintronics, Device/Circuit/Architecture Co-design
Low-power electronics, process variations and robust, high yield designs, Bio-electronics

EDUCATION:

Ph.D. (Jun. 1990)	Electrical & Computer Engineering, *University of Illinois at Urbana-Champaign* Thesis: Timing Verification and Synthesis of Robust Delay Fault Testable Circuits Advisor: Prof. Jacob Abraham
B.Tech. (May 1983)	Electronics & Electrical Engineering, *Indian Institute of Technology, Kharagpur*

WORK EXPERIENCE:

Jan. 2005 – present	Roscoe H. George Professor of ECE Purdue University
Aug. 2001 – 2005	Professor, School of Electrical & Computer Engineering Purdue University
Jul. 1997 – 2001	Associate Professor, School of Electrical & Computer Engineering Purdue University
Sep. 1999 – Dec. 1999	Visiting Faculty, EECS, University of California – Berkeley
Jul. 1999 – Aug. 1999	Visiting Faculty, Intel Corporation, Portland, Oregon
Aug. 1993 – Jun. 1997	Assistant Professor, School of Electrical & Computer Engineering Purdue University
Sep. 1997 – Dec. 1997	Visiting faculty at Intel Corporation, Portland, Oregon
Jun. 1996 – Jul. 1996	Visiting faculty at Intel Corporation, Santa Clara, California
Aug. 1990 – Aug. 1993	Member of Technical Staff in Semiconductor Process and Design Center Texas Instruments, Dallas Worked on Field Programmable Gate Arrays and on low-power electronics
Spring 1993	Adjunct Faculty, University of Texas at Dallas Taught Fault-Tolerant Computing
1992 – 1993	SRC (Semiconductor Research Corporation) Mentor Responsibilities included monitoring research on VLSI testing at the University of Texas at Austin and the University of Illinois at Urbana-Champaign.
1985 – 1990	University of Illinois, Graduate Research Assistant
Feb . 1989 – May 1989	Summer Intern, Texas Instruments, Dallas
May 1988 - Aug. 1988	Summer Intern, Texas Instruments, Dallas

AWARDS AND HONORS:

- Fellow, IEEE, since 2001.
- Humboldt Research Award, 2010.
- IEEE Circuits and Systems Society (CASS) Technical Achievement Award, 2011.
- Distinguished Alumnus Award, Indian Institute of Technology, Kharagpur, 2011.
- Semiconductor Research Corporation (SRC) Technical Excellence Award, 2005.
- Purdue College of Engineering Research Excellence Award, 2008.
- M.K. Gandhi Distinguished Visiting Faculty, Indian Institute of Technology. Mumbai, Jan. 2010.
- Motorola Research Visionary Board Member, 2002.
- Purdue University Faculty Scholar 1998.
- Roscoe H. George Professor of ECE.
- NSF CAREER development award, 1995.
- IBM Faculty Partnership Award, 2001.
- ATT/Lucent Foundation award, 1997.
- 2012 ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED) Best Paper Award for paper titled, "TapeCache: High Density, Energy Efficient Cache Based on Domain Wall Memory," August 2012.
- 2006 IEEE Transactions on VLSI Systems Best Paper Award for paper titled, A Process-Tolerant Cache Architecture for Improved Yield in Nanoscale Technologies," Jan. 2005.
- 2006 ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED) Best Paper Award for paper titled, Analysis of Super Cut-off Transistors for Ultralow Power Digital Logic Circuits
- Low Power Design Contest Award (with C. Kim and J. Kim) for "A Low-Power Embedded SRAM Cache with PVT-Aware Leakage Reduction and Improved Stability" in ISLPED 2005.
- 2005 IEEE Circuits and Systems Society Outstanding Young Author Award (Chris Kim) for paper titled, "Ultra-Low Power DLMS Adaptive Filter for Hearing Aid Applications" in IEEE Trans. on VLSI Systems.
- "A Novel Low-Power Scan Design Technique Using Supply Gating," Best paper award, *IEEE International Conference on Computer Design*, 2004.
- "Defect Oriented Testing of Analog Circuits Using Wavelet Analysis of Dynamic Current," Best paper award, *4th IEEE Latin American Test Workshop*, 2003.
- "Circuit-Compatible Modeling of Carbon Nanotube FETs in the Ballistic Limit of Performance," Best Student Paper Award, *IEEE NANO 2003*.
- "On Effective IDDQ Testing of Low-Voltage CMOS Circuits Using Leakage Control Techniques," Best paper award, *IEEE International Sympoisum on Quality of IC Design*, 2000.
- Technical Advisory Board, Zenasis Technologies.
- "Intrinsic leakage in low-power deep sub micron CMOS ICs," Honorable Mention Paper Award, *International Test Conference*, 1997.

- Recipient of National Scholarship (Government of India) 1977-78.
- Merit Scholarship (Indian Institute of Technology) 1979-83.

RESEARCH GRANTS AND CONTRACTS:

- IBM Corporation (Single Investigator), "Research on Synthesis for Low Power CMOS Logic," $100,000, (December 1993 – November 1995), Award No. 6712385.
- Advanced Research Projects Agency (Single Investigator), "Power Estimation and Synthesis for Low Power," $347,245, 03/21/95 – 07/20/98, Award No. F33615-95-C-1625.
- National Science Foundation (CAREER Development Award), "Integrated Framework for Test Synthesis, Power Optimization, and Reliable Design of VLSI Circuits," $90,000, 06/01/95 – 05/31/98, Award No. 9501869-MIP.
- National Science Foundation (Single Investigator), "Architectural Transformations to Achieve Low Power Consumption in VLSI Circuits," $10,000, 06/01/95 – 05/31/98, Award No. 9501869-MIP.
- National Research Council (Senior Investigator), "Efficient Use of Narrowband Radio Channels for Mobile Digital Communications," PI: Michael Fitz, 1994.
- Equipment grant from Intel, $10,154, October 1996, PI: KaushiK. Roy
- FPGA Equipment Grant to Support EE559 and Computer Engineering Research Activities, Texas Instruments Inc., Equipment worth $33,000, 1994.
- LSI Logic, ASIX VLSI tester, KaushiK. Roy, worth $250,000, January 1996.
- Intel Corporation (Single Investigator) "Differential Current Switch Logic," Intel Corporation, $66,000, 11/01/95 – 10/31/97, Award No. 6712575.
- Intel Corporation (Single Investigator) "Multiple Threshold Voltage and Dynamic Threshold Voltage Design Techniques for in Deep Sub-Micron Bulk and SOI Technology," $ 70,000 for 1 year starting Dec. 1997.
- Intel Corporation (Single Investigator) "Multiple Threshold Voltage and Dynamic Threshold Voltage Design Techniques for in Deep Sub-Micron Bulk and SOI Technology,"– equipment worth $ 13,768 for the project, Feb. 1998.
- National Science Foundation (Single Investigator), "Ultra Low Energy Computing using Adiabatic Switching Principle," $45,146, 1996-1997, Award No. 9633516-MIP.
- Advanced Research Projects Agency (Single Investigator), "Data Path Synthesis for Low-Power Using Dual-Gated SOI Transistors," $161,764, 06/01/96 – 05/31/99, Award No. DAAH04-96-1-0222.
- IBM Corporation (Single Investigator), "Datapath Synthesis for Ultra-low Energy Portable Applications," $ 50,000, 1996-1998.
- Rockwell Corporation (Single Investigator), "Low-Power Electronics for Portable Computing and Wireless Communications," $50,000, 10/02/96-10/01/98.
- AT&T/Lucent Technologies Special Purpose Grants in Science & Engineering (Single Investigator), "Low-Power Design Techniques for Portable Computing and Wireless Communications," $26,872, 1996-1998.
- Office of Naval Research (Single Investigator), "Low Power Electronics for Portable Computing and Wireless Communications," $86,534, Award No. N00014-97-1-0324, 1997.

- Lucent Technologies (Single Investigator), "Low-Power BIST," $30,000 for one year, starting Dec. 1997.
- Purdue Research Foundation (Single Investigator), "Power Dissipation and Performance Driven Logic Optimization," $30,600, 1994-1997.
- Semiconductor Research Corporation (Single Investigator), "Ultra Low Power Digital Logic Design," $440,000, Award No. 98-HJ-638 4 years staring September 1998.
- Intel Corporation (Single Investigator) "Multiple Threshold Voltage and Dynamic Threshold Voltage Design Techniques for in Deep Sub-Micron Bulk and SOI Technology (renewal)," $332,014, starting Dec. 1998 for three years.
- National Science Foundation (Single Investigator), "Subthreshold Digital Logic," $50,000, Award No. CCR-9901152.
- Semiconductor Research Corporation, Co-PI with Professor Cheng-Kok Koh, "On-Chip RLC Interconnect Synthesis," $384,000, Award No. 99-TJ-689, July 1 1999 – June 30 2002.
- Semiconductor Research Corporation, "Integrated Circuit Architecture Approach to Low-Power Memory Hierarchy Design," PI – KaushiK. Roy, Co-PI: Vijakumar and Babak Falsafi, $300,000 for three years starting Feb. 2000.
- Intel Corp., "SOI Circuit Design," (Single Investigator), $210,000 for three years starting May 2000.
- Intel Corp., "CAD for SOI Circuits," (Single Investigator), $25,000 for one year starting May 2000.
- Intel Corp., "Noise-Aware Floorplanning and Global Routing," (Co-PI's: C-K. Koh and K. Roy), $165,000 for three year starting August 2000.
- Semiconductor Research Corporation, "Low Power VLSI Signal Processing," (Single Investigator), $35,690, 08/01/00 to 07/31/01, Award No. 6741608.
- Agilent Technologies, "Leakage Power Management in Ultra High Performance Design," (Single Investigator), $60,000 for one year starting Dec. 2000.
- Gigascale Silicon Research Center (Uiversity of California – Berkeley) – DARPA/SRC Center, "Design and Test of High-Speed Scaled CMOS Circuits," $410,000 12/98 – 12/2003.
- IBM Faculty Partnership Award, $80,000, 2001.
- DARPA, "Mission Specific Processing," $884,927 for three years starting June 2001.
- DARPA, "Leakage Power Management in High Performance Systems," PI: KaushiK. Roy, Co-PI: T. Vijaykumar, $507,000 for 2.5 years starting April 2002.
- National Science Foundation, "Novel testing of CMOS Circuits Using Wavelet Transforms," PI: K. Roy, $160,000 for 4 years starting September 2002.
- NASA Nanoelectronic Center at Purdue (URETI), Director: S. Datta, Co-PI: KaushiK. Roy, $100,000/year + academic year support, 5 years starting December, 2002.
- National Science Foundation Center for Nano Computing, Director: M. Lundstrom, Co-PI: KaushiK. Roy, $75,000/year + academic year support, 5 years starting January 2003.
- DARPA, "Modulated Load Harmonic Reradiation for Low-Power Communication from Large Collections of Sensors," PI: M. R. Bell, co-PIs: C. A. Bouman, J. V. Krogmeier, C. P. Rosenberg,, K. Roy, N. Shroff, K. Webb, August 1, 2002 - July 31,2004, Contract No. MDA 972-02-1-0032, $450,000.
- Semiconductor Research Corporation, "Robust Circuits for Scaled CMOS Technologies," PI: K. Roy, $560,000 for period April, 2003 through December, 2007.

- MARCO Center (Giga Scale Silicon System Research, University of California), "Design and Test of Sacled CMOS Circuits," Co-PI: KaushiK. Roy $450,000 for three years starting August 2003.
- Semiconductor Research Corporation, "Tera-Scale Integration Using Carbon Nanotube Transistors," PI: K. Roy, Co-PI: M. Lundstrom, $40,000 for 1 year starting February, 2003.
- Semiconductor Research Corporation, "System-On-Chip for Power-Aware Wireless Communications," PI: K. Roy, $300,000 for three years starting October, 2003.
- Intel Corporation, "Nano-Circuit Simulation Laboratory," PI: K. Roy, $130,000 (October 2003).
- Intel Corporation/Semiconductor Research Corporation, "Designing with Unreliable Components," PI: K. Roy, $60,000 for a year starting August 2004.
- Motorola/Semiconductor Research Corporation, "Compact Models to Evaluate Asymmetric Double Gate Devices," PI: K. Roy, $25,000 for a year starting August 2004.
- National Science Foundation/ Semiconductor Research Corporation, "Integrated Framework for Reliability and Process Variation Aware Design Methodology for VLSI Circuits," PI: M. Alam, Co-PI: K. Roy, $470,000 for three years starting September 2004.
- Gigascale Silicon Research Center (Uiversity of California – Berkeley) – MARCO Center, "Error Resilient CMOS Circuits," $600,000 12/2005 – 12/2009.
- C2S2 (Circuits and Systems Research Center, Carnegie Mellon University), a MARCO Center, Double-Gate MOSFET Devices and Circuits, $300,000 08/2006 08/2009.
- Intel Corporation, Integrated Design and Test of Scaled CMOS Circuits, PI: Kaushik Roy, $45,000 gift, September 2006.
- Texas Instruments, Ultralow Power Digital Circuits, PI: Kaushik Roy, $50,000 gift, December 2006.
- Semiconductor Research Corporation, "An Integrated BIST, Diagnosis, Self-Repair and Adaptive Design Methodology for Highly Reliable Nano-Scale Systems," PI: K. Roy, Start date Oct 1 2007, $330,000 for 3 years.
- DARPA, "Ultra-Low-Power and Low-Cost Systems Using Optimized Poly-Si Thin- Film-Transistors," PI: K. Roy, $200,000 for two years, 2007.
- Semiconductor Research Corporation, Ultralow Power System Design Using Subthreshold Operations, PI: K. Roy, $180,000 for 3 years starting August 2007.
- National Science Foundation, PI: K. Roy, co-PI: M. Thottethodi, $361,264 for 3 years starting Oct. 1, 2007. Award number CCF-0702612
- Boeing, Process Adaptive Sub-Threshold Logic and Memory, PI: K. Roy, $108,000, 01/01//2008 12/22/2008.
- Intel Corporation, "Hybrid III-V/Si Devices for Enhanced Performance," PI: K. Roy, $35,000, December 2008.
- Intel Corporation, "High-Speed Nano-devices Simulation Cluster," $85,000 of computers, December 2008.
- NASA SBIR with RNET technologies, "Phase I: Radiation Mitigation Methods for Reprogrammable FPGA, Contract Number: NNX09CF29P," K. Roy's share: $33,000 for a year, starting February 2009.
- DARPA SBIR with RNET technologies, "Phase I: Innovative Approaches to Low Power, Sub-Threshold Electronic Circuits," K. Roy's share: $33,000 for a year, starting March 2009.

- Cyberonics, Inc., PI: P. Irazoqui, Co-PIs: K. Roy, and J. Rickus, "Core Technology Development Plan for Seizure Detection and Mitigationfor Cyberonics Next-Generation Devices," $ 1,200,000, 12/1/09-11/30/12.
- NASA SBIR with RNET technologies, "Phase II: Radiation Mitigation Methods for Reprogrammable FPGA," K. Roy's share: $200,000 for 2 years, starting April 2010.
- DARPA SBIR with RNET technologies, "Phase I: Ultra Low Power-Rad-Hard SRAM" K. Roy's share: $33,000 for a year, starting April 2010.
- National Science Foundation, PI: B. Jung, Co-PI: K. Roy and S. Bhunia (Case Western University) "SHF: Medium: Collaborative Research: System Level Self Correction Using On-Chip Micro Sensor Network and Autonomous Feedback Control," $ 900,000, three years, starting July 2010.
- Qualcomm Inc., PI: K. Roy, "STT-MRAM Research Engagement," $70,000, Project Period: 06/15/10-06/14/11.
- Qualcomm Inc., PI: K. Roy, "STT-MRAM Research Engagement," $55,000, gift money, 06/2010.
- National Science Foundation, PI: K. Roy, Co-PI: B. Jung, "SHF:Small: Standardized On-line Test and Verification Architecture Using TFTs on Glass and Inductive Wireless Links," $ 450,000, three years, starting July 2010.
- National Science Foundation, PI: A. Raghunathan, Co-PI: K. Roy, "CSR: Small: Scalable Effort Design: Exploiting Algorithmic Resilience for Energy Efficiency," $ 500,000, three years, starting July 2010.
- Intel Corporation, PI: K. Roy, Co-PI: M. Lundstrom, A. Raghunathan, C. Kim, S. Datta, and D. Markovic, "Post-CMOS Devices and Architecture," $ 300,000 (gift) for a year starting November 2010.
- Intel Corporation, PI: K. Roy, Co-PI: M. Lundstrom, A. Raghunathan, "Post-CMOS Devices and Architecture," $ 180,000 (gift) for a year starting November 2011 for a year.
- Index Center/ Nano Research Initiative, PI: J. Appenzeller, Co-PI: S. Datta, K. Roy, Z. Chen, P. Ye, "All Spin Logic," $ 450,000/ year for two years, starting January 2011.
- Boeing (and Dpeartment of Defense), PI: K. Roy, "Modeling and Impact of TDDB on Mixed-Signal Circuits," $103,835/ year, November 2011 – December 2012.
- Semiconductor Research Corporation, PI: K. Roy, "Low-Power Reliable STT-MRAMs: MTJStacks, Bit-Cells, and Architecture," $300,000 for three years starting January 2012.

PROFESSIONAL SOCIETY ACTIVITIES:

- Guest Editor, *IEEE Design and Test of Computers*, special issue on Low-Power VLSI Design, Winter 1994.
- Guest Editor, *IEEE Transactions on VLSI Systems*, special issue on Low-Power Design, June 2000.
- Guest Editor, *IEE Proceedings: Computers and Digital Techniques*, Special issue on "Low-power systems-on-chip," July 2002.
- Guest Editor, *IEEE Transactions on Circuits and Systems*, Special issue on "Nano-electronic circuits and systems," November 2007.
- Guest Editor, *IEEE Journal of Emerging and Selected Topics in Circuits and Systems*, Special issue on "Advances in Design of Energy-Efficient Circuits and Systems," June 2011.

- Guest Editor, *IEEE Sensors Journal*, Special issue on "Low Energy Systems", to appear in summer 2011.
- Editor, *IEEE Transactions on Electron Devices*, 2011 – present.
- Associate Editor, *IEEE Transactions on Circuits and Systems – I*, August 1997- July 1999.
- Associate Editor, *IEEE Transactions on VLSI Systems*, 1999 – 2001.
- Associate Editor, *IEEE Design and Test of Computers*, 1995 – present.
- Associate Editor, *IEEE Signal Processing Letters*, 2002 – 2003.
- Associate Editor, *IEEE Transactions on Circuits and Systems I*, 2006 present.
- Executive Committee Member Design Community Chair, *IEEE/ACM Design Automation Conference*, 2006-2008.
- Executive Committee Member – *IEEE/ACM International Symposium on Low Power Electronics and Design*, 2006-present.
- Technical Program Chair, *ACM/IEEE International Symposium on Low Power Electronics and Design*, August 2004.
- Technical Program Chair, *International Symposium on On-line Testing*, 2005.
- General Chair, *ACM/IEEE International Symposium on Low Power Electronics and Design*, August 2005.
- Technical Program Chair, *IEEE VLSI Design Conference*, January 2005.
- Program Chair, *IEEE Great Lakes Symposium on VLSI*, March 2000.
- General Chair, *IEEE Great Lakes Symposium on VLSI*, March 2001.
- IEEE Students Counselor, Purdue University, 1995 – 1997.
- Publicity Chair, *12th IEEE VLSI Test Symposium*, 1994.
- Finance Chair, *13th IEEE VLSI Test Symposium*, 1995.
- Finance Chair, *14th IEEE VLSI Test Symposium*, 1996.
- Steering/Advisory Committee, *IEEE 1st International Symp. on Quality of Electronic Design*, 2000, 2001, 2002 & 2003.
- Program Committee Member, *IEEE International Conference on Computer Design*, 1995-1996.
- Program Committee Member, *IEEE VLSI Test Symposium*, 1994-1997, 2004, 2005.
- Program Committee Member, *IEEE VLSI Conference*, 1997-1999, 2001-2005.
- Program Committee Member, *IEEE Great Lakes Symp. on VLSI*, 1999, 2000, 2001, 2002, 2003.
- Program Committee Member, *ACM/IEEE International Conference on Computer-Aided Design, ICCAD*, 1997, 1998, & 1999.
- Program Committee Member, *ACM International Conference on Low Power Electronics and Design*, 1998, 1999, 2000, 2001, 2002, 2003, 2004, 2005.
- Program Committee Member, *1999 Power and Timing Optimization Workshop (PATMOS).*
- Program Committee Member, *1999 Microelectronic Education Conference*, Arlington, VA.

- Program Committee Member, *IEEE International Symposium On-line Testing*, 2000 – present.
- Program Committee, 2000 Workshop on "Compilers and Operating Systems for Low Power," held in conjunction with International Conference on Parallel Architectures and Compilation Techniques, 2000.
- Program Committee, *2001 IEEE Computer Society International Conference on Microelectronic Systems Education.*
- Program Committee, *DATE (Design and Test in Europe)* 2001, 2002, 2003, 2004, 2005.
- Program Committee, *International Symposium on Circuits and Systems*, 2002, 2003.
- Program Committee, *ACM/IEEE Design Automation Conference*, 2002, 2003, 2004.
- Program Committee, *IEEE VLSI Circuit Symposium*, 2003, 2004, 2005.
- Program Committee, *SPIE's First International Symposium on Microtechnologies for the New Millennium 2003, 2005*, Maspalomas, Gran Canaria, Spain.
- Member of *IEEE, ACM,* and *Phi Kappa Phi*

INVITED LECTURES AND TUTORIALS AND PLENARY/KEYNOTES:

Keynotes/Plenary/Forum Talks

- "Low Power IC Design," *Keynote Talk*, Low Power VLSI kick-off meeting for German NSF, Nov. 5, 1999.
- "Deep-Submicron Leakage: Future Trends and Possible Solutions," Keynote talk, Low Leakage Conference, Texas Instruments, October 24, 2001.
- "Design and Test Considerations for Scaled Technologies," *Keynote talk*, *IEEE Latin American Test Workshop*, 2004.
- "Integration of Design and Test in the Nano-Scale Era: Wishful Thinking or Reality?" *Keynote Talk* , *IEEE Latin American Test Workshop*, March 2009.
- "Technology Scaling and Challenges for Ultralow Voltage Design," Invited Presentation at *2009 International Solid State Circuits Conference (ISSCC)*, Low Voltage Forum, February 8, 2009, San Francisco, California.
- "Ultra-Dynamic Voltage Scaling: Power Dissipation, Error Resiliency, and Yield", *Keynote talk*, ST Microelectronics Conference, Noida, India, February 3, 2010.
- "Emerging Technologies: Prospects and Perspective," *Keynote talk*, *2011 IEEE VLSi Conference*, Chennai, India, January 2011.
- "Computing with Spin as a State Variable," International Symposium on Integrated Circuits (Singapore, December, 2011)
- "Spin as State Variable for Computation: Prospects and Perspectives," *ACM/IEEE International Conference on Low Power Electronics and Design*," August 1, 2012.

Invited Talks and Invited Tutorials

- Invited to present lecture on "Power Analysis and Design at System Level: Notebook Computers" and "Software Power Optimization," at the *NATO Advanced Studies Institute* on "Low Power Design in Deep Submicron Electronics," (Lucca, Italy), August 20-30 1996.

- "Channel Architecture Synthesis for Row-Based FPGAs," in *Advanced Routing of Electronic Modules*, University of Maryland, CALCE Electronic Packaging Research Center, Sept. 1995.
- "Low-Power Electronics," *Georgia Institute of Technology*, April 1995.
- "Power Estimation and Synthesis for Low-Power," *Computer Science Colloquium at Purdue University*, March 1994.
- One day tutorial on "Low-Power IC Design," *ACM Design Automation Conference* (Anaheim, California), June 1997, with Dr. Brock Barton (TI) and Prof. Sayfe Kiaei (Oregon State University).
- Educational session on "Low-Power IC Design," *IEEE Custom Integrated Circuits Conference* (Santa Clara, California), May 1997.
- Invited to be a panel member to discuss "Future Needs and Directions in CAD," at the *IEEE Intl. Symp. on Circuits and Systems* (Atlanta, Georgia), May 15, 1996.
- Invited to be a panel member to discuss "Low Voltage Design," *IEEE International Conference on Computer Design (ICCD)* (Austin, Texas), October 7-9, 1996.
- One day tutorial on "Architecture and CAD Issues in FPGA's," *International Conference on VLSI Design* (New Delhi, India), January 1995, with Mahesh Mehendale (Texas Instruments).
- One day tutorial on "Low Power VLSI Design," *International Conference on VLSI Design* (Bangalore, India), January 1996, with Rabindra K. Roy (NEC Research).
- Tutorial on "Low-Power Design," *European Design and Test Conference* (Paris, France), March 1996.
- Tutorial on "Low-Power Design," *IEEE International Symposium on Circuits and Systems* (Atlanta, Georgia), May 1996, with Rabindra K. Roy (NEC Research).
- Tutorial on "Low-Power Design," *IEEE ASIC Conference* (Rochester, New York), September 23, 1996, with Rabindra K. Roy (NEC Research).
- Tutorial on "Low-Power Design," *IEEE Intl. Conf. on Computer Design*, (Austin, Texas), October 1996, with Rabindra K. Roy (NEC Research).
- "Design of Low-Power High-Performance Circuits," *1996 Annual Workshop on VLSI* Clearwater, Florida.
- Tutorial on "Low-Power Design," *IEEE Intl. Conf. on Electronics, Circuits, and Systems* (Rhodes, Greece), October 13-16, 1996.
- Tutorial on "Design of Low-Power Digital and Analog Systems," *IEEE VLSI Conference* (Hyderabad, India), Jan. 1997, with R. Harjani (University of Minnesota) and R. Roy (NEC Research).
- Tutorial on "Low Power Design of Digital CMOS LSI," *1997 Asia & South Pacific Design Automation Conference - ASP-DAC* (Chiba, Japan), Jan. 28, 1997.
- Invited to present a one day course on "Low Power Design," at *Ecole Poly de Montreal* (Montreal, Canada), February 14, 1997.
- Invited to present a one day course on "Low Power Design," at Kodak, (Rochester, New York), February 7, 1997.
- Visiting faculty, Sep. 1997, Lulea University of Technology, Sweden.
- Tutorial on "Low Power IC Design," *7th International Symposium on IC Technology, Systems & Applications* (Singapore, Sep. 1997).

- "Design of Low-Power Circuits," *Ericsson*, Lund, Sweden, Sept. 19, 1997.
- Tutorial on "Low Power IC Design," *5th Internal Conference on VLSI and CAD* (Seoul, Korea, Oct. 1997)
- "Programmable DSP," *IEEE VLSI Conference*, Chennai, India, Jan. 1998.
- "Low-Power VLSI: Design, Technology, and CAD," *1998 Asia & South Pacific Design Automation Conference - ASP-DAC*, (Yokohama, Japan, Feb. 1998).
- "Low-Power Circuit Techniques," *Invited tutorial at IEEE Custom Integrated Circuits Conference*, May 1998.
- "Low-Power System Design," *IEEE VLSI Design*, Goa, India, with A. Raghunathan (NEC) and S. Dey (University of California, San Diego).
- "VLSI Signal Processing using FPGA's," *IEEE VLSI Design*, Goa, India, with Sudip Nag (Xilinx Corporation).
- "Design and Optimization for Low-Leakage with Multiple Threshold CMOS," *Invited talk at International Workshop on Power and Timing Modeling, Optimization and Simulation*, Lyngby, Denmark, October 7, 1998.
- "Low Energy Computing for Portable and Wireless Applications," *Invited Talk at NORCHIP Conference & Ericsson*, Lund, Sweden, Nov. 10, 1998.
- "Low Power IC Design," *Two day short course at Lund University*, Lund, Sweden, Nov. 11-12, 1998.
- "Low Power CMOS Digital Design," *8th International Symposium on Integrated Circuits, Devices, and Systems*, Sep. 1999, Singapore.
- "Low Power VLSI Signal Processing," Computer Science Department, University of Hamburg, Germany, Nov. 6, 1999.
- "Low Power VLSI Signal Processing," *IEEE VLSI Conference*, Jan. 2000, Calcutta, India.
- "Low Voltage CMOS," invited talk at IBM T. J. Watson Research.
- "System Level Low-Power Design," *IEEE/ACM Design Automation Conference*, tutorial presentation, June 2000.
- "Low Voltage CMOS Design," *IEEE International Symposium on Circuits and Systems*, tutorial presentation, May 6, 2001, Sydney.
- "Low Power Design Techniques," *ACM Design Automation Summer School*, short course, May 21, 2001, Hyanisport.
- "Low Voltage CMOS Design," *International Symposium on Integrated Circuits, Devices, and Systems*, invited tutorial, September 5, 2001, Singapore.
- "Design and Test of Low Voltage CMOS Circuits," *IEEE International Test Conference*, full day tutorial, Baltimore, October 28, 2001.
- "Low Voltage CMOS Design and Test," *Design and Test in Europe*, Tutorial presentation, Munich, March 2002.
- "Leakage Tolerant CMOS Design," *IEEE Custom Integrated Circuits Conference*, Invited tutorial presentation, Orlando, May 2002.
- "Leakage Tolerant CMOS Design," *VLSI Circuits Symposium*, Tutorial presentation, June 2002.

- " Low-Power Design," Invited short course presentation in ACM organized short course in Latin America, November 2002, Porto Alegre, Brazil.
- "Low-Power CMOS Design," *IEEE VLSI Design Conference*, Tuorial Presentation, January 2003.
- "Leakage Tolerant Design," *IEEE International Symposium on Circuits and Systems*, Tutorial Presentation, May 2003.
- "Design of Scaled CMOS Circuits for Low-Leakage," *IEEE Custom Integrated Circuits Conference*, San Jose, September 2003.
- "Design of Scaled CMOS Circuits for Low-Leakage," *IEEE SOC Conference*, Portland, September 2003.
- "Design of Nano-scale CMOS Circuits," Full day tutorial, *ISIC-2004*, September, 2004.
- "Design of Nano-scale CMOS Circuits," Short course in Brazil (Porto de Gahlinas), Sponsored by the Brazilian National Science Foundation (cNPQ), Catholic University, Porto Allegre, 2004.
- "Design Considerations for the Nano-Scale Regime: Device, Circuit, Architecture Perspective," ECE Colloqium, University of Minnesota, February 2005.
- "Design Considerations for the Nano-Scale Regime: Device, Circuit, Architecture Perspective," invited lecture in Austin Conference on Energy Efficient Design (ACEED), sposored by IBM, February 2005.
- "Design Considerations for the Nano-Scale Regime: Device, Circuit, Architecture Perspective," half day workshop on Circuits and Systems, University of California - Irvine, April 2005.
- "Low-Power System Design," nVidia, February 2006.
- "Low-Power Design of Scaled CMOS Circuits," ECE, Distinguished lecture at the University of Maryland, 2006.
- "Low-Power Design of Scaled CMOS Circuits," ECE, Distinguished lecture at the University of Southern California, 2006.
- "Low-Power Design of Scaled CMOS Circuits," ECE, Distinguished lecture at UT-Austin, 2006.
- "Low-Leakage Electronic System Design," 7-day short course at Texas Instruments, Bangalore.
- "Design of Nano-Scale CMOS: From devices to Circuits," Invited lecture at Intel, Haifa, July 2006.
- "Design of Nano-Scale CMOS: From devices to Circuits," Invited lecture at the PowerWall Forum, Intel, Hillsboro, August 2006.
- "Process Tolerant Design of Nano-scale CMOS Circuits," Invited lecture, ECE, Carnegie Mellon University, October 2006.
- "Process Variation Tolerant System design", *Invited lecture at Intel PowerWall Forum*, 2007.
- "Low-Power Process-Tolerant System design in the Nano-Scale Era," *IBM TJ Watson Experts Workshop*, November 2007.
- "Low-Power design under Parameter Variations," *International Symposium on Low Power Electronics and Design*,"Embedded Tutorial, August, 2008, Bangalore, India.
- "Low-Power and variation Tolerant Electronics," Kenote Presentation, *6th IEEE East-West Design and Test Symposium (EWDTS)*, October 2009, Lviv, Ukraine.
- "Ultra Low Voltage CMOS," Invited Presentation, *2008 VLSI SoC Conference*, October 2009, Rhodes, Greece.

- "Device/Circuit Interactions at the 22nm Technology Node," Tutorial Presentation at *2008 IEEE Electron Devices Meeting (IEDM)*, December 2008, San Francisco, California.
- "Process Variations & Process -Adaptive Design for the Nano-meter Regime," *2009 Asia & South Pacific Design Automation Conference Design Forum*, January 2009.
- "'Robust SRAMs in sub-45nm Technology," *ISQED Tutorial*, March 2009.
- "Process Adaptive Design," & "'Ultralow Power Design," *University of Catalunya – Barcelona*, Inivited lectures and interactions, June 2009.
- "Low-Power SOC Design: State of the Art and Directions," Tutorial Presentation, *ACM Design Automation Conference*, July 27, 2009.
- "Design of CMOS Circuits in the Nano-scale Regime," *IEEE TTTC organized Summer school presentation*, Florianapolis, Brazil, May 7-9, 2010.
- "New Design Paradigms for Low-Power Systems," *SRC/ATIC/NSF Forum on Minimum Energy Electronic Systems (MEES 2020)*, Invited presentation, May 23-24, 2010.
- "Integrated Systems with Heterogeneous Devices," *3D System Integration Workshop*, Georgia Tech., Atlanta, Invited presentation, June 14, 2010.
- "Towards Zero Test Cost," *Intel Forum on Test and Verification of IC's*, Invited Talk, Santa Clara, California, November 2010.
- "Error Resilient System Design," *Tutorial Talk at the 2011 IEEE VLSI Conference*, Chennai, India, January 2011.

OTHER ACTIVITIES:

- IEEE Students Advisor, Purdue University, 1995 – 1997.
- Organized the IEEE student paper contest for undergraduates, April 1995 (sponsored by Sprint).
- Organized the IEEE student paper contest for undergraduates, April 1996 (sponsored by Sprint).
- Organized the IEEE student paper contest for undergraduates, April 1997 (sponsored by Sprint).
- Vice-General Chair, Purdue University ECE Industrial Affiliates Workshop, 1998.
- General Chair, Purdue University ECE Industrial Affiliates Workshop, 1999.

ADMINISTRATIVE SERVICES TO UNIVERSITY:

- VLSI and Circuit Design area chair, 1994 – 2001; 2007-present.
- Graduate Admissions Committee, 1998 and 1999.
- Computer Engineering area committee, member, 1993-present.
- Computer Engineering Chaired Professor Search Committee, 1996.
- QE (Qualifying Exam.) Committee, 1996-1997.
- IEEE Student Branch Advisor, 1995 – 1997.
- Faculty grievances committee member, 1995 & 1996.

- Dean's Research Advisory Committee, 1997.
- Awards Committee, 2002-2003.
- Space Management Comittee, 2003.

TEACHING EXPERIENCE:

1. Taught the following courses at Purdue University:
   - MOS VLSI Design (EE559)
   - VLSI Testing and Verification (EE695K)
   - Computer Architecture (EE 565)
2. Developed VLSI Testing and Verification course (EE695K) for the first time. Now it has a permanent number EE 688.
3. Developed an Advanced VLSI course (EE695KR) with Professor Koh. Course was taught in Spring 2000.
4. Taught the following course at University of Texas at Dallas (Adjunct Faculty):
   - Fault-Tolerant Computing (Spring '93)

GRADUATE STUDENT SUPERVISION:

Ph.D. Theses Supervised:

1. Tan-Li Chou, *Accurate Power Estimation of CMOS Digital Circuits And Its Applications to Low-Power Digital Logic Synthesis*, Sep. 1996. Currently at Intel Corp., Hillsboro, Oregon.
2. Yibin Ye, *Design and Synthesis of Adiabatic Switching Circuits*, Aug. 1997. Currently at Intel Corp., Hillsboro, Oregon.
3. Chuan-Yu Wang, *Estimation of Maximum Power for CMOS Digital Circuits*, Aug. 1997. Currently Synopsys Corp., Mountain View, California.
4. Mark Johnson, *Design Optimizations to Facilitate Rduction of Supply Voltage and Threshold Voltage in CMOS Logic*, Jun. 1998. Currently Lab Manager for Digital and Systems Laboratories at Purdue University, Indiana.
5. Khurram Muhammad, *Algorithmic and Architectural Techniques for Low Power Digital Signal Processing*, Mar. 1999. Currently at Texas Instruments, Dallas.
6. Zhanping Chen, *Accurate Power Estimation in Low Voltage CMOS with Application to Circuit Design and Testing*, Mar. 1999. Currently at Intel Corp.
7. Dinesh Somasekhar, *Power and Dynamic Noise Consideration in High Performance CMOS VLSI*, Jul. 1999. Currently at Intel Corp., Hillsboro, Oregon.
8. Xiaodong Zhang, *Low Power BIST*, Oct. 1999, Currently at Synopsys, Mountain View, California.
9. Ali Keshavarzi, *Testing Solutions for Intrinsically Leaky CMOS Integrated Circuits*, Aug. 2000, Currently at Intel Corp., Hillsboro, Oregon.

10. Liqiong Wei, *Design and Optimization of Multiple Threshold CMOS for Low Power and High Performance Applications*, Nov. 1999, Currently at Intel Corp., Hillsboro, Oregon.

11. Hendrawan Soeleman, *Ultra Low Power Digital Sub-threshold Logic*, August 2000, Currently at Sun Microsystems, Mountain View, California.

12. Rongtian Zhang, *Low-Power High-Performance SOI Circuit Design*, July 2001, Currently at SGI, California.

13. Shiyou Zhao, *Power Supply Noise Analysis for Deep Submicron VLSI Circuits*, August 2001, Currently at Micron, Idaho.

14. Yonghee Im, *Design of Robust CMOS Circuits for Scaled Technologies*, December 2002, Currently at Sun Microsystems, California.

15. Lih-Yih Chiou, *Synthesis of Application-Specific Multi-Mode Systems for Low-Power Applications*, May 2003, Assistant Professor,National Cheng Kung University, Tainan, Taiwan.

16. Naran Sirisantana, *High-Performance Low-Power CMOS Circuits Using Multiple Channel Length and Multiple Oxide Thickness* , December 2003, Intel Corporation.

17. Seung-Hoon Choi, *Analysis and Design of CMOS VLSI Considering Uncertainties in Circuit Parameters*, December 2003, Intel Corporation.

18. Jae-Joon Kim, *Circuit Design for Silicon-On-Insulator (SOI) CMOS Technologies,* May 2004, IBM TJ Watson Research.

19. Cassondra Crotty Neau, *Exploring Device and Circuit Architecture for Scaled Technologies,* August 2004.

20. Chris Hyung-Il Kim, *Design of High Performance, Low Power VLSI Circuits for Scaled Technologies,* August 2004, Assistant Professor, University of Minnesota, Minneapolis.

21. Hai Li, *Low Power Design Techniques at Architectural Level,* August 2004, Assistant Professor of ECE, New York University.

22. Woopyo Jeong, *Robust and Higly Efficient Datapath Design in Scaled CMOS Technologies,* December 2005, Samsung.

23. Dongku Kang, *Low-Power and Layout-Aware Data-Path Synthesis for Nanometer Technologies,* December 2005, Samsung.

24. Hunsoo Choo, *Low Power Methodology for Digital Signal Processing and Multimedia Applications*, May 2005, Texas Instruments, Dallas, Texas.

25. Yongtao Wang, *Algorithm and Architectural Low-Power Techniques for Digital Signal Processing and Wireless Communication Applications*, August 2005, Texas Instruments, Dallas, Texas.

26. Yiran Chen, *Design Techniques for Power-Efficiency and Robustness in Scaled High-Performance Systems*, August 2005, currently Assistant Professor of ECE, University of Pittsburgh.

27. Hamid Mahmoodi, *Low Power, Robust, and High Performance Circuit Design in Nano-Scale CMOS*, Assistant Professor, San Francisco State University, San Francisco, California.

28. Swarup Bhunia, *Power and Yield-Aware Design and Test of Nano-Scale CMOS Circuits*, August 2005, Assistant Professor, Case Western University, Cleveland, Ohio.

29. Amit Agarwal, *Process Variation Aware High Performance and Low Power VLSI System Design in Nano-Scale Regime*, September 2005, Circuits Research Laboratory, Intel, Hillsboro, Oregon.

30. Mark M Budnik, *A Distributed Power delivery and Decoupling Network Minimizing Ohmic Loss and Supply Voltage Variation in Silicon Nanoscale Technologies*, May 2006, Assistant Professor, Valparaiso University.

31. Jongsun Park, *Low Complexity Digital Signal Processing System Design Techniques*, September 2005, Marvel Semiconductors.

32. Hari Ananthanarayanan, *Technology and Circuit Design in Nanoscale Single- and Multiple-Gate Silicon CMOS*, September 2006, Qualcomm, San Diego.

33. Saibal Mukhopadhyay, *Design Methodologies for Memories in Scaled Technologies*, August 2006, Assistant Professor, ECE, Georgia Institute of Technology starting September 2007.

34. Animesh Datta, *Process-Tolerant CMOS Circuit and System Design*, January 2007, Qualcomm, San Diego.

35. Qikai Chen, *Low Power and Robust Memory Design: Device, Circuit, and Microarchitecture Perspective*, May 2007, Intel Corporation, Santa Clara.

36. Tamer Cakici, *Exploiting Independent Gate Technology in Multiple-Gate Silicon CMOS Circuit Design*, May 2007, Texas Instruments, Dallas.

37. Aditya Bansal, *Modeling and Optimization of Multiple-Gate FETs for Low-Power and Robust Circuit Design*, August 2007, IBM TJ Watson Research, Yorktown Heights, New York.

38. Arijit Raychowdhury, *Design of High Performance and Low Power Digital Circuits with Carbon Nanotube Based FETs*, September 2007, Circuits Research laboratory, Intel Corporation, Hillsboro, Oregon. **Choras Foundation Doctoral Dissertation Award**.

39. Kunhyuk Kang, *Analysis and Design of Nano-Scale VLSI Circuits Considering The Spatial and Temporal Reliability Degradation*, October 2007, Intel Corporation, Hillsboro, Oregon.

40. Myeong-Eun Hwang, *Ultralow Power and Process Variation Tolerant VLSI Circuit Design in Nanoscale Technologies*, December 2007, Intel Corporation, Hillsboro, Oregon.

41. Swaroop Ghosh, *Voltage-Scalable Adaptive System Design for Low Power and Error Resilience in Nanometer Technologies,* August 2008, Intel Corporation, Hillsboro, Oregon.

42. Nilanjan Banerjee, *Architecture-Circuit Co-Design for Low-Power and Error-Resilience in the Nanometer Regime*, August 2008, Intel Corp., Santa Clara, California.

43. Mesut Meterelliyoz, December 2008, Intel, Hillsboro, Oregon.

44. Jung-Hwan Choi, *Thermal Modeling, analysis, and Management Techniques for Nano Scale VLSI Circuits*, March 2009, Samsung Corporation, Seoul, Korea.

45. Jaydeep Kulkarni, *Low Voltage Robust Memory Circuit Design*, May 2009, Intel, Hillsboro, Oregon. **Doctoral Dissertation Award**.

46. Patrick Ndai, *Architecture-Aware Circuit Design for Process Tolerance and Resilience*, July 2009, Texas Instruments, Dallas, Texas.

47. Jing Li, *Robust and Energy-Efficient Heterogeneous System Design in Emerging Technologies*, July 2009, IBM TJ Watson Research, Yorktown, New York.

48. Ik-Joon Chang, *Aggressive Voltage Scaling in Digital Circuits*, October 2009, Samsung Corporation, Seoul, Korea.

49. Ashish Goel, *Low-Power, Process and Error Tolerant Circuit Design for Nanometer Technologies*, June 2010, Broadcom.

50. Georgios Karakonstantis, *Cross Layer Design Methodologies for Energy Efficient and Variation Tolerant Circuits and Systems*, December 2010, EPFL, Switzerland.

51. Debabrata Mohapatra, *Approximate Computing: Enabling Voltage Overscaling in Multi-media Applications*, April 2011, Intel Corporation, Santa Clara.

52. Niladri Mojumder, *Design of Hybrid Spintronic Devices at Scaled Technologies for Non-Volatile Memory Applications*, September 2011, Global Foundries.

53. Charles Augustine, *Spintronic Memory and Logic: From atoms to Systems*, October 2011, Intel Corporation, Hillsboro, Oregon.

54. Sang Phill Park, *On-Chip Memory Design in Scaled Technologies*, October 2011, Intel Corporation, Hillsboro, Oregon.

55. George Panagopoulos, *On Variability and Reliability of CMOS and SPIN based Devices*, August 2012, Intel Corporation, Munich, Germany.

Ph.D. Theses Currently Supervising:

56. Sumeet Gupta

57. Mrigank Sharad

58. Yusung Kim

59. Xunyao Fong

60. Myeong Aye Kang

61. Himanshu Markendeya

62. Lu Chao

63. Dongsoo Lee

64. Soo Youn Kim

65. Selin Baytok

66. Paul Griffin

67. Vaibhav Gupta

68. Harsha Choday

69. Chih-Hsiang Ho

70. Mayur Bubna

71. Kon-Woo Kwon

72. Karthik Yogendra

73. Wuh-Sul Choo

74. Arun Goud

MS Theses Supervised:

75. Priya Patil, *Low Power Driven Logic Synthesis*, Feb. 1996. Currently at Intel Corp., California.

76. Hendrawan Soeleman, *Power Estimation of Static CMOS Combinational Digital Logic Circuits*, Aug. 1996.

77. M. Lundberg, "Fast Power Estimation Methods with Application to Adaptive Channel Equalization," Lulea University of Technology, Lulea, Sweden. *Ericsson MD110 User Group Award for the Best MS thesis in Telecommunications area in Sweden.*

78. N. Sankarayya, *Computational Optimizations for Low-Power Digital Signal Processing*, Dec. 1997.

79. Naran Sirisantana, *High-Performance Low-Power CMOS Circuits Using Multiple Channel Length and Multiple Oxide Thickness*, Jan. 2000.

80. Jong-Sun Park, *High-Performance FIR Filter Implementation Based on Sharing Multiplication*, June 2000.

81. Cassondra Crotty, *Low Complexity Finite Impulse Response Digital Filter Design Using Factorization of Perturbed Coefficients*, June 2000.

82. Hunsoo Choo, *Decision Feedback Equalizer with Computation Sharing Multiplication Using Redundant Number Scheme*, December 2000.

83. Amit Agarwal, *Design of Leakage Tolerant Caches for Scaled Technologies,*, January 2002.

84. Hiroaki Suzuki, *Adaptive Supply Voltage for Low-Power Ripple-Carry and Carry-Select Adders*, December 2003.

85. Debjyoti Ghosh, *Low-Complexity Power-Efficient BIST*, December 2003, Analog Devices.

86. Aditya Bansal, *Optimization and Characterization of Sub-50nm Gate Length Asymmetric Halo MOSFETs*, December 2003.

87. Cheng-Yi Chen, *Efficient Communication Channel Utilization for Mapping FFT onto Mesh Array and Torus Array*, May 2004, Socle Technology Corp, TW.

88. Rouzbeh Jazayeri, *An Efficient Low Power and High Performance Multiplier for Digital Filtering*, May 2004, Intel.

89. Mathew Cooke, *Energy-Recovery Clocking Scheme and Circuit Elements*, December 2004, AMD.

90. James Gallagher, *Low Power Design using Dual-Vt for Nanometer-Scale CMOS*, May 2005, Intel.

91. Arjun Guha, *Design of Robust SRAM Cells*, May 2006, Micron.

92. Pooja Batra, *Logic Families for Ultralow-Power Process Tolerant Digital Subthreshold Design*, February 2007, Sun Microsystems.

93. Saakshi Gangwal, *Optimization of Surface Orientation for Robust, High-Performance and Low-Power FinFET SRAM*, May 2007, Intel Corporation, Austin.

94. Dheepa Lekshmanan, *Device Circuit Co-design for Robust and High Performance FinFET Logic and SRAMs*, May 2007, Texas Instruments, Dallas.

95. Vinita Soman, *Cell Based Library Design Methodology for Improved performance and Variation Tolerance in Subthreshold Circuits*, Intel Corp., Hillsboro, Oregon.

96. Sumeet Gupta, *Modeling and Analysis of Digital Computation in Ultra-Subthreshold Regime: Approaching CMOS Limits*, currently enrolled in the PhD program in my group.

97. Niladri Mojumder, *Self-Repairing SRAM using On-Chip Detection and Compensation*, enrolled in PhD program in my group.

98. Christine Placek, *Voltage Over-Scaling in Unbalanced Pipelines with Adaptive Clocking*, Intel Corporation, Hillsboro, Oregon.

MS Theses Currently Being Supervised:

Visiting Scholar and Post-doctoral Researcher:

99. Magnus Lundberg, Sweden.
100. Alexandro Adario, PhD student from Brazil.
101. Mikael Kerttu, Lulea University, Sweden.
102. Dr. Bipul Paul, Post-doctoral researcher, PhD from Indian Institute of Science, India.
103. Dr. Keejong Kim, Post-doctoral researcher from Samsung, currently in Broadcom.
104. Prof. Meng-Huseh Chiang, National Ilan University, Taiwan
105. Prof. Il-Sup Chung, Korea

ACTIVITIES AS A REFEREE:

1992 - present	National Science Foundation
1988 - present	IEEE Transactions on Computer-Aided-Design, IEEE Transactions on Circuits and Systems, IEEE Transactions on VLSI Systems, IEEE Transactions on Electron Devices, IEEE/ACM Design Automation Conference, International Test Conference, International Conference on Computer-Aided-Design, IEEE VLSI Test Symposium, etc.

LIST OF PUBLICATIONS

BOOKS

1. K. Roy and S. Prasad, *Low-Power CMOS VLSI Circuit Design*, John Wiley & Sons, Inc., ISBN 0-471-11488-X, 2000, 359 pages.

2. K-S. Yeo and K. Roy, *Low-Voltage Low-Power VLSI Subsystems,* McGraw-Hill 2004, ISBN: 0-07-143786-X, 294 pages.

CHAPTERS IN BOOKS

3. K. Roy, "Segmented Channel Routing," book chapter in *Advanced Routing of Electronic Modules*, ed. M. Pecht, CRC Press, 1995, pp. 207-235.

4. M. Levitt and K. Roy, "Testing of BiCMOS Logic," book chapter in *BiCMOS Technology and Applications*, Kluwer Academic Publishers, ed. A. Alvarez, 1993, pp. 271-294.

5. K. Roy and S. Prasad, "Power Dissipation Driven FPGA Place and Route under Delay Constraints," in *Field Programmable Logic – Architectures, Synthesis, and Applications*, Springer-Verlag, 1994, pp. 57-65.

6. K. Roy and S. Nag, "On Channel Architecture and Routability for FPGA's under Faulty Conditions," in *Field Programmable Logic – Architectures, Synthesis, and Applications*, Springer-Verlag, 1994, pp. 361-372.

7. K. Roy, R. Roy, and T.-L. Chou, "Design of Low Power Digital Systems," in *Emerging Technologies*, ed. W. Liu and R. Cavin, IEEE, May 1996, pp. 137-204.

8. K. Roy, "Power Analysis and Design at System Level: Notebook Computers," in , Kluwer Academic Press, *Low Power Design in Deep Submicron Electronics*, October 1996, ed. J. Mermet and W. Nebel, pp. 419-431.

9. K. Roy and M. Johnson, "Software Power Optimization," in *Low Power Design in Deep Submicron Electronics*, Kluwer Academic Press, October 1996, ed. J. Mermet and W. Nebel, pp. 433-459.

10. T.-L. Chou and K. Roy, "Logic Synthesis," in *Encyclopedia of Electronics*, John Wiley & Sons, March 1999, ISBN 0471139467.

11. H. Soeleman and K. Roy, "Accurate Power Estimation of Combinational Digital Circuits," in *The Computer Engineering Handbook*, edited by V. Oklobdzija, CRC Press, 2002, ISBN: 0-8493-0885-2.

12. A. Agarwal and K. Roy, "Exploring High Bandwidth Pipelined Cache Architecture for Scaled Technology," in Embedded Software for SoC, Edited by A. A. Jerraya, S. Yoo, N. Wehn, D. Verkest (editors), Kluwer Academic Publishers, June 2003.

13. A. Agarwal, C. H. Kim, and K. Roy, "Circuit Techniques for Leakage Reduction," in *Low Power Electronics Design*, Edited by C. Piguet, CRC press, 2004, pp. 13.1-13.15, ISBN: 0-8493-1941-2.

14. A. Raychowdhury and K. Roy, "Nanometer Scale Technologies: Device Considerations," in *Nano, Quantum, and Molecular Computing: Implications to High Level Design and Validation,* Kluwer Academic Press, pp. 5-29, June 2004, ISBN: 1-4020-8067-0.

15. A. Keshavarzi and K. Roy, "Impact of Leakage Power and Variation on Testing," in *Leakage in Nanometer CMOS Technologies*, Springer, 2006, ISBN: 0-387-25737-3.

16. K. Roy and S. Bhunia, " Low Power Design Techniques and Test and Test Implications," Chapter in *Power Aware Testing and Test Strategies for Low Power Devices*, Springer, ISBN: 978-1-4419-0927-5.

17. J. Kulkarni and K. Roy, "Tecnology/Circuit Co-Design for III-V FETs," Chapter in *Fundamentals of III-V Semiconductor MOSFETs*, Springer, ISBN: 978-1-4419-1546-7, pp. 423-441.

18. G. Karakonstantis and K. Roy, "Low-Power and Variation-Tolerant Application-Specific System Design," Chapter in *Low-Power Variation-Tolerant Design in Nanometer Silicon*, Springer, ISBN: 978-1-4419-7417-4, pp. 249-292.

ARTICLES IN JOURNALS

19. P. Banerjee, J. Rahmeh, C. Stunkel, S. Nair, K. Roy, V. Balasubramanian, and J. Abraham, "Algorithm Based Fault Tolerance on Hypercube," *IEEE Transactions on Computers*, August, 1990, pp. 1132-1145.

20. K. Roy and J. Abraham, "The Use of RTL Descriptions in Accurate Timing Verification and Test Generation," *IEEE Journal of Solid State Circuits*, September, 1991, pp. 1230-1239.

21. K. Roy, "A Bounded Search Algorithm for Segmented Channel Routing for FPGAs and Associated Channel Architecture Issues," *IEEE Transactions on Computer-Aided-Design of Integrated Circuits*, November, 1993, pp. 1695-1705.

22. K. Roy and S. Prasad, "Circuit Activity Based Logic Synthesis for for Low Power Reliable Operations," *IEEE Transactions on VLSI Systems*, December, 1993, pp. 503-513.

23. M. Levitt, K. Roy, and J. Abraham, "BiCMOS Logic Testing," *IEEE Transactions on VLSI Systems*, June 1994, pp. 241-248.

24. K. Roy and S. Nag, "Automatic Synthesis of FPGA Channel Architecture for Performance and Routability," *IEEE Transactions on VLSI Systems*, December 1994, pp. 508-511.

25. K. Roy and S. Prasad, "Logic Synthesis for Reliability – An Early Start to Controlling Electromigration and Hot Carrier Effects," *IEEE Transactions on Reliability*, June, 1995, pp. 251-255.

26. K. Roy and S. Nag, "On Routability for FPGA's under Faulty Conditions," *IEEE Transactions on Computers*, November 1995, pp. 1296-1305.

27. K. Kornegay and K. Roy, "Structured Test Methodology and Test Economics for Multichip Modules," *IEEE Transactions on Components, Hybrids, Manufacturing Technology – Advanced Packaging*, February 1996, pp. 195-202.

28. S. Prasad and K. Roy, "Transistor Reordering for Power Minimization under Delay Constraint," *ACM Transactions on Design Automation of Electronic Systems*, Vol. 1, No. 2, April 1996, pp. 280-300.

29. D. Somasekhar and K. Roy, "Differential Current Switch Logic: A Low-Power DCVS Logic Family," *IEEE Journal of Solid-State Circuits*, July 1996, pp. 981-991.

30. T.-L. Chou and K. Roy, "Accurate Power Estimation of CMOS Sequential Circuits," *IEEE Transactions on VLSI Systems*, September 1996, pp. 369-380.

31. Y. Ye and K. Roy, "Energy Recovery Circuits Using Reversible and Partially Reversible Logic," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, September 1996, pp. 769-778.

32. T.-L. Chou and K. Roy, "Estimation of Activity for Static and Domino CMOS Circuits Considering Signal Correlations and Simultaneous Switching," *IEEE Transactions on Computer-Aided Design of Integrated Circuits*, October 1996, pp. 1257-1265.

33. N. Sankarayya, K. Roy, and D. Bhattacharya, "Algorithms for Low Power High Speed FIR Filter Realization Using Differential Coefficients," *IEEE Transactions on Circuits and Systems: Analog and Digital Signal Processing*, June 1997, pp. 488-497.

34. M. Johnson and K. Roy, "Datapath Scheduling with Multiple Supply Voltages and Voltage Converters," *ACM Transactions on Design Automation of Electronic Systems*, July 1997.

35. T.-L. Chou and K. Roy, "Statistical Estimation of CMOS Circuit Activity under Probabilistic Delays," *IEICE (Japan) Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, special issue on VLSI Design and CAD Algorithms, October 1997, pp. 1915-1923.

36. Y. Ye and K. Roy, "An XOR-Based Decomposition Diagram and Its Application in Synthesis of AND-XOR Network," *IEICE (Japan) Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, special issue on VLSI Design and CAD Algorithms, October 1997, pp. 1742-1748.

37. S. Nag and K. Roy, "Performance and Wireability Driven Layout for Row-Based FPGAs," *Journal of VLSI Design*, Vol. 7, No. 4, 1998, pp. 353-364.

38. K. Roy, "Power Dissipation Driven FPGA Place and Route Under Timing Constraints," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, May 1999, Vol. 46, No. 4, pp. 634-637.

39. T.-L. Chou and K. Roy, "Power Estimation Under Uncertain Delays," *Integrated Computer-Aided Engineering*, Wiley-Intersciece, pp. 107-116, vol. 5, no. 2, 1998.

40. C.-Y. Wang and K. Roy, "Maximum Power Estimation for CMOS Circuits Using Deterministic and Statistical Techniques," *IEEE Transactions on VLSI Systems*, March 1998, pp. 134-140.

41. Z. Chen, K. Roy, and T.-L. Chou, "Efficient Statistical Approach to Estimate Power Considering Uncertain Properties of Primary Inputs," *IEEE Transactions on VLSI Systems*, pp. 484-492, September 1998.

42. D. Somasekhar and K. Roy, "LVDCSL: A High-Performance Low-Power Logic Using High Fan-in Gates," *IEEE Transactions on VLSI Systems*, Special issue on low-power design, December 1998, pp. 573-577.

43. L. Wei, Z. Chen, K. Roy, M. Johnson, Y. Ye, and V. De, "Design and Optimization of Dual Threshold Circuits for Low-Voltage Low-Power Applications," *IEEE Transactions on VLSI Systems*, Special issue on low-power electronics and design, March 1999, pp. 16-24.

44. C. Wang and K. Roy, "An Activity-Driven Encoding Scheme for Power Optimization in Microprogrammed Control Unit," *IEEE Transactions on VLSI Systems*, March 1999, pp. 130-134.

45. M. Johnson, D. Somasekhar, and K. Roy, "Models and Algorithms for Bounds on Leakage in CMOS Circuits," *IEEE Transactions on Computer-Aided Design of IC's*, June 1999, pp. 714-725.

46. H. Soeleman, K. Roy, and T.-L. Chou, "Estimating Circuit Activity in Combinational CMOS Digital Circuits," *IEEE Design and Test of Computers*, April-June 2000, pp. 112-119.

47. C-Y. Wang and K. Roy, "Maximization of Power Dissipation in Large CMOS Circuits Considering Spurious Transitions," *IEEE Transactions on Circuits and Systems - I*, April 2000, pp. 483-490.

48. Z. Chen, K. Roy, and E. Chong,"Estimation of Power Dissipation Using a Novel Power Macromodeling Technique," *IEEE Transactions on Computer-Aided-Design*, November 2000, pp. 1363-1369.

49. X. Zhang, K. Roy, and S. Bhawmik, 'Low Power Weighted Random Pattern Testing," *IEEE Transactions on Computer-Aided-Design*, November 2000, pp. 1389-1398.

50. K. Muhammad and K. Roy, "Fault Detection and Location Using IDD Waveform Analysis," *IEEE Design and Test*, January-February 2001, pp. 42-49.

51. A. Keshavarzi, K. Roy, and C. Hawkins, "Intrinsic Leakage in Deep Submicron IC's – Measurement Based Test and Power Solutions," *IEEE Transactions on VLSI Systems*, December 2000, pp. 717-723.

52. Y. Ye and K. Roy, "QSERL: Quasi-Static Energy Recovery Logic," *IEEE Journal of Solid-State Circuits*, February, 2001 pp. 239-249.

53. L.-Y. Chiou, K. Muhammad, and K. Roy, "Signal Strength based Switching Activity Modeling and Estimation for DSP Applications," *Journal of VLSI Design*, Special issue on low power design, Vol. 12, No. 2, pp.233-243, 2001

54. S.-H. Yang, M. Powell, B. Falsafi, K. Roy, and T. Vijaykumar, "An Energy-Efficient High Performance Deep-Submicron Instruction Cache," *IEEE Transactions on VLSI Systems*, Special issue on low-power design, February 2001, pp. 77-89.

55. H. Soeleman, K. Roy, and B. Paul, "Robust Sub-Threshold Logic for Ultra-Low Power Operation," *IEEE Transactions on VLSI Systems*, Special issue on low-power design, February 2001, pp. 90-99.

56. R. Zhang, K. Roy, C.-K. Koh, and D. Janes, "Stochastic Interconnect Modeling, Power Trends, and Performance Characterization of 3-Dimensional Circuits," *IEEE Transactions on Electron Devices*, April 2001, pp. 638-652.

57. Z. Chen, L. Wei, and K. Roy, "On Effective IDDQ Testing of Low Voltage CMOS Circuits Using Leakage Control Techniques," *IEEE Transactions on VLSI Systems*, October 2001, pp. 718-725.

58. M. Lundberg, K. Muhammad, K. Roy, and S. Wilson, "A Novel Approach to High Level Switching Activity Modeling with Applications to DSP System Synthesis," *IEEE Transactions on Signal Processing*, December 2001.

59. S. Zhao, C.-K. Koh, and K. Roy, "Decoupling Capacitance Allocation and Its Application to Power Supply Noise Aware Floorplanning," *IEEE Transactions on Computer-Aided Design of IC's*, January 2002, pp. 81-92.

60. K. Muhammad and K. Roy, "A Graph Theoretic Approach for Synthesizing Very Low-Complexity High-Speed Digital Filters," *IEEE Transactions on Computer-Aided Design of IC's*, February 2002, pp. 204-216.

61. M. Johnson, D. Somasekhar, L. Chiou, and K. Roy, "Leakage Control With Efficient Use of Transistor Stacks in Single Threshold CMOS," *IEEE Transactions on VLSI Systems*, February 2002, pp. 1-5.

62. Z. Chen, L. Wei, A. Keshavarzi, and K. Roy, "IDDQ Testing for Deep Sub-Micron IC's: Challenges & Solutions," *IEEE Design & Test*, March-April 2002, pp. 24-33.

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