

Enhancement of Thermal Transfer From β -Ga₂O₃ Nano-Membrane Field-Effect Transistors to High Thermal Conductivity Substrate by Inserting an Interlayer

Jinhyun Noh^{ID}, Prabudhya Roy Chowdhury, Mauricio Segovia, Sami Alajlouni^{ID}, Mengwei Si^{ID}, Adam R. Charnas^{ID}, Shouyuan Huang, Kerry Maize, Ali Shakouri, Xianfan Xu, Xiulin Ruan, and Peide D. Ye^{ID}, *Fellow, IEEE*

Abstract—The role of a HfO₂ or ZrO₂ interlayer as a thermal bridge between a β -Ga₂O₃ channel and a sapphire substrate was investigated using a β -Ga₂O₃ nano-membrane FET as a test vehicle. A 35% less channel temperature increase was observed when a thin HfO₂ or ZrO₂ interlayer was inserted between the β -Ga₂O₃ channel and the sapphire substrate compared to devices without interlayers. Phonon density of states (PDOS) mismatch can explain the improvement of the thermal boundary conductance (TBC). In the acoustic region, the PDOS of HfO₂ or ZrO₂ has about a 700% larger overlap area with the PDOS of β -Ga₂O₃ compared to the PDOS of sapphire. This suggests that the insertion of a thermal bridge interlayer can provide a potential solution to the low thermal conductivity of β -Ga₂O₃ and the self-heating effect of β -Ga₂O₃-based FETs.

Index Terms—Nano-membrane, phonon density of state, self-heating effect, thermal boundary conductance (TBC), thermal bridge, thermal conductivity, β -Ga₂O₃ FET.

I. INTRODUCTION

WIDE bandgap semiconductor materials have been intensively investigated and developed for RF power and power switch applications. Beyond widely studied materials such as SiC and GaN, the newly emerging and promising material β -Ga₂O₃ has attracted attention due to its ultra-wide bandgap of 4.8 eV, high electron mobility of 300 cm²/V · s, high Baliga's figure-of-merit (FOM) than that of SiC and GaN, and substrate mass production potential by low-cost melt growth methods [1]–[13]. However, all β -Ga₂O₃ power

devices have serious self-heating effects (SHE) due to their low thermal conductivity (κ) of 10–25 W/m · K [14]. SHE significantly limits the maximum drain current (I_D), the output power density (P), and the long-term reliability [14]–[21].

In our previous works, integration of a low- κ β -Ga₂O₃ nano-membrane on a high- κ substrate was done to address the channel thermal issue [22]. By using higher κ substrates such as diamond, the lowest peak temperature and the highest I_D were obtained [23], [24]. However, additional studies are needed to address the critical issue of the thermal interface between β -Ga₂O₃ and substrates. Moreover, the exfoliation and transfer method also makes the bonding between β -Ga₂O₃ nano-membranes and substrates weaker than direct growth by epitaxy. This means that thermal boundary conductance (TBC) can be more serious in β -Ga₂O₃ nano-membrane FETs for the improvement of heat transfer and elimination of SHE.

TBC between β -Ga₂O₃ and high thermal conductivity substrates is a concern in β -Ga₂O₃ nano-membrane FETs or β -Ga₂O₃ epitaxial FETs [25]–[28]. Using a sapphire substrate for the β -Ga₂O₃ channel, an intermediate layer is proposed to help bridge phonon mismatch which might improve the total TBC between β -Ga₂O₃ and sapphire [29], [30]. In this work, we have fabricated β -Ga₂O₃ nano-membrane FETs on a sapphire substrate with an interlayer between the β -Ga₂O₃ and the substrate. A sapphire substrate was used to see the effect of interlayers because sapphire has a moderate level of thermal conductivity, and is more common and cost-effective compared to diamond although sapphire has lower thermal conductivity than diamond. A thin (~5 nm) interlayer of hafnium oxide (HfO₂) or zirconium oxide (ZrO₂) was selected to act as a bridge between the phonon spectra mismatch of β -Ga₂O₃ and sapphire. A 35% reduction of temperature increase (ΔT) at the same power condition is achieved after inserting the HfO₂ or ZrO₂ interlayer. The bridging effect of HfO₂ or ZrO₂ between β -Ga₂O₃ and sapphire is understood by their phonon density of states (PDOS) spectra.

II. DEVICE FABRICATION AND MEASUREMENT

The device fabrication steps are identical to those in previous publications [22]–[24] with the exception of an additional atomic layer deposition (ALD) step. Right before the exfoliation and transfer of β -Ga₂O₃, a 5-nm interlayer of HfO₂ or ZrO₂ was deposited on sapphire substrates by ALD at 200°C using TDMAHf ((CH₃)₂N)₄Hf), TDMAZr ((CH₃)₂N)₄Zr, and H₂O as the Hf, Zr, and O precursors,

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Jinhyun Noh, Sami Alajlouni, Mengwei Si, Adam R. Charnas, Kerry Maize, Ali Shakouri, and Peide D. Ye are with Birk Nanotechnology Center, the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA (e-mail: yep@purdue.edu).

Prabudhya Roy Chowdhury, Mauricio Segovia, Shouyuan Huang, Xianfan Xu, and Xiulin Ruan are with the School of Mechanical Engineering, Purdue University, West Lafayette, IN 47907 USA.

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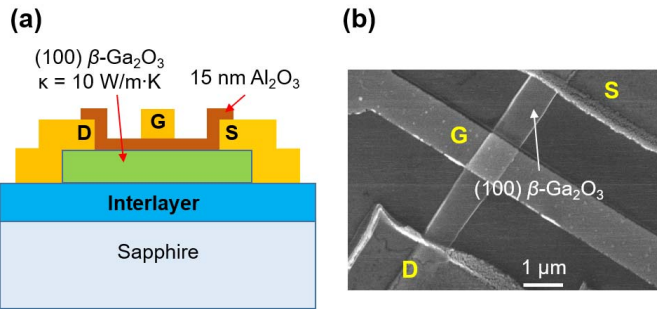


Fig. 1. (a) Cross-sectional schematic view of a fabricated β -Ga₂O₃ nano-membrane FET. (b) SEM image of a β -Ga₂O₃ nano-membrane FET with a 5-nm HfO₂ interlayer.

respectively. Consequently, β -Ga₂O₃ nano-membrane FETs were fabricated and studied on three types of substrates that are 5-nm HfO₂ on sapphire, 5-nm ZrO₂ on sapphire, and directly on sapphire for comparison. Around 150-nm-thick β -Ga₂O₃ flakes were selected for the device fabrication. After membrane transfer, source and drain regions were patterned by electron-beam lithography (EBL) using a JEOL JBX-8100FS. ZEP 520A was used as the electron-beam resist. Before metallization, an Ar plasma bombardment with radio frequency power of 100 W was applied to improve the contact resistance by generating oxygen vacancies to enhance the n-type surface of β -Ga₂O₃ flakes. A Ti/Al/Au (15/60/50 nm) metal stack was deposited using an electron-beam evaporation and lift-off process. A 15-nm Al₂O₃ was deposited by ALD at 250 ° as the gate dielectric using TMA [(CH₃)₃Al] and H₂O as the Al and O precursors, respectively. Finally, Ni/Au (50/50 nm) gate metal was formed using EBL, electron-beam evaporation, and lift-off process; the same as the source and drain formation. After the whole fabrication, the devices were annealed at 400° in nitrogen ambient for 30 min to improve the source and drain contact resistance. Fig. 1(a) shows a cross-sectional schematic view of a fabricated β -Ga₂O₃ nano-membrane FET with an interlayer. Fig. 1(b) shows an SEM image of a β -Ga₂O₃ nano-membrane FET with a 5-nm HfO₂ interlayer.

Sample direct current (dc) current–voltage (I – V) characteristics of the three device types are shown in Fig. 2. The β -Ga₂O₃ nano-membrane FETs on sapphire, HfO₂/sapphire, and ZrO₂/sapphire substrates with similar dimensions of gate length (L_g) = 1 μ m, gate to source distance (L_{SD}) = \sim 3.5 μ m, and thickness = \sim 150 nm were measured for a fair comparison of electrical properties. The threshold voltage (V_T) of the three selected devices is \sim -25 V as shown in Fig. 2(a). The maximum drain current ($I_{D,max}$) at drain to source voltage (V_{DS}) of 10 V, and gate to source voltage (V_{GS}) of 0 V of three devices are also \sim 300 mA/mm as shown in Fig. 2(b). The output and transfer characteristics of representative β -Ga₂O₃ nano-membrane FETs on substrates with different interlayers are similar. This indicates that electrical property behaviors of β -Ga₂O₃ nano-membrane FETs are not affected by the thin interlayer between β -Ga₂O₃ and a sapphire substrate significantly.

The gate electrode temperatures at various dc bias conditions were measured using steady-state thermo-reflectance (TR) imaging experiments. The gate Au pads were illuminated as a representative of the channel temperature through a green LED (λ = 530 nm) with Au TR coefficient (C_{TH} = -2.5×10^{-4} K⁻¹) known [31]. For a fair comparison, the temperature of various β -Ga₂O₃ nano-membrane FETs with similar dimensions of gate width (W) = 1 μ m, L_{SD} =

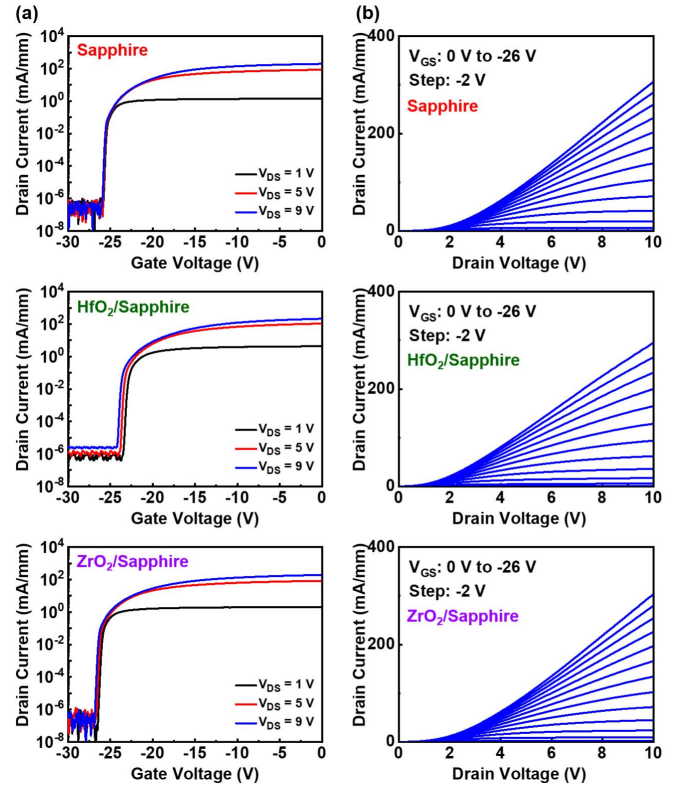


Fig. 2. (a) I_D – V_{GS} and (b) I_D – V_{DS} characteristic curves of the three fabricated β -Ga₂O₃ nano-membrane FETs on a sapphire, a 5-nm HfO₂/sapphire, and a 5-nm ZrO₂/sapphire substrate. L_g = 1 μ m, L_{SD} = \sim 3.5 μ m, thickness \sim 150 nm.

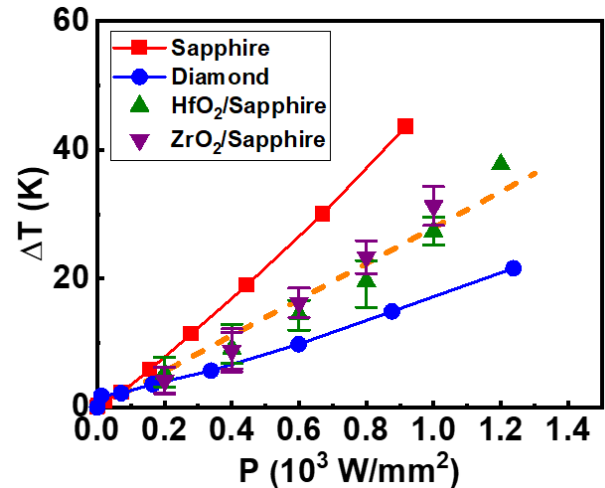


Fig. 3. Comparison of the TR measured ΔT versus P (W/mm²) characteristics of β -Ga₂O₃ nano-membrane FETs on a sapphire, a diamond, 5-nm HfO₂/sapphire, and 5-nm ZrO₂/sapphire substrate.

\sim 6.5 μ m on a 5-nm HfO₂/sapphire, a 5-nm ZrO₂/sapphire substrate, and direct sapphire and diamond substrates were measured. Fig. 3 shows the measured ΔT versus biased power dissipation (P) normalized by the active device area (W/mm²). With the interlayer inserted, β -Ga₂O₃ nano-membrane FETs on a 5-nm HfO₂/sapphire or a 5-nm ZrO₂/sapphire substrate have 35% lower ΔT at the same P condition, compared to that of only sapphire. Although the improvement is not as great as diamond, the reduction of temperature increase is clearly seen in Fig. 3. This demonstrates that an ultrathin HfO₂ or ZrO₂ interlayer helps heat transfer from β -Ga₂O₃ to a sapphire substrate by acting as a thermal bridge.

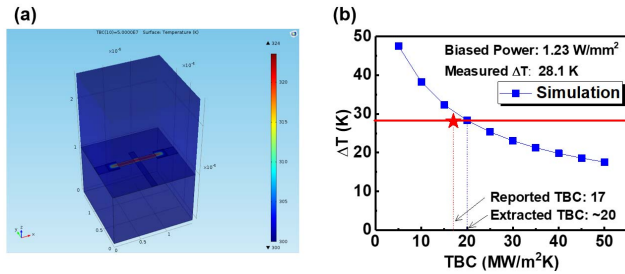


Fig. 4. (a) Simulated temperature distribution of a TR measured β -Ga₂O₃ FET on a diamond substrate. (b) Extraction of the TBC value between β -Ga₂O₃ and diamond from TBC versus ΔT graph.

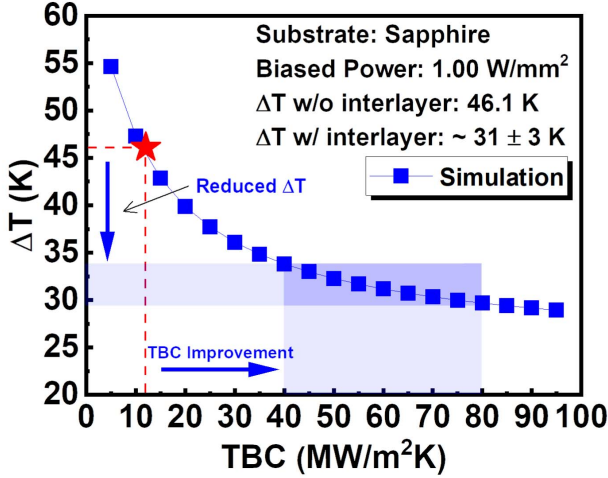


Fig. 5. Comparison of the TR measured ΔT versus P (W/mm²) characteristics of β -Ga₂O₃ nano-membrane FETs on a sapphire, a diamond, 5-nm HfO₂/sapphire, and 5-nm ZrO₂/sapphire substrate.

In order to obtain the quantitative TBC between the β -Ga₂O₃ and the substrate via experimental measurements, a simple steady-state method was applied. The heat transfer of 1-D thermal diffusion is described by

$$\rho C_p \frac{\partial T}{\partial t} = \frac{\partial}{\partial x} \left(\kappa \frac{\partial T}{\partial x} \right) + P \quad (1)$$

where ρ is the density of the material, C_p is specific heat per mass, κ is the thermal conductivity, and P is the heat generation source [32]. The first transient heat transfer term can be neglected in the steady-state simulations. Using (1), the TBC between the β -Ga₂O₃ and the diamond substrate is obtained by fixing all other known parameters such as κ of materials, biased power dissipation, and measured temperature [24]. Using COMSOL simulation in Fig. 4(a), the extracted TBC from TR measurement was about 20 MW/m² · K, which is well matched with a recently reported value as shown in Fig. 4(b) [33]. This verifies the methodology is valid to estimate the TBC of other novel thermal interfaces. In the same way, the TBC between β -Ga₂O₃ and a sapphire substrate of ~12 MW/m² · K can be obtained as shown in Fig. 5. By the insertion of a HfO₂ or ZrO₂ interlayer, the TBC of the whole β -Ga₂O₃/HfO₂ or ZrO₂/sapphire interface is improved to ~60 ± 20 MW/m² · K, five times better than with direct contact.

III. DISCUSSION

In order to analyze, the TBC of the interface between HfO₂ or ZrO₂ and sapphire was measured using the well-established time-domain thermoreflectance (TDTR) technique for thermal

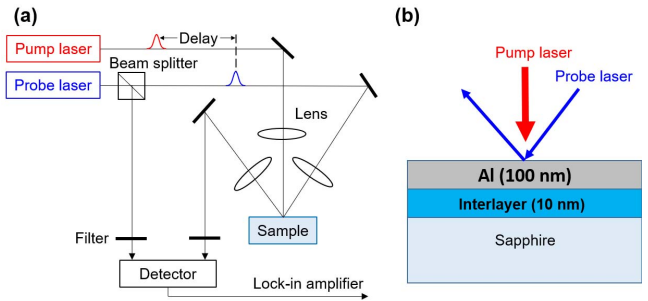


Fig. 6. (a) Schematic of the TDTR measurement system. (b) Schematic of the TDTR measurement of the sample stack consisting of an Al transducer, interlayers, and a sapphire substrate.

measurement of bulk or nanostructured materials [34]–[43]. Fig. 6(a) shows the schematic of the TDTR measurement setup. An ultrafast laser with a center wavelength of 800 nm, 100-fs duration pulse laser, and ~80-MHz repetition rate was used. The series of laser pulses is split using a beam splitter to a pump and a probe beam. The pump beam was modulated at 864 kHz, 2 MHz, and 5 MHz for more accurate measurements. The modulated and delayed pump beam and the non-modulated and non-delayed probe beam are brought in focus to the surface of the sample. The radii of pump and probe beams are 8 ± 2 μ m. Only for the TDTR measurement, samples with 100 nm Al/10 nm HfO₂ or ZrO₂/sapphire were fabricated as shown in Fig. 6(b). The top Al layer is an optical absorption layer and thermal reflectance transducer. The reflected probe light is filtered using the different polarization orientation with the pump beam and detected by a photodetector and a locked-in amplifier at the pump modulation frequency. Finally, the TBC can be extracted by fitting to 2-D transient heat diffusion model using the in-phase and out-of-phase signals which indicate the temporal change at the transducer surface [44], [45].

The TBC between HfO₂/sapphire and ZrO₂/sapphire are extracted as 277 ± 50 MW/m² · K and 394 ± 20 MW/m² · K, respectively. The error range is quite large due to the thinness of the interlayers. In consideration of absorption depth, thin interlayers of 10 nm were used for the TDTR measurement samples. However, κ becomes very dependent on film thickness when it is on the order of the mean free path of the energy carriers [46]–[49]. Because of the thickness of the interlayer and its small κ , the effective TBC of the film, defined as its thermal conductivity divided by its thickness, is of the same order of magnitude as the reported TBCs, i.e., ~100 MW/m² · K. This leads to large uncertainty. Regardless of the error range, the TBC levels of the interfaces between an interlayer HfO₂ or ZrO₂ and sapphire are confirmed to be one order larger than the TBC of the whole β -Ga₂O₃/HfO₂ or ZrO₂/sapphire interface. This leads to the conclusion that the β -Ga₂O₃/HfO₂ or ZrO₂ interface is the bottleneck for heat transfer. As mentioned, the TBC of the whole β -Ga₂O₃/HfO₂ or ZrO₂/sapphire interface is improved from ~13 to ~55 MW/m² · K by insertion of a HfO₂ or ZrO₂ interlayer. The bottom interface of HfO₂ or ZrO₂/sapphire has one order higher TBC value than the whole β -Ga₂O₃/HfO₂ or ZrO₂/sapphire interface, so that the bottom interface could be negligible in the whole interface TBC calculation. In conclusion, the improvement of TBC from ~13 to ~55 MW/m² · K could be considered to be caused by the improvement of the top β -Ga₂O₃/HfO₂ or ZrO₂ interface compared to the direct β -Ga₂O₃/sapphire interface.

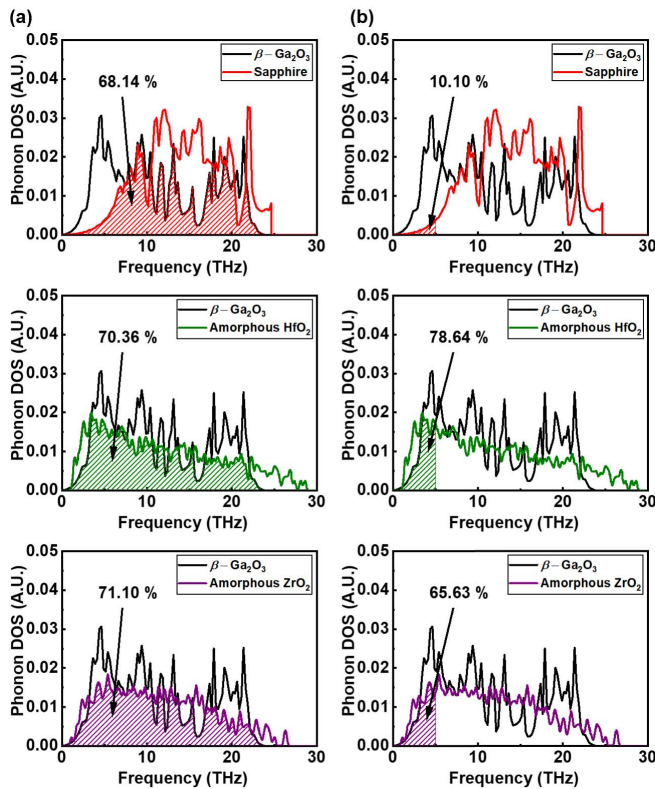


Fig. 7. (a) PDOS overlap of β -Ga₂O₃ with sapphire, β -Ga₂O₃ with HfO₂, and β -Ga₂O₃ with ZrO₂. (b) PDOS overlap of β -Ga₂O₃ with sapphire, β -Ga₂O₃ with HfO₂, and β -Ga₂O₃ with ZrO₂ in the low frequency acoustic phonon region ($< \sim 5$ THz for β -Ga₂O₃).

In order to explain the improvement of the TBC, the PDOS mismatch between β -Ga₂O₃ and sapphire, HfO₂, and ZrO₂ were compared. Depending on the mismatch of PDOS between two materials, TBC can be high or low regardless of κ [50]. The PDOS of crystalline β -Ga₂O₃ and sapphire were calculated using density functional theory (DFT) calculations performed using the Vienna *Ab initio* Simulation Package (VASP) [51]. Electron wavefunctions were solved using the projector augmented wave function (PAW) method with a plane wave basis set cutoff of 520 eV. The Perdew-Burke-Ernzerhof (PBE) parameterization of the generalized gradient approximation (GGA) was used to calculate the electron exchange and correlation. For structural optimization of a single unit cell, an $8 \times 8 \times 8$ Monkhorst-Pack k -point mesh was used. The second-order force constants and the PDOS were calculated by the finite-differences method using the open-source code Phonopy [52] for a $3 \times 3 \times 3$ supercell. Fig. 7(a) shows the PDOS overlap of β -Ga₂O₃ with sapphire, β -Ga₂O₃ with HfO₂, and β -Ga₂O₃ with ZrO₂. The PDOS of β -Ga₂O₃ was obtained from first-principles DFT calculation, with the PDOS of amorphous HfO₂ and ZrO₂ as reported in the literature [53]. The overlap area in a frequency range of 0–30 THz is similar to each other. However, there is a significant phonon mismatch in the acoustic region corresponding to the low frequency acoustic phonon modes ($< \sim 5$ THz for β -Ga₂O₃) as shown in Fig. 7(b). Lower frequency phonons also known as acoustic phonons are responsible for most of the heat transport [32]. The PDOS of HfO₂ or ZrO₂ has about seven times larger overlap area with the PDOS of β -Ga₂O₃ in the acoustic region compared to the PDOS of sapphire. The smaller TBC is expected at the β -Ga₂O₃/sapphire interface

considering its larger phonon mismatch in the acoustic region. This explains the improvement of the TBC when a HfO₂ or ZrO₂ interlayer is inserted as a thermal bridge between β -Ga₂O₃ and a sapphire substrate.

IV. CONCLUSION

In this work, the role of a HfO₂ or ZrO₂ interlayer as a thermal bridge between β -Ga₂O₃ and a sapphire substrate in β -Ga₂O₃ nano-membrane FETs was demonstrated. A 35% less channel temperature increase was observed when a HfO₂ or ZrO₂ interlayer was inserted between β -Ga₂O₃ and a sapphire substrate compared to without an interlayer. Phonon DOS mismatch was investigated to explain the improvement to the TBC. The PDOS of HfO₂ or ZrO₂ has approximately 700% larger overlap with the PDOS of β -Ga₂O₃ in the low-frequency acoustic phonon region responsible for most heat transport compared to the PDOS of sapphire. This suggests that the insertion of a thermal bridge interlayer can provide a potential solution for the reduction of SHE in β -Ga₂O₃ based devices. This work also demonstrates a general approach to enhance thermal transport across the interface between two materials with a large mismatch in phonon states, by introducing an intermediate layer of a material whose phonon states can bridge the mismatch between the original materials, which confirms previous theoretical predictions [29], [30].

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