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Title: *Simulation and Optimization of an In-plane Thermal Conductivity Measurement Structure for Silicon Nanostructures*

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ABSTRACT

Silicon-on-insulator (SOI) based measurement structures have recently been developed to measure the thermal conductivity of nanostructured materials. For example, suspended steady-state measurement structures fabricated from SOI wafers are often used for measuring the in-plane thermal conductivity of thin silicon films as the heat transfer is confined to the lateral direction. However, few researchers have focused on optimizing the important structural and measurement parameters, such as geometry and applied heater power levels to ensure accurate measurements. In this work, a pre-existing suspended steady-state joule heating measurement design with a large suspended region (~10 mm^2) is first simulated and compared with results from literature. Then, we develop a smaller-scale (suspended surface area ~500 μm^2) structure for the measurement of porous nanostructured silicon materials and optimize it by maximizing the measurement accuracy for the range of expected sample thermal properties.

INTRODUCTION

Nanostructured silicon has attracted significant attention in recent years and characterizing the thermal properties is important due to their use in applications including thermoelectric, thermal sensors, and MEMS actuators [1]. Introducing micro/nano-scale features such as periodic pore structures can reduce the thermal conductivity of silicon thin films. However, the electrical conductivity may not be severely impacted if the features are large compared to the mean free path of electrons. With low thermal conductivity and high electrical conductivity, silicon nanostructures are expected to be promising, potentially low-cost, thermoelectric materials [2].

Several measurement structures using silicon-on-insulator (SOI) wafers have been developed to measure the in-plane thermal conductivity of nanostructured silicon [3]. The SOI

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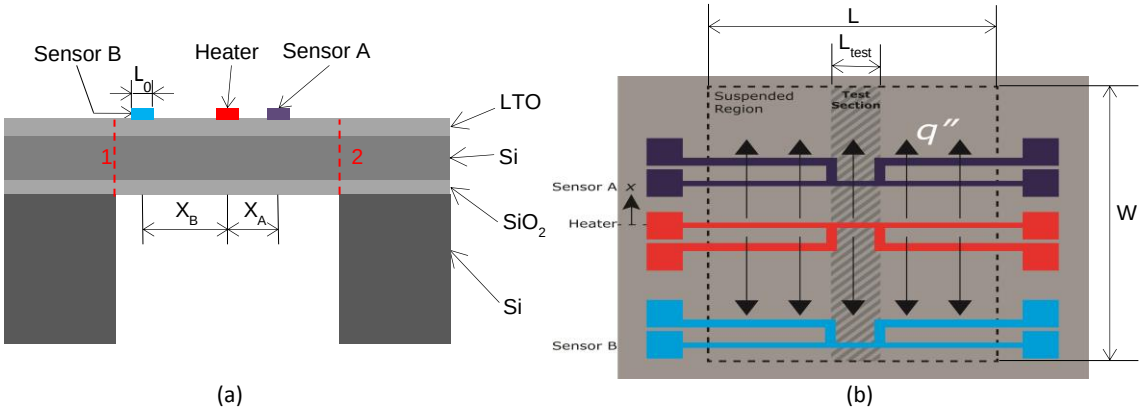

Figure 1. (a) Cross-sectional and (b) top view schematic of the in-plane thermal conductivity measurement structure [not to scale]. Resistive metal lines are patterned on the suspended sample to measure the thermal properties. Current flowing through the center resistive line (heater) generates a heat flux, which is conducted to the edges of the sample region. In the test section (*e.g.* the center portion of the suspended region), the heat flow is generally one-dimensional. The remaining two metal line (sensosr A and B) are used as temperature sensors and the in-plane thermal conductivity is determined by measuring the temperature at these two locations as a function of input heater power.

substrate provides an ultra-thin, high purity, single crystal silicon layer (device layer) attached to a buried silicon dioxide passivation layer (BOX layer), on a bulk silicon substrate (handle wafer). The BOX layer provides a convenient etch stop when fabricating nanostructures from the silicon device layer and also allows for precise suspension of the silicon thin film device layer. Thus, SOI wafers are the chosen starting material for many thermal transport studies of silicon micro/nanostructures. Suspending the thermal measurement structure confines the heat transfer to the lateral direction, which makes these suspended structures useful for measuring the in-plane thermal conductivity. Previous measurements with these types of structures yielded interesting results for the in-plane thermal conductivity of silicon microstructures [4, 5]. However, few researchers focused on the impact, and optimization of, important structural and measurement parameters such as heater and sensor geometry and current intensity. Numerical modeling allows optimization of these parameters prior to experimentation to ensure accurate measurement results.

In this work, we focus on silicon test structures fabricated from SOI wafers as shown in Figure 1. Heat generated at the center metal heater line is conducted across the thin film to the unsuspended portions of the sample, which act as heat sinks. The heat flow is nearly one-dimensional in the test section near the center of the heater line. Two additional metal lines, used as resistive thermometers, measure the resulting temperature profile as a function of input heater power. For both the heater and sensor lines, voltage probes are connected near the center of the metal lines to measure the resistance of the test section only, which is dependent on the temperature of the metal lines. While these types of structures have been used at a larger scale (~10 mm^2) to measure thermal transport in silicon thin films [5, 6, 7, 8], they have not yet been adapted to the scale needed to measure nanostructured films. Specifically, much smaller suspended regions are required due to challenges of patterning large surface areas with nanoscale features.

In this manuscript, we present the results of simulations used to optimize the geometry and

test conditions for measuring the thermal conductivity of nanostructured silicon materials. First, we compare the thermal COMSOL simulations with existing experimental data for similar measurement structures. Then, we optimize the design of suspended steady-state joule heating measurement structures for porous nanostructured silicon materials to maximize the measurement accuracy for the range of expected sample thermal properties.

SIMULATIONS OF EXPERIMENTAL GEOMETRY

Two-dimensional and three-dimensional COMSOL Multiphysics® models of the geometry allow optimization of the measurement structure in terms of geometrical parameters and test conditions (applied current levels, etc.). Fitting the simulated data with the simple, one-dimensional analytical model, which will also be used to fit the experimental data, predetermines the maximum accuracy of the thermal conductivity measurement and facilitates optimization the device configuration.

Simulations of the entire cross-section, shown in Figure 1, confirm that the temperature at the boundary of the suspended region (as shown in Figure 1(a)) is approximately constant. As shown in Figure 2, this boundary temperature does not vary significantly with increasing applied heater and sensor currents. Although there is a slight offset from the set base temperature, it is negligible compared to the temperature rise (~5K) at the heater location and can be considered as constant temperature when applying the boundary conditions. After confirming this assumption, further simulations confine the simulation domain to suspended region for efficiency.

Then, two-dimensional heat transfer in suspended regions is simulated for measurement device designs with micro and nano scale structures. Radiation heat loss is neglected as the

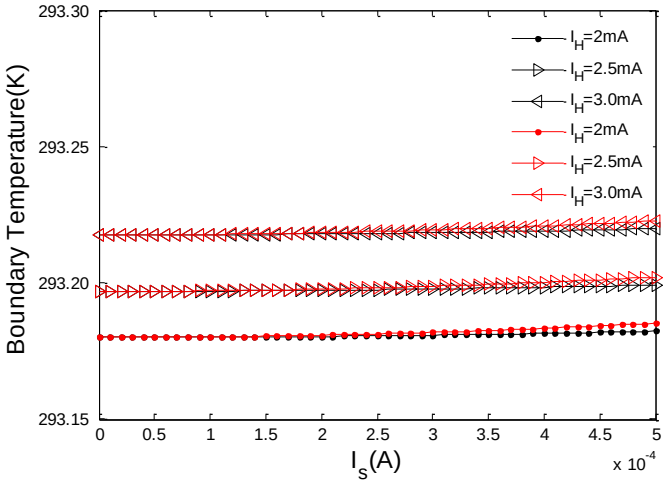

Figure 2: Impact of heater and sensor currents on temperature of at the boundary of the suspended region (see Fig. 1, boundary marked with red dashed lines). The minimal temperature rise above the set base temperature (293.15 K) with all applied heater and sensor current level shows that the constant temperature assumption used in later models accurately approximates the system, which allows the models to be confined to the suspended region

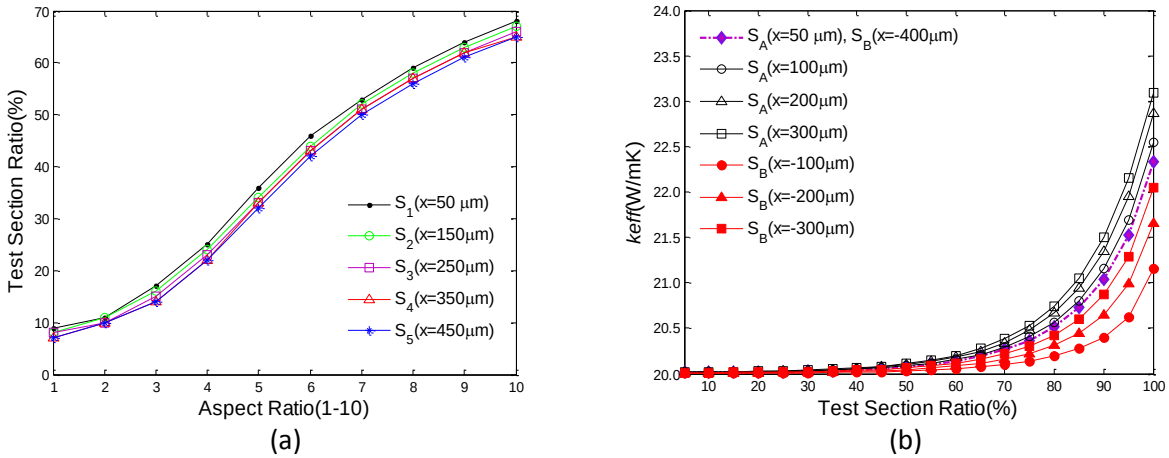

Figure 3: (a) Impact of the aspect ratio (*AR=L/W*) of the suspended region on the relative width of the test section (test section ratio = L_{test}/L) for various sensor placements for the large area measurement devices. (b) The effective thermal conductivity as a function of the relative width of the test section as a function of the sensor placement. The heater and sensor currents are I_H=2.5 mA and I_S=0.1 mA, respectively, and the trends are similar for different current levels. The input thermal conductivity of the simulated material is 20 W/mK.

temperature rise is confined to 5K, and convection effects are neglected because experiments will be conducted in vacuum. Only the center area of the suspended region comprises the test section to avoid two-dimensional effects, which allows a simplified data analysis using an approximate one-dimensional heat conduction solution. The maximum allowable width of the test section, L_{test}, is found by determining the location where the temperature decreases by 0.5% from the centerline temperature rise. The test section ratio, which compares the test section width to the total suspended width (L_{test}/L), depends on the aspect ratio of the suspended region and the position of the sensors as shown in Figure 3.

Assuming one-dimensional heat conduction, the in-plane thermal conductivity is easily extracted,

$$k = \frac{\left(\frac{Q}{2}\right)*(x_A - x_B)}{S*(T_A - T_B)} \quad (1)$$

where Q is the heater power dissipation in the test section, (x_A-x_B) is the distance between sensor A and B, S is the cross-section area of the test section, and T_A and T_B are the average temperatures for sensor A and B in the test section, respectively. When the thermal conductance of the silicon dioxide insulating layer is negligible, the thermal conductivity extracted using this expression is accurate. However, as the thermal conductivity of the sample decreases and the conductance of the sample is comparable to that of the oxide region, the two layers must be treated in parallel. Figure 4 shows the extracted thermal conductivity from the large-area measurement structures with and without correcting for the conduction through the oxide layer.

The suspended region aspect ratio, the heater and sensor current, and their positions on the measurement accuracy impact the performance of the measurement device. A detailed model

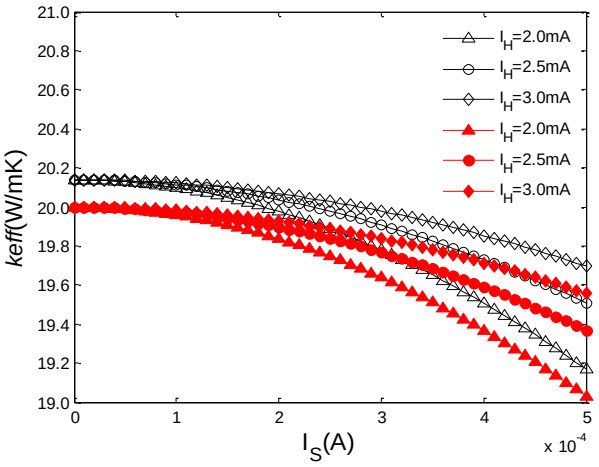

Figure 4: Extracted thermal conductivity measurement from simulations of silicon microscale test structures. The effective thermal conductivity with (red filled markers) and without (black open markers) correcting for thermal conduction in the SiO_2 layer as a function of sensor current with varying heater current. Here, sensor positions are fixed at x_A=10 μm and x_B=-400 μm.

including the radiation heat loss, the thermometer geometry, and the structure outside the suspended region will be included in future studies. In addition to thermal performance, the difficulty of sample fabrication must be considered when designing these types of structures.

RESULTS

Large Area Design: Comparison to Literature

We initially simulate device designs similar to that used by Asheghi *et al.* [5] with a suspended region on the order of 0.1 cm^2. Specifically, the suspended region is L x W = 10000 μm x 1000 μm with sensors placed at x_A = 10 μm and x_B = 400 μm from the heater line, and the center L_{test} = 1000 μm comprises the test section. Figure 4 shows simulation results for thermal conductivity measurement in silicon microstructures. Here, the actual thermal conductivity of the simulated material was 20 W/mK at room temperature.

First, the required current heater and sensor levels must be determined. We consider the impact of the current levels on the thermal conductivity extracted from the simulations as an indicator of the allowed current ranges. As shown in Figure 4, the measurement accuracy decreases with increasing sensor current and this situation is partly improved by using a larger heater current. At large sensor current, heating at the sensor lines becomes significant compared to the applied heater power and distorts the temperature profile yielding poor results for thermal conductivity.

Then we investigate the impact of the aspect ratio (AR=L/W) of the suspended region on the relative width of the test section (test section ratio= L_{test}/L) for various sensor placement positions. Figure 3(a) reveals that the allowed width of the test section

increases with increasing aspect ratio. Considering the fabrication difficulties rising with the larger aspect ratio, aspect ratio with 5 to 6 are an ideal choice. In addition, Figure 3(b) shows the effective thermal conductivity as a function of the relative width of the test section depending on the sensor placement. The measured thermal conductivity begins to deviate greatly from the true value when test section ratio increases. The test section width can be larger and still achieve the same accuracy in the extracted thermal conductivity if the sensors lines are placed closer to the heater. While this allows for a higher electrical resistance of the test section and thus more accurate temperature measurements, the improvement is even less than 5%, and might be mitigated by reducing the temperature difference between the two sensor lines.

New Small Area Design

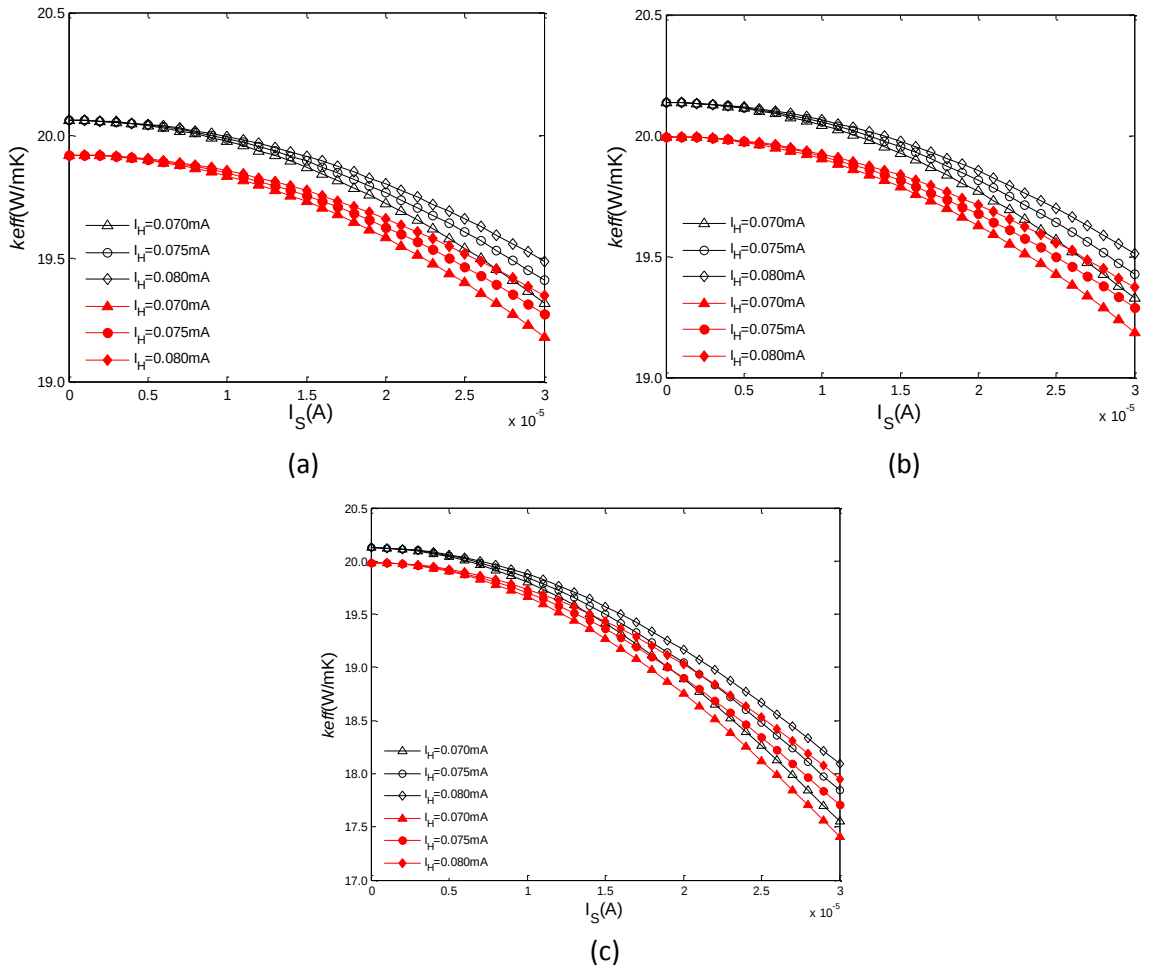

Figure 5: Simulation results for thermal conductivity measurement in smaller scale silicon nanostructures for various sensor placements: (a) x_A=0.1 µm, x_B=1 µm; (b) x_A=0.2 µm, x_B=1 µm; and (c) x_A=0.1 µm, x_B=4 µm. The input thermal conductivity of the simulated material is 20 W/mK.

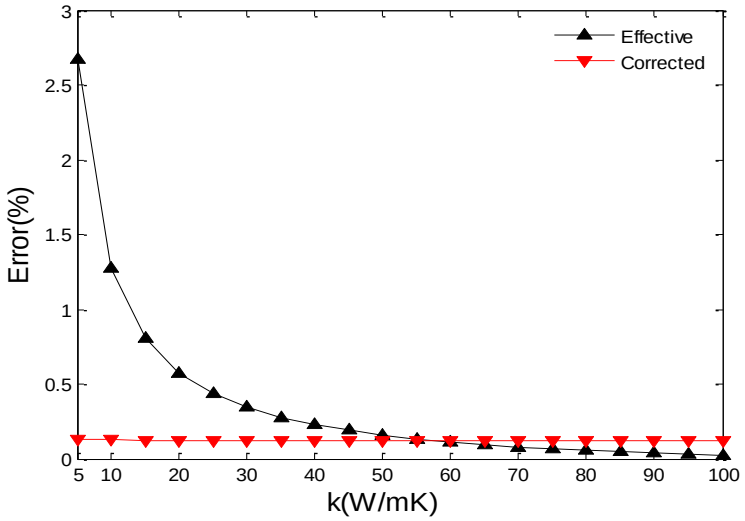

Figure 6: Impact of the sample thermal conductivity on the measurement error for a structure with a 10 μm x 50 μm suspended region and sensors positioned at at x_A=0.2 μm and x_B=1.0 μm. The heater and sensor currents used in this structure are I_H=0.075mA and I_S=0.005mA. The error is defined as ($k_{effective}$-k)/k*100% for the thermal conductivity extracted using equation (1) and ($k_{corrected}$-k)/k*100% after correcting the thermal transport via SiO_2, respectively.

A measurement structure with a much smaller suspended region is required for characterization of nanostructured materials due to challenges of, and time required for, patterning large surface areas with nanoscale features. Appling the same methodology used in microscale measurement structures simulation, a 10 μm x 50 μm suspended region is simulated with COMSOL®. The test section used to extract the thermal conductivity is 20% of the width of the suspended region (L_{test} = 10 μm).

Figure 5 shows the simulation results for thermal conductivity measurement in silicon nanostructures with various sensor placement positions. Two dimensional effects play a significant role for the smaller scale structures. With some placements of the sensor lines, an accurate thermal conductivity value cannot be extracted from the simulated measurement data, even correcting for the thermal transport through the SiO_2 (as shown in Figure 5(b)). This is different than for the large area structure where the same relative sensor placement, x_A/L_0=5, where L_0 is the width of sensor line, leads to accurate thermal conductivity data and is likely due to the 2-D heat transfer effects. These results illustrate that the choice of sensor placement is more critical in these smaller structures. Specifically, the absolute distances should be given more consideration for measurement in nanostructures. In addition, the measurement accuracy is improved if the second sensor line is placed closer to the heater (as illustrated by comparing the panels in Figure 5).

Finally, we vary the thermal conductivity of the sample for a structure with a 10 μm x 50 μm suspended region, sensor A placed at x_A=0.2 μm, and sensor *B* placed at x_B=1.0 μm. Figure 6 shows the error in the extracted thermal conductivity (with and without correcting for thermal transport through the oxide layer) compared to the input thermal

conductivity. The error is small for measuring thermal conductivities simulated from 5 W/mK to 100 W/mK, which is an expected range for the thermal conductivity of silicon nanostructures [9, 10]. For the low thermal conductivity measurement, correcting the thermal transport through the SiO_2 yields more accurate results due to the similar magnitude of thermal conductances in these two layers.

CONCLUSIONS

Structures for measuring thermal transport in silicon microstructures and nanostructures are simulated using COMSOL® in order to optimize the device design. The impact of suspended region geometry, heater and sensor currents, and sensor placement on the measurement accuracy is studied for both the large area structures previously used to characterize microscale silicon films, and for new small area structures, designed to measure silicon nanostructures.

Analysis of the thermal measurement accuracy and fabrication constraints must be combined in order to choose suitable design parameters. For example, while increasing the aspect ratio improves the measurement accuracy, large aspect ratio devices are challenging to fabricate. In addition, sensors positions closer to the heater help the one-dimensional heat transfer analysis, but the measurement of voltage (α T) loses accuracy experimentally due to the resulting low voltage (temperature) difference between these two sensors. Combining the simulation results with practical fabrication and experiment limitations, optimized design configurations are predicted from these simulations. Beyond the analysis of silicon-based nanostructures, this device configuration can be used as a platform for other materials.

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