Design and Characterization of a Thermal Test Vehicle with Embedded Phase Change Material

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***Abstract*—Phase change materials (PCMs) are a promising passive thermal management solution for electronics. However, their integration outside of the microelectronics package introduces additional thermal resistance between the PCM and the heat source, and makes them an non-viable solution for mobile devices due to spatial constraints. In this study, we integrate PCMs within the silicon chip in close proximity to the heat source. We fabricate thermal test vehicles (TTVs) with realistic mobile chip form factors to experimentally assess the performance of a silicon device incorporated with metallic PCM (specifically, a eutectic Bi/In/Sn alloy). The embedded PCM TTV demonstrates a noteworthy 2.3× extension in 'on' operational time during temperature cycling compared to an all-silicon benchmark TTV. Furthermore, it achieves a 10% reduction in the overall maximum temperature rise and a significant 47% decrease in temperature fluctuations during duty cycling. Degradation in the thermal performance of an embedded PCM TTV is observed due to increases in the PCM melt/freeze temperature. This phenomena occurs as result of incomplete phase transitions during the 'on' or 'off' portions of the duty cycle. However, temperature cycling for 5000 cycles confirms the stability of the embedded PCM for an extended operational period provided that complete melting/freezing occurs during each cycle. The substantial decrease in temperature fluctuations is crucial for enhancing device thermal stability, emphasizing the potential of embedded PCMs in ensuring reliable performance over extended operational periods.**

***Index Terms*—Thermal Management, Phase Change Materials, Embedded Cooling, Microelectronics, Thermal Test Vehicle, Semiconductor Fabrication**

I. Introduction

Phase change materials (PCMs) have been explored for application as effective thermal buffers within electronic devices with transient power profiles. They can either be used to extend processor operational time through melting for a large power pulse, or improve thermal stability through repeated melting and freezing for cyclic power loads. The majority of past PCM studies have focused on PCM heat sinks packaged externally from the active chip module. While this strategy does improve the transient thermal response of the device, the presence of multiple interfaces between the PCM-laden heat sink and the heat source limits the effective use of the PCM within the system. Additionally, spatial design constraints for mobile devices make such a macroscale strategy impractical. A more effective strategy involves the integration of PCM near the heat source at the silicon chip level. This integration would both eliminate resistance pathways that typically exist when using external heat sinks, and make PCMs a viable thermal management strategy for mobile devices.

A few studies have explored die-level integration approaches for PCM thermal buffers. Soupermanien *et al.* [1] integrated PCMs within a power electronics module, reporting a significant reduction of 28°C in hotspot temperatures. Gurrum and colleagues [2] etched PCM microchannels within a power electronics die, and observed temperature reductions of up to 25°C. Green, Federov, and Joshi [3] implemented a composite PCM-heat spreader structure within a silicon die, and noted an extension of device operating times by over 650%. For duty cycle based power profiles, Shao *et al.* [4] demonstrated the viability of an embedded PCM cooling strategy for computational sprinting. Similar temperature swing reductions of 21% were also observed by Kim *et al.* [5] for a gallium nitride device with integrated PCM. Prior computational studies [6, 7] highlighted that an embedded PCM cooling strategy reduces both peak temperatures and transient temperature fluctuations, and presented machine-learning based optimization strategies to balance high thermal conductivity silicon pathways and high thermal capacitance PCM zones for a device with an embedded PCM layer.

Although these past studies highlight the promise of embedded PCMs at reducing thermal volatility, there is a need to experimentally verify an embedded PCM thermal management approach for a fully encapsulated PCM device and for extended operational times. Although a silicon interposer with integrated composite materials was proposed and fabricated by Ollier *et al.* [8], that work did not experimentally validate the system with a transient power profile. Thus, there is clearly a need for systematic experimental evaluation of the impact of embedding PCM within the device layer of an electronic device.

This work builds upon our prior computational studies on embedded PCM cooling [6, 7] and details the successful fabrication of a fully embedded PCM thermal test vehicle (TTV). To our knowledge, this is the first such device to be fabricated *and* validated across a range of transient power profiles. In this work, we first detail the design and fabrication process of our TTV and describe the experimental platform. Then, we present experimental results for temperature cycling and duty cycling for an embedded PCM TTV compared to an all-silicon control TTV. Finally, we demonstrate the stability of an embedded PCM TTV for 5000 cycles.

II. Methods

A thermal test vehicle (TTV) was developed to provide a controlled environment for testing and analyzing the thermal behavior of the proposed embedded PCM device against an all-silicon benchmark. The TTV offers the advantage of replicating realistic operational conditions, as it enables independent control of multiple power zones with precise temperature measurements. The TTV was connected to a custom printed circuit board (PCB) via gold wire bonds to interface with a data acquisition and control system for thermal benchmarking.

A. Thermal Test Vehicle Design

We consider an 11 $\times$ 11 mm device that consists of two 400 µm thick bonded silicon substrates (see Fig. 1(a-b)). A 250 µm PCM layer is etched in the backside of the top silicon substrate to embed the PCM close to the heat source. In this study, we use a eutectic bismuth-tin-indium alloy [9] (also called Alloy/Solder 174) with a melt temperature of 77 °C. The bottom surface of the silicon device layer generates heat and is electrically insulated with a 250 nm silicon-dioxide layer. To emulate transient heat fluxes in real electronic devices, the heat generation occurs as periodic square wave. The bottom and top surfaces of the device are exposed to natural convective cooling and forced cooling, respectively. The maximum viable PCM layer cross section is 9 $\times$ 9 mm, which allows for a 1 mm silicon containment/bonding zone at the edge of the chip. The device operates at an average ambient temperature of $T_0 \approx 295$ K.

The device features a heating layer consisting of five distinct zones, each with an individual resistance temperature detector (RTD) to provide localized temperature readings. This approach enables targeted and controlled heat generation, allowing for comprehensive analysis of the thermal performance of the device under various conditions. The heating zones are patterned as squares within a 9 $\times$ 9 mm area, with one hotspot heater in the center and four surrounding background heaters (see Fig. 1(c)). This layout ensures that the heating zones align with the PCM layer in the other wafer, facilitating efficient heat transfer. Four-wire RTDs in each zone provide accurate temperature measurements, allowing for detailed analysis of temperature distributions across the device.

B. Thermal Test Vehicle Fabrication

Each TTV consists of two components - a heating chip and a filled PCM reservoir - that are combined to produce a single 11 $\times$ 11 mm wide, 800 µm thick silicon device (see Fig. 2). Heaters and sensors are fabricated on a 100 mm diameter, 400 µm thick, double-side polished silicon wafer (procured through Pure Wafer). Reservoirs for the PCM are fabricated on a second (identical) silicon wafer. All fabrication was performed at the Birck Nanotechnology Center at Purdue University. All lithography was performed using the Heidelberg MLA150 Maskless Aligner, a 10 µm AZ9260 photoresist layer, AZ400K 1:3 aqueous developer solution, and acetone (for photoresist removal and lift-off). The fabrication process is divided into three parts: (1) heater/sensor fabrication on the first wafer (Section II-B1), (2) PCM reservoir etching on the second wafer (Section II-B2), and (3) dicing, PCM dispensing, and bonding (Section II-B3).

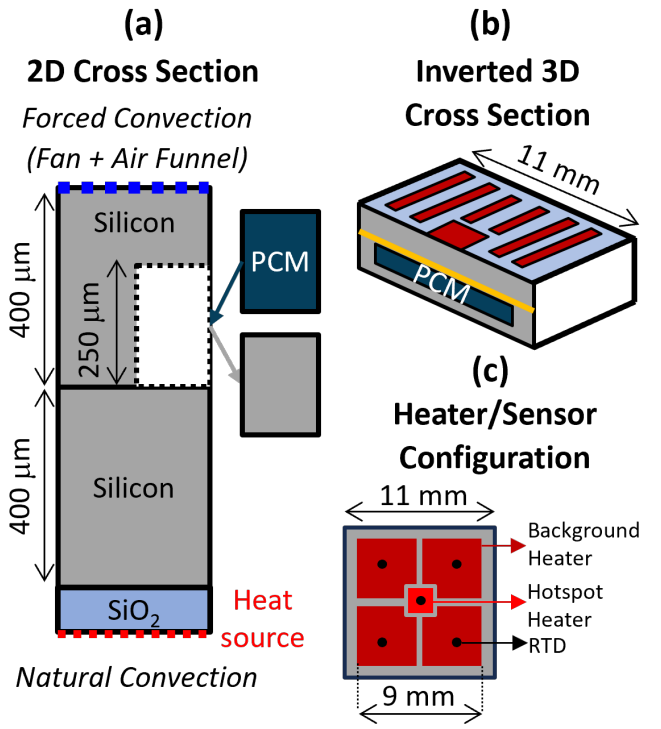

Fig. 1. (a) *2-D and* (b) 3-*D schematics of the fabricated device with embedded PCM zone*. The device combines a heating chip (bottom silicon substrate) and a 250 µm PCM reservoir (top silicon substrate) to create a single, 800 µm thick PCM embedded device. The bottom heated surface experiences natural convection, while forced air convection cools the top surface of the chip. The 11 $\times$ 11 mm test chip has a 1 mm containment edge that is used to bond the layers together. Thus, the viable region for PCM is 9 $\times$ 9 mm. (c) *Schematic of the heaters and sensors on the test chip.* Five heaters (one hotspot heater in the center and four background heaters), each with a 4-wire RTD for localized temperature reading, fit within the 9 $\times$ 9 mm zone.

1) Wafer 1: Heater/Sensor Fabrication: The TTV utilizes thin-film platinum heaters to generate heat in five distinct heating zones, with each zone equipped with a platinum 4-wire RTD for local temperature measurement. A 4-wire resistance measurement eliminates the effect of lead wire resistance for accurate temperature readings. Platinum was chosen for the heating element due to its high resistivity to oxidation, and for the RTD due to its linear relationship between resistivity and temperature. Both the heaters and RTDs are patterned and fabricated in the same step to simplify the fabrication process. Gold lead wires are used to connect the heaters and RTDs to a printed circuit board (PCB). Gold was chosen for this application due to its high resistance to oxidation, which ensures a reliable electrical connection over time. Additionally, gold-to-gold wire bonding provides a strong and durable connection between the TTV and the PCB. Overall, the use of gold lead wires in conjunction with platinum heaters and RTDs in the thermal test vehicle enables accurate temperature measurement and reliable heater control.

First, a 250 nm thick dielectric silicon dioxide layer was thermally grown (wet oxidation, 1100 °C) (Fig. 2(a)). After

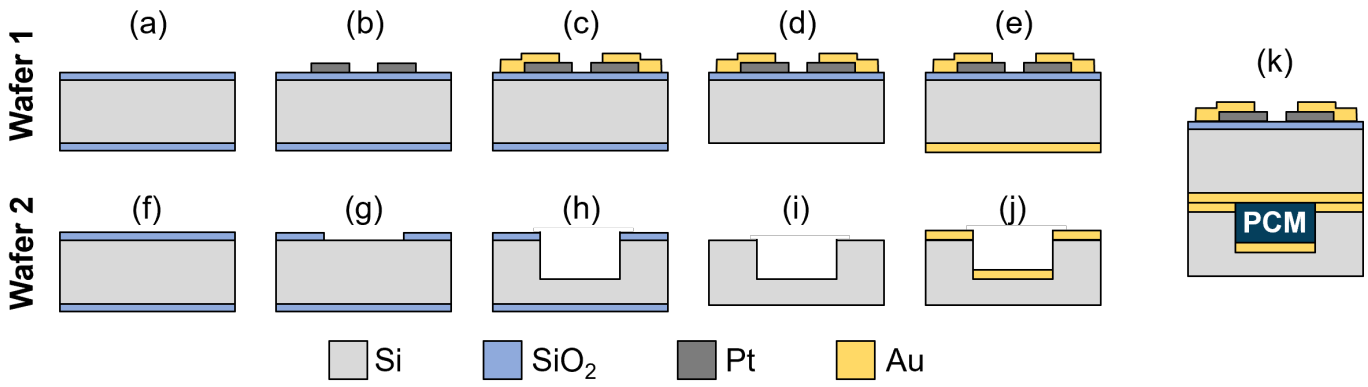

Fig. 2. *Schematic of thermal test vehicle (TTV) fabrication process.*: The heater/sensor wafer (wafer 1) and the wafer with the PCM reservoirs (wafer 2) undergo independent processing before being bonded. **(a-e) Wafer 1 Process**: (a) Grow 250 nm oxide; (b) Deposit Ti-Pt heaters/RTDs; (c) Deposit Ti-Au trace wire; (d) Remove bottom-side oxide; (e) Deposit Ti-Au thermocompression bonding layer; **(f-j) Wafer 2 Process:** (f) Grow 1.2 µm oxide; (g) Pattern and etch oxide to create oxide hard mask; (h) Etch silicon to create PCM reservoir; (i) Remove oxide; (j) Deposit Ti-Au thermocompression bonding layer. Each wafer is diced and the PCM dispensed into the reservoir. **(k) Thermocompression bonding** to produce the embedded PCM TTV.

lithography, a 5 nm layer of titanium, and a 20 nm layer of platinum were deposited by e-beam evaporation using the CHA E-Beam Evaporator (Fig. 2(b)). After lift-off and trace-wire lithography, the same deposition process was used to deposit a 10 nm layer of titanium, and a 400 nm layer of gold (Fig. 2(c)). In both deposition processes, titanium was first deposited to function as an adhesive layer. Silicon dioxide on the non-deposited side was then removed using a buffered oxide etch solution (Fig. 2(d)). The heating/sensor wafer is shown in Fig. 3(a).

2) Wafer 2: PCM Reservoir Etching: All PCM reservoirs are etched on the second wafer simultaneously using deep reactive-ion etching (RIE) via the Bosch process. The Bosch process allows for deep etches while ensuring vertical side walls. Since it damages photoresist, a silicon dioxide hard mask is used.

On the second wafer, a 1.2 µm thick silicon dioxide layer was thermally grown (wet oxidation, 1100 °C) to function as a hard mask for the silicon etching process (Fig. 2(f)). After lithography, silicon dioxide was dry-etched (STS AOE) to create an oxide mask (Fig. 2(g)), followed by silicon dry-etching (STS-ASE) to create 250 µm PCM reservoirs (Fig. 2(h)). The PCM reservoir wafer is shown in Fig. 3(b). Silicon dioxide was then removed from both sides of the wafer using a buffered oxide etch solution (Fig. 2(i)).

3) Dicing, PCM dispensing and bonding : Both wafers were first solvent cleaned. Then, a 50 nm layer of Ti and 500 nm layer of Au were deposited on the bottom side of the first wafer (heater/sensor wafer) and top side of the second wafer (PCM reservoir wafer) using e-beam evaporation (Fig. 2(e and j)). The wafers were then diced (Disco DAD641) to produce 11×11 mm sections of heating/sensing chips and PCM reservoirs.

The reservoir volumes were calculated by using the measured depth (KLA-Tencor P-7 Profilometer) and surface area (from the lithography mask). A eutectic bismuth-tin-indium alloy (Alloy 174) with a melt temperature of 77 °C was used as the embedded PCM in the TTV and was procured via RotoMetals [10]. PCM properties are provided in Table I

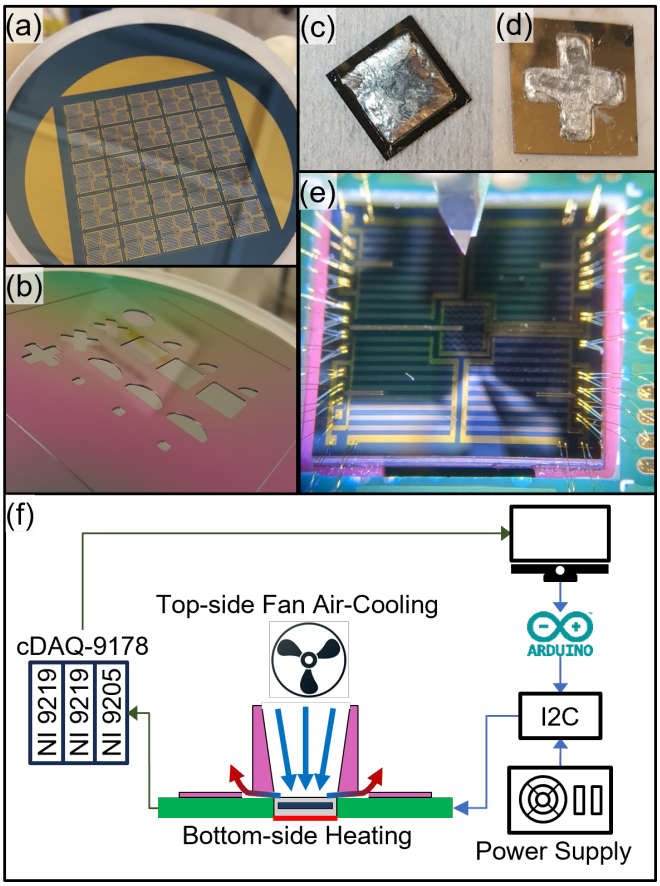

Fig. 3. Images highlighting the progression of the experimental methods used to evaluate an embedded PCM cooling approach: (a) wafer 1 with a grid of heater/sensor chips; (b) wafer 2 with etched PCM reservoirs; (c-d) PCM reservoirs with dispensed Bi/Sn/In PCM; (e) wire-bonded TTV with embedded PCM. (f) Schematic of the experimental platform.

and can be referenced to experimental analysis performed by Fukuoka and Ishizuka [9]. Dispensing of the liquid PCM was done via a pointy-tipped swab. Handling metallic PCM is challenging due to its high surface tension. To overcome this,

TABLE I
PROPERTIES OF EMBEDDED ALLOY-174 PCM

Composition	$\mathbf{T_m}$ (°C)	$\rho_{\mathbf{solid}}$ ($\mathrm{kg/m^3}$)	$\rho_{\mathbf{liquid}}$ ($\mathrm{kg/m^3}$)	$\mathbf{k_{solid}}$ (W/mK)	$\mathbf{k_{liquid}}$ (W/mK)	$\mathbf{C_{p,solid}}$ (J/kgK)	$\mathbf{C_{p,liquid}}$ (J/kgK)	$\mathbf{L_H}$ (J/kg)
Bi 57%, In 17%, Sn 26%	77	8780	8200	35.8	28.8	401	883	47730

a thin metal oxide film was first created on the reservoir walls by pressing a small amount of PCM against the walls. This was followed by a slow and careful dispensing of the PCM while intermittently measuring the mass of the reservoir on a weighing scale. To prevent overfilling, the PCM was dispensed in a liquid state (expanded state) and a 5 µm safety margin was used when calculating allowable PCM volume. Photographs of two dispensed PCM reservoirs are shown in Fig. 3(c-d).

A filled reservoir die was then stacked and aligned with a heater/sensor chip, and bonded using thermocompression. The temperature and pressure were slowly increased over the course of 30 minutes, and the stack was exposed to 300 °C and 370 kPa for 60 minutes to produce a single TTV.

After wire-bonding, the TTV RTDs were calibrated in an oven, and an Omega 2252 thermistor was used to monitor the oven temperature. A linear regression was used to determine the relation between the measured resistance and operating temperature for each RTD.

C. Experimentation Platform

The experimental evaluation of the thermal test vehicle (TTV) was carried out using a platform that enables individual control of each heater zone, while simultaneously acquiring temperature data from the TTV. The platform consists of a custom printed circuit board (PCB) that interfaces the TTV to the power supply and data acquisition systems. Heater control and data acquisition are fully automated via LabVIEW.

The TTV was first adhered to a custom 3-D printed air-funnel that attaches onto the PCB. The fan then attaches to the top of the air-funnel and cools the TTV from the top. The heaters and RTDs were electrically connected to the PCB using gold wire bonds (a closeup wirebonded TTV is shown in Fig. 3(e)). The PCB contains a voltage divider circuit (shown in Fig. 4) that is wired in parallel, and a shunt resistor that is wired in series with each heating zone. The voltage across the divider circuit and shunt resistor is measured and used to calculate the power generated in each heating zone using $P = I_{flow}V_{drop}$, where $V_{drop} = V_{1,measured}(R_1 + R_2)/R_1$ and $I_{flow} = V_{shunt,measured}/R_{shunt}$.

A single DC power supply (HP 6428B) powers the heaters within the TTV. Individual control of the heaters was achieved through a custom-designed inter-integrated circuit (I2C) that interfaces with an Adafruit servo-driver (PCA9685). The circuit utilizes pulse width modulation to downscale the voltage from the power supply to the desired voltage. Communication between LabVIEW and the I2C happens using an Arduino Uno. The facility was first constructed by Collier Miers [11] and was retrofitted for this study. The I2C circuit was designed by Bert Gramelspacher.

Voltage and temperature monitoring occur using a NI cDAQ-9178 with three modules: two universal analog input modules (NI9219) for four-wire resistance monitoring of the all RTDs and two-wire resistance monitoring of an OMEGA 2252 thermistor (to measure ambient temperature), and a voltage module (NI9205) for monitoring the voltages across the shunt resistor and the voltage divider. A schematic of the experimental platform is shown in Fig. 3(f).

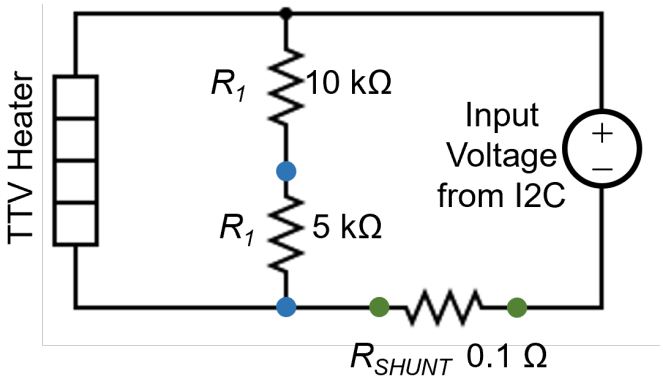

Fig. 4. Electrical circuit showing the resistor setup on the PCB that is used to measure heater power. Voltage is measured across R_1 (shown across blue dots) and R_{shunt} (shown across green dots) to calculate the heater voltage drop and current flow respectively.

III. RESULTS AND DISCUSSION

Given the optimal effectiveness of PCMs in transient power profiles, rectangular pulse heating is used to facilitate repeated cycles of melting and solidifying. A transient usage scenario is emulated through two distinct types of tests: temperature cycling and duty cycling. In the temperature cycling tests, the hotspot temperature undergoes oscillations between two setpoints, mimicking a safety margin 'cut-off' temperature and a cooler 'restart' temperature (for example, the heaters being powered on until a temperature sensor reach 85 °C and then the heaters are turned off until all sensors cool to 65 °C). Duty cycling tests involve fixed on and off times (for example, 2.5 s on and 2.5 s off) to mimic consistent power profiles as seen in computational sprinting [4]. In all experiments in this study, all heaters are switched on and the center hotspot heater has a heat flux 3× higher than the background heaters.

Although the intent is uniform power throughout the 'on' portion of the temperature/duty cycle, the heat dissipation during a single pulse decreases slightly over the duration of the pulse due to the heater control scheme. As the temperature of the TTV increases, the resistance of the platinum heaters increases. Since the voltage across the heaters remains fixed, the increase in resistance causes a slight decrease in power. Thus, the average power over the pulse duration during the final heating cycle is reported here.

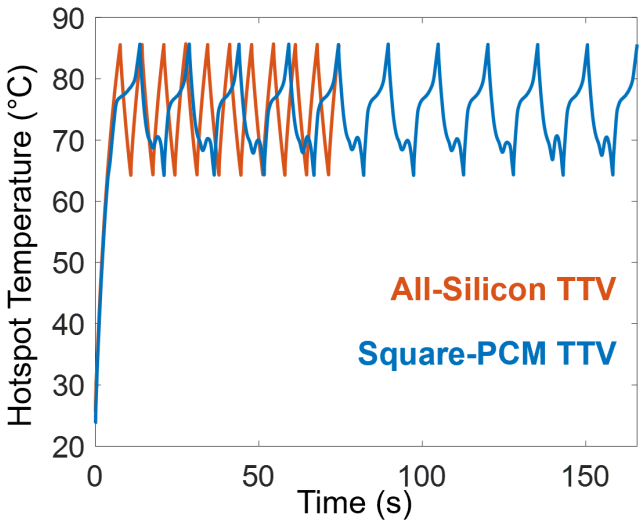

Fig. 5. Absolute hotspot temperature during the temperature cycling experiment, where the TTV hotspot oscillates between a 85 °C 'cut-off' temperature and a 65 °C 'restart' temperature, for the TTVs (blue) with and (orange) without the square-shaped PCM reservoir. This study focused on 11 'on' and 10 'off' cycles with 2.50 W of heat during the 'on' cycle. The square-PCM TTV extends the 'on' operation time by 2.3× due to PCM melting but also extends the 'off' duration due to PCM freezing. Overall, both TTVs have a similar average energy dissipation rate.

Results from two embedded PCM TTVs are reported here: (1) one with a 9 × 9 mm square PCM reservoir (covering the entire allowable PCM volume) (see Fig. 3(c)) and (2) one with a plus-shaped PCM reservoir with 3 mm wide edges (see Fig. 3(d)). The sample with the square-shaped PCM reservoir is used for the temperature cycling (Sec. III-A), duty cycling (Sec. III-B), and degradation (Sec. III-C) studies. The sample with the plus-shaped PCM reservoir is used for the extended operation study (Sec. III-D). The thermal performance of the TTVs with the embedded PCM are benchmarked against a TTV that has a solid silicon layer instead of die with a PCM reservoir.

A. Temperature Cycling

For the temperature cycling experiments, the system power is controlled based on the hottest RTD temperature. Specifically, the heaters will switch on until the hotspot RTD reaches a 'cut-off' temperature of 85 °C, then switch off until the hotspot RTD cools down to the 'restart' temperature of 65 °C, after which the heaters are turned back on. These temperature setpoints facilitate for complete PCM melting and freezing during each cycle. This experiment was run for 11 'on' cycles with a power dissipation of 2.5 W and 10 'off' cycles.

For this experiment, the background heaters generate approximately 0.54 W of heat, and the center hotspot heater generates approximately 0.33 W of heat, for a total TTV power of ∼2.50 W. The transient thermal responses of the all-silicon TTV and TTV with the square-shaped PCM reservoir are shown in Fig. 5 as orange and blue lines, respectively.

The TTV with the square-shaped PCM reservoir extends the 'on' operation time during the set number of cycles by 2.3× compared to the all-silicon TTV. Since the PCM melts at 77 °C, the system is able to dissipate 2.3× more energy during a single 'on' phase before reaching the cut-off temperature. However, there was a trade-off, as the 'off' duration time also extends due to PCM freezing (at 70 °C). When comparing the average energy dissipation rate, both TTVs have a comparable performance. The all-silicon TTV completes the 11 'on' cycles at the 75 s mark. At this point, both TTVs have dissipated a total of ∼100 J of heat. Thus, with a similar heat dissipation rate, an embedded PCM TTV could be useful for computational schemes that require a longer 'on' operation duration. Also, more effective active cooling such as a liquid cold plate could significantly reduce the time required for resolidification.

B. Duty Cycling

The duty cycling experiments use a fixed 50% duty cycle with on and off times of 2.5 s each (5 s period) for a total of 120 cycles, or for a total run time of 600 s. The background heaters generate approximately 0.56 W, and the center hotspot heater generates approximately 0.38 W of power during the 'on' portion of the duty cycle, for a total TTV power of ∼2.60 W. The transient thermal responses of the all-silicon TTV and TTV with the square-shaped PCM reservoir are shown in Fig. 6 as orange and blue lines, respectively. Note that the thermal response plots the hotspot temperature rise above the ambient temperature, and not the absolute hotspot temperature.

The TTV with the square-shaped PCM reservoir achieves a significant improvement in thermal performance compared to the all-silicon TTV, reducing the overall maximum temperature increase by 10% from 63 °C to 57 °C. Additionally, it

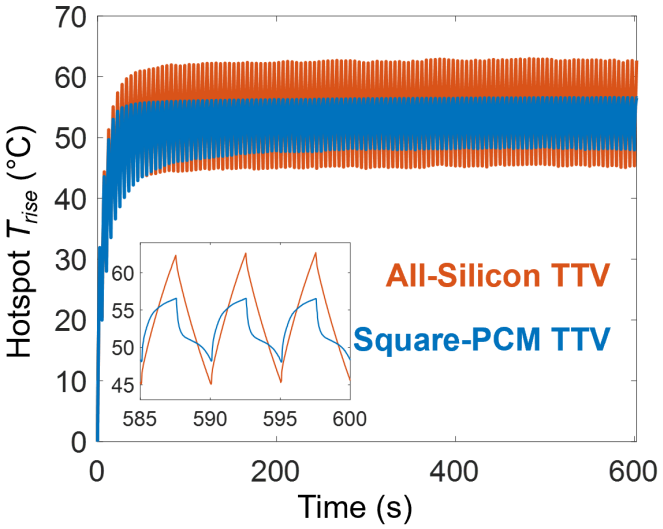

Fig. 6. Hotspot temperature rise (above ambient) for the TTVs (blue) with and (orange) without the square-shaped PCM reservoir. The duty cycling experiment runs for 120 cycles at a 50% duty cycle with a period of 5 s and total power output of 2.60 W during the heating portion of each cycle. The inset on the bottom left focuses on the thermal response for the final three cycles. The square-shaped PCM reservoir decreases the overall maximum temperature rise by 10% (from 63 °C to 57 °C) and also reduces temperature oscillations by 47% (from 17 °C to 9 °C) compared to the all-silicon TTV. This was due to consistent PCM melting/freezing during each duty cycle.

diminishes temperature oscillations by 47%, from 17 °C to 9 °C. The consistent PCM solid-liquid phase transitions during each duty cycle act as a buffer, absorbing excess heat and moderating temperature fluctuations. The observed 47% reduction in temperature oscillations is a key indicator of the thermal stability introduced by an embedded PCM layer.

C. PCM Degradation From Incomplete Melting/Freezing

To understand the impact of aging and repeated cycling on the performance of the PCM thermal buffer, the duty cycling experiment (detailed in Section III-B) is conducted over seven consecutive days at randomly selected times to assess potential PCM degradation. The results of this degradation study for the TTV with the square-shaped PCM reservoir are illustrated in Fig. 7, where the thermal response is presented using a divergent red-to-green color scale that corresponds to successive days.

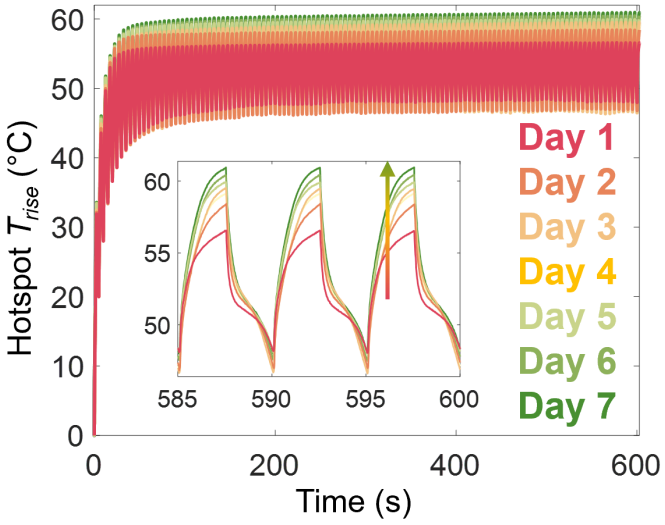

Fig. 7. Hotspot temperature rise (above ambient) for duty cycle testing on seven consecutive days. The inset shows the thermal response of the TTV for the last three duty cycles. The thermal response on the first day is represented in red, while subsequent days exhibit a progressively 'greener' gradient. The thermal response of the final day is depicted in green. The thermal performance decreases progressively due to a significant increase in the PCM melt temperature over time, which may stem from incomplete melting and freezing occurring in each duty cycle.

Figure 7 shows the duty cycle testing results over the seven days. There is an increase in both the overall maximum temperature rise and temperature oscillations with each passing day. This phenomenon can be attributed to shifts in the melting and freezing temperatures. This appears to correlate with incomplete melting and freezing occurring during each duty cycle (as indicated by the absence of a sensible heating temperature spike that is otherwise observed post-melting or post-freezing as seen in Fig. 5). The significant increase in the PCM melt temperature with each subsequent day and slight increases in the PCM freeze temperature leads to or reflects the gradual deterioration in the thermal performance of the system.

However, in other *ad hoc* tests (not shown) where the system was allowed to fully melt and fully solidify, no significant degradation was observed. To study this effect in a more consistent manner, additional testing is conducted on a separate sample as detailed in the following section.

D. Extended Operation

To improve our understanding of the stability of PCM and test the hypothesis that the degradation of the PCM performance is tied to incomplete melting and solidification (as seen in Section III-C), we next conduct an extended temperature cycling experiment with the TTV with the plus-shaped PCM reservoir. Specifically, this system was cycled for 5000 temperature cycles (total run time of ∼21 hours). To accommodate complete PCM melting and freezing, the 'cut-off' and 'restart' temperatures were adjusted to 80 °C and 55 °C, respectively. That is, the heaters switch on until the hotspot RTD reaches 80 °C, then switch off until the hotspot RTD cools down to 55 °C, and then the cycle repeats for 5000 cycles. The results are illustrated in Fig. 8, wherein the temperature responses from cycles 10, 1000, 2000, 3000, 4000, and 5000 are superimposed on top of each other in a scale from dark blue (cycle 10) to light blue/cyan (cycle 5000).

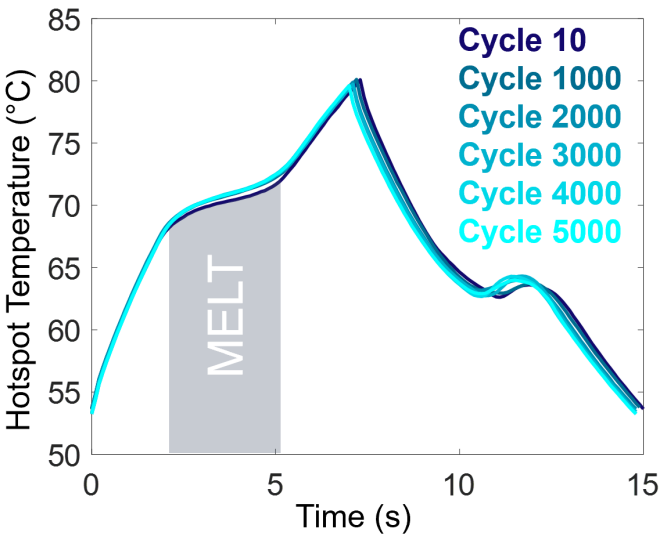

Fig. 8. Absolute hotspot temperature during the PCM stability tests. In these extended temperature cycling experiments, the TTV with the plus-shaped PCM reservoir is subjected to 5000 temperature cycles between 55 °C and 80 °C. Selected cycles are shown here from the tenth cycle in dark blue through cycle 5000 in light blue/cyan. The system remains stable throughout all 5000 cycles, suggesting that the metallic PCM embedded in a silicon device can consistently outperform an all-silicon device provided that complete melting/freezing is achieved every cycle.

The overlapping temperature response reveals that the system is stable throughout the 5000 cycles. The PCM consistently undergoes complete melting and freezing, maintaining identical melt and freeze temperatures across all cycles. This observation adds confidence that systems with metallic PCM embedded within silicon device layers will be able to manage transient temperature spikes throughout the system operation lifetime. Moreover, our initial studies highlight a critical requirement for the PCM: for optimal stability, the PCM must undergo full melting and solidifying during each cycle.

IV. Conclusion

This study demonstrates the potential of embedding metallic PCM within an active device layer (here, a silicon chip) for reducing temperatures and temperature oscillations during transient operation of the system. Specifically, these experiments address an issue with previous designs of PCM-laden heat sinks where the thermal resistance between the hot spot and the heat sink make the performance less effective with increasing power levels. Furthermore, this approach addresses spatial constraints within mobile chips by strategically embedding PCM directly within the silicon chip without significantly increasing the device/package dimensions. The experimental approach involved fabricating thermal test vehicles with realistic mobile chip form factors to assess the performance of a device with an embedded PCM thermal buffer. Importantly, this work is among the first to successfully fabricate device with an embedded PCM zone within the chip and validate its performance for realistic power profiles.

The significant improvement in thermal performance with the PCM reservoir demonstrates the efficacy of this thermal management strategy. Specifically, the embedded PCM extends operational time by 2.3$\times$ during temperature cycling compared to an all-silicon benchmark device. Furthermore, during duty cycling, it reduces both the overall maximum temperature by 10% and temperature fluctuations by 47%. This enhanced thermal stability is crucial for preventing thermal-induced stress on semiconductor components, thereby contributing to prolonged device lifespan and reliability.

A notable finding is the occasionally observed shifts in PCM melt/freeze temperature, that impact the temperatures of the device, and occur when incomplete melting and/or solidification occurs during duty cycling. However, extended operational testing with temperature cycling (for 5000 cycles, with a run time of $\sim$21 hours) showcases the stability of the embedded PCM when complete melting and freezing is achieved during every cycle. The results highlight the critical importance of ensuring complete phase transitions for the prolonged and reliable functionality of PCM-based thermal management systems.

Future research should delve into exploring different duty cycle times and varied PCM distributions to refine the optimization of an embedded PCM thermal management approach. Additionally, investigating the root causes behind PCM degradation will be important in ensuring robustness of embedded PCM systems. In conclusion, this study establishes a novel methodology for integrating PCM within a silicon device and also lays the groundwork for continued advancements in PCM-based thermal management of microelectronics.

Acknowledgment

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