

The absence of specified acceptance criteria for evaluating commercial off-the-shelf circuit card assemblies (CCAs) leads to a vital absence of quality control in the otherwise robust production of embedded systems technologies. To address the needs of our stakeholders, NSWC Crane and Purdue University's School of Materials Engineering, our goal is to establish comprehensive acceptance criteria integrating industry standards and proprietary visual and microscopic inspection techniques. This aims to integrate a consistent and reliable identification of viable commercial off-the-shelf circuit card assemblies into the production pipeline, crucial for ensuring reliability and performance.

This work is sponsored by Naval Surface Warfare Center, Crane, IN

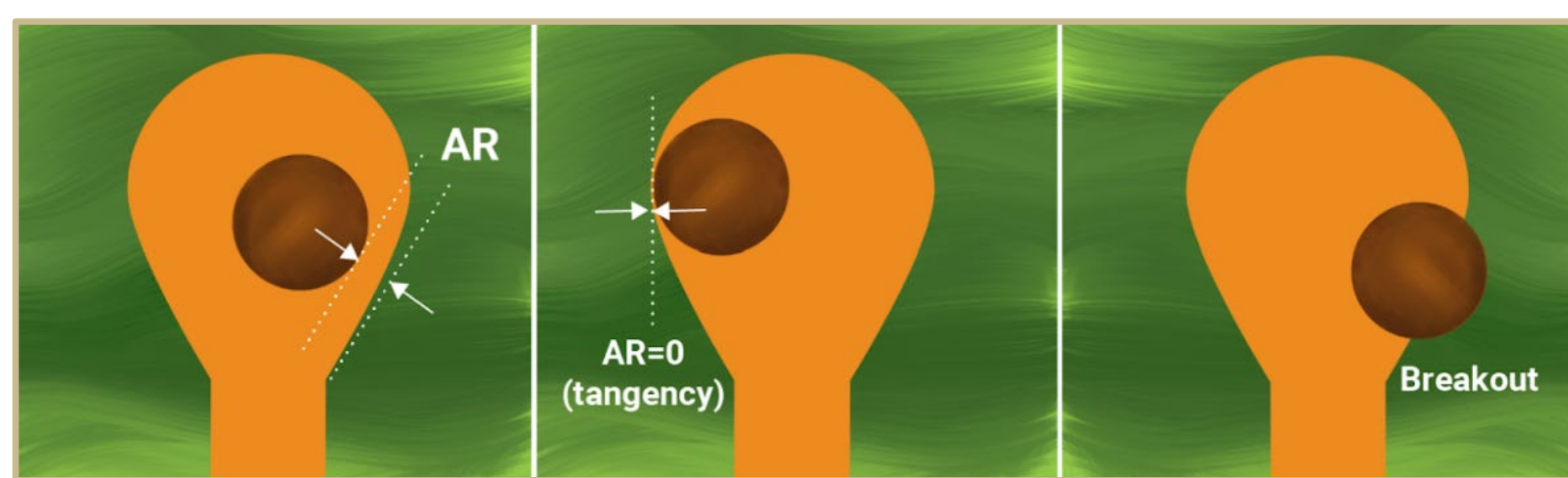


## Background & Objectives

### CCAs in the Naval Defense Industry

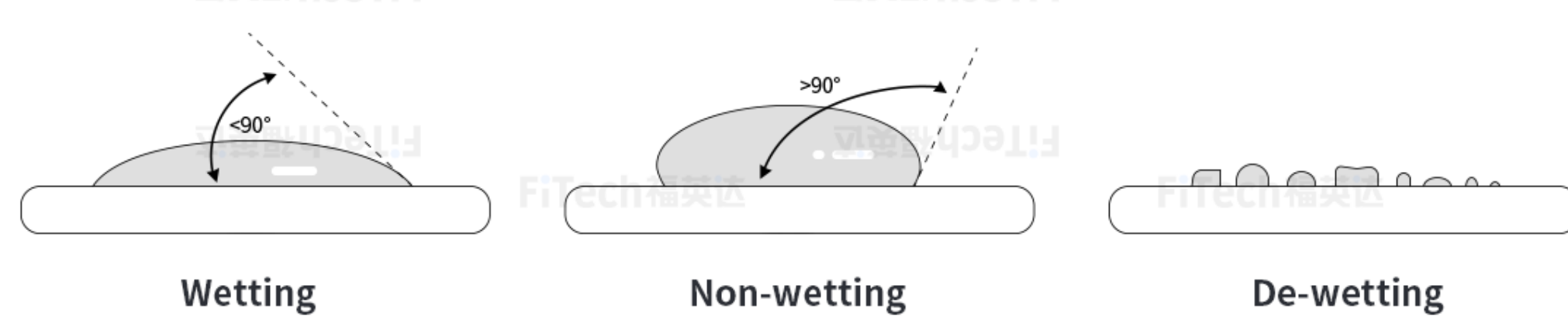
- In naval defense, CCAs are instrumental in communication, navigation, surveillance, and weapon control in military technologies
- CCA failure can cause catastrophic failure in mission-critical environments, underscoring the importance of quality guarantees
- Counterfeit components made with improper methods or scrap materials from e-waste are common, and can lead to higher risk of failure due to the proper scrutiny and standards not being applied
- Regulations such as IPC standards are commonly used to ensure reliability between nodes in the supply chain

### Failure Modes



### Inadequate Annular Ring<sup>1</sup>

- Due to lack of tool calibration or mechanical and thermal warping
- Leads to poor electrical connection or misalignment of components



### Solder Adherence Issues<sup>2</sup>

- Solder doesn't properly adhere to the board or lead
- Caused by contaminants on pad, insufficient soaking time or inadequate heating during solder reflow, or poor surface finish

### Purpose of Project

- Analyze e-waste and determine potential failure mechanisms
- Establish a comprehensive acceptance criteria for assessing CCAs
- Gain extensive knowledge of IPC standards and their use cases

## Methods & Materials

### Sample Prep

The circuit boards were sectioned with an abrasive saw. This was done to isolate components of the board and minimize the size of the samples for easier microscopy analysis.

### Optical Analysis

Optical analysis was performed using a stereoscope to quickly assess the features on the board, as well as any defects that are conspicuous. Solder joints, integrated circuit packages, conformal coatings, and conductive traces were among some features analyzed.

### Scanning Electron Microscopy (SEM)

SEM was performed on sectioned pieces of the Arduino. Areas of interest were identified by both literature and optical microscopy. Due to the size and shape of the sections, they needed to be propped up in the sample holder with a small cap and clay to allow for a more accurate focus.

### Energy Dispersive Spectroscopy (EDS)

EDS was performed on areas of interest found during SEM. This method generated semi-quantitative results of which elements were present in each board displayed in maps and spectra.

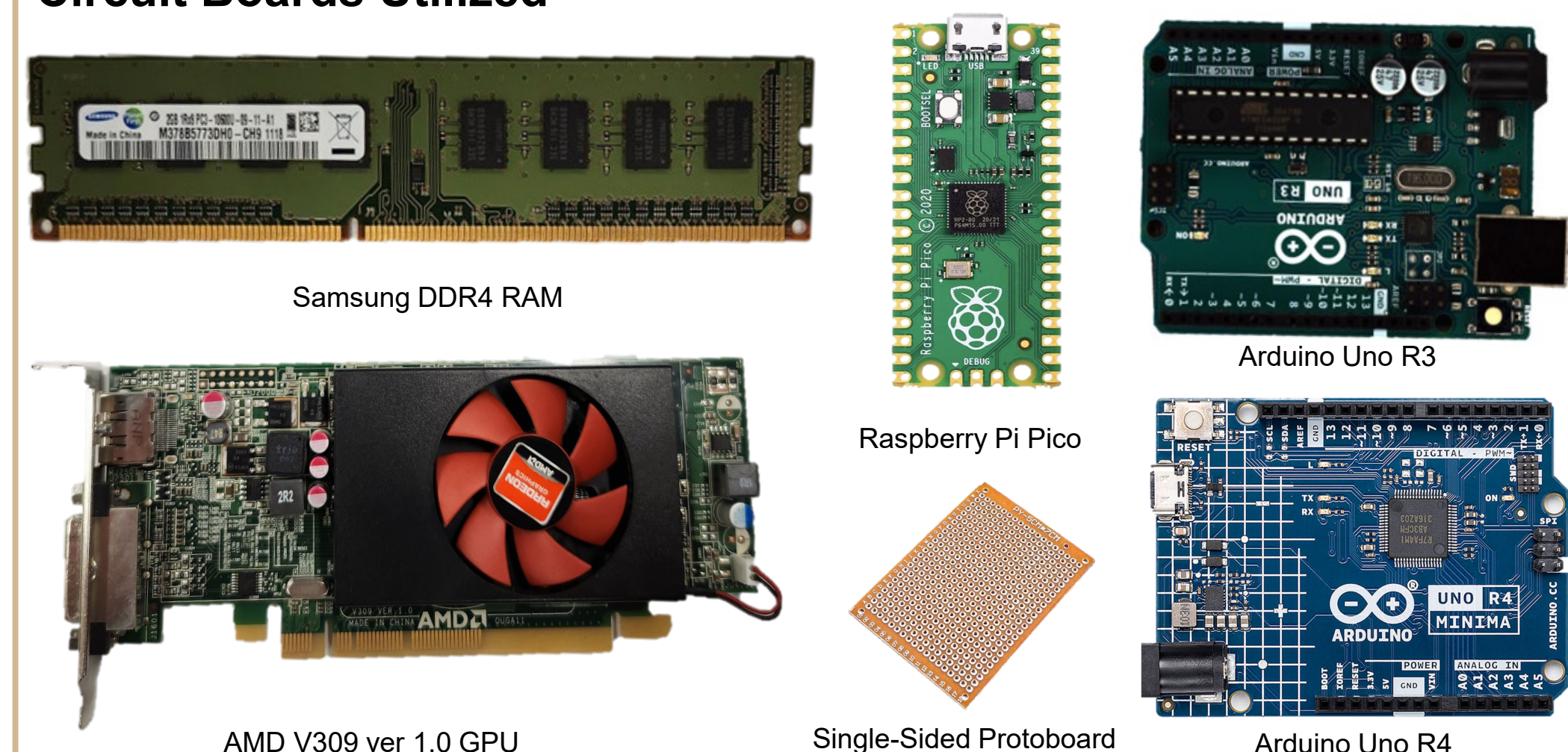
### X-Ray Fluorescence (XRF)

XRF was performed to gather an elemental analysis of boards which primarily focused on determining the solder content and inspecting defects.

### Computed Tomography (CT)

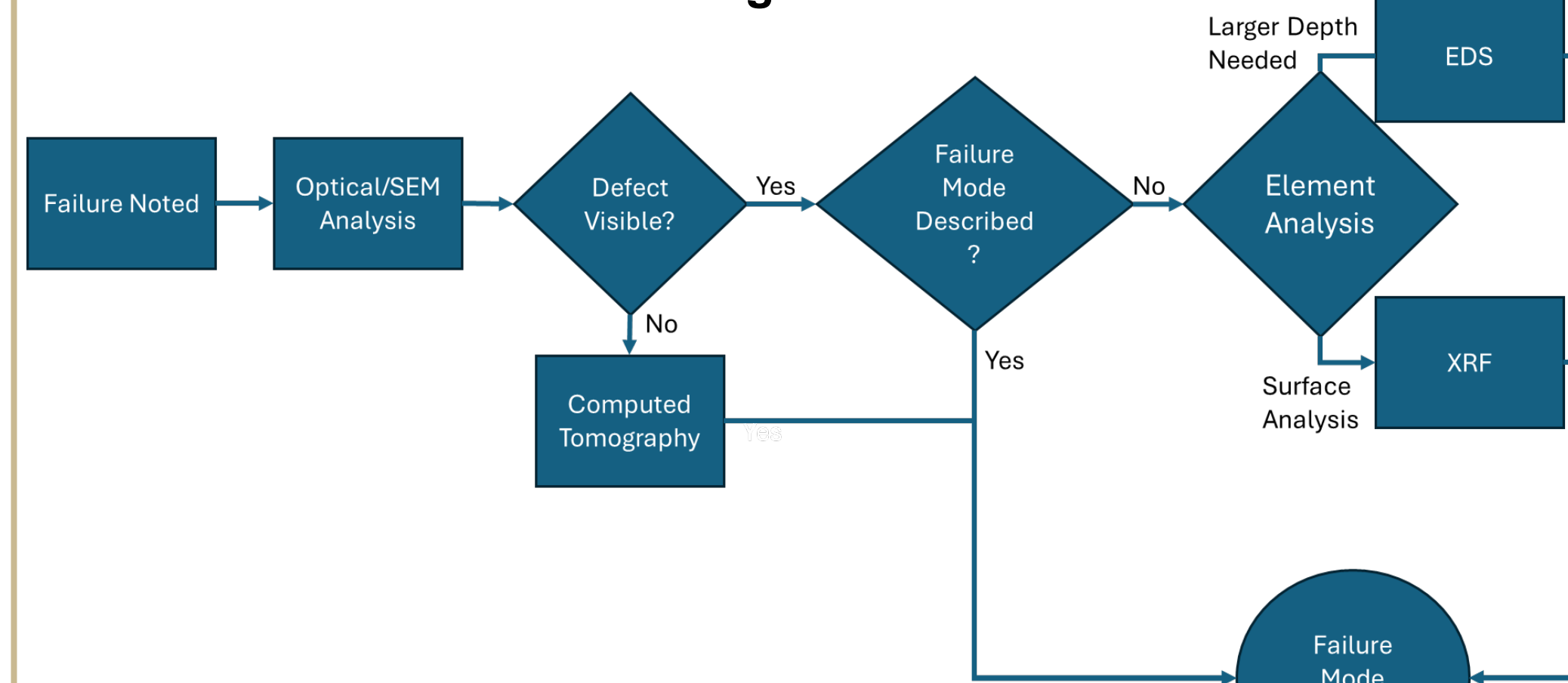
CT is a non-destructive scan that utilizes X-rays to generate a 3D image of a board, highlighting the conductive pathways between and within board constituents.

### Circuit Boards Utilized



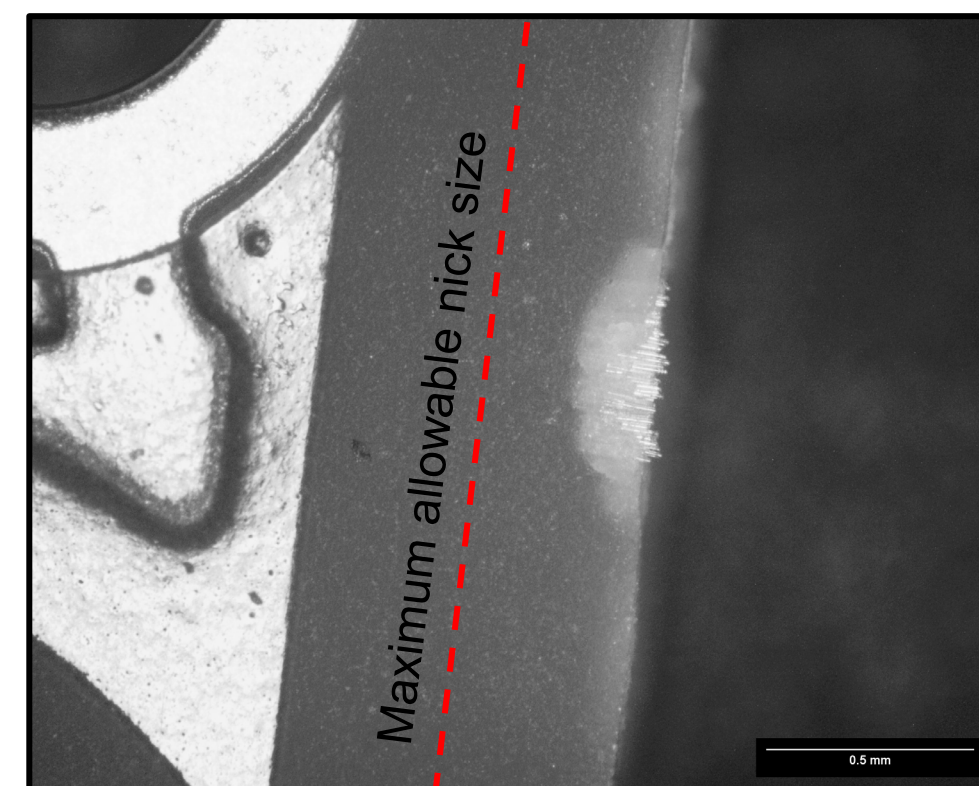
## Results & Discussion

### Defect Investigation Flowchart



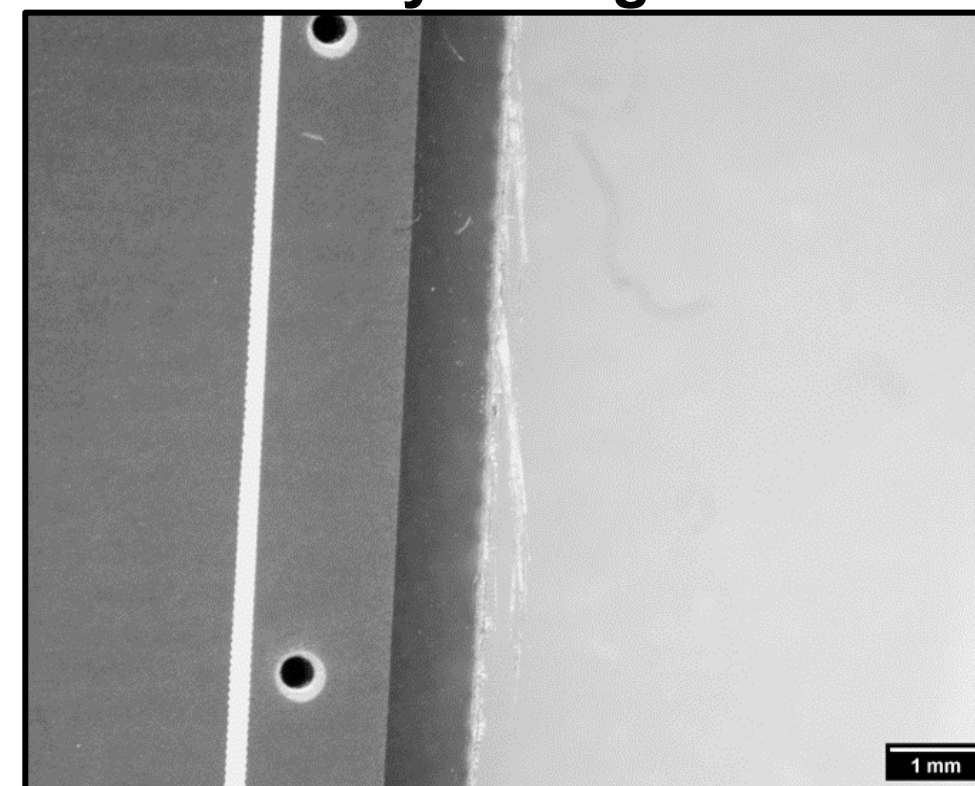
### Investigation Procedure Resulting From Defect Analysis

#### Nicks



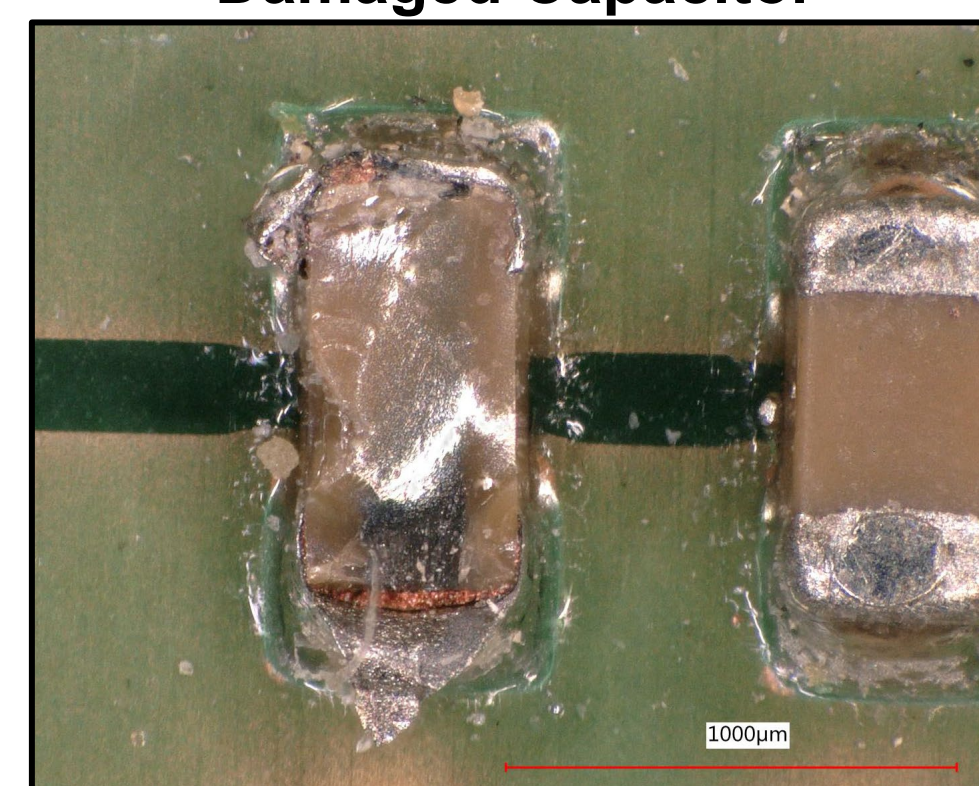
Repetitive nicks were discovered along the edges likely originating from the separation of the boards. These are permissible if they do not extend beyond 50% of the distance to the nearest conductor or exceed 2.5 mm. This occurrence **conforms** to IPC standards<sup>3</sup>.

#### Frayed Edges



The rough edges likely stem from the cutting of the board to size. Edges should be smooth without any burrs; however, rough edges are acceptable given any loose burrs do not impede fit or functionality. Therefore, this instance of fraying **conforms** to IPC standards<sup>3</sup>.

#### Damaged Capacitor



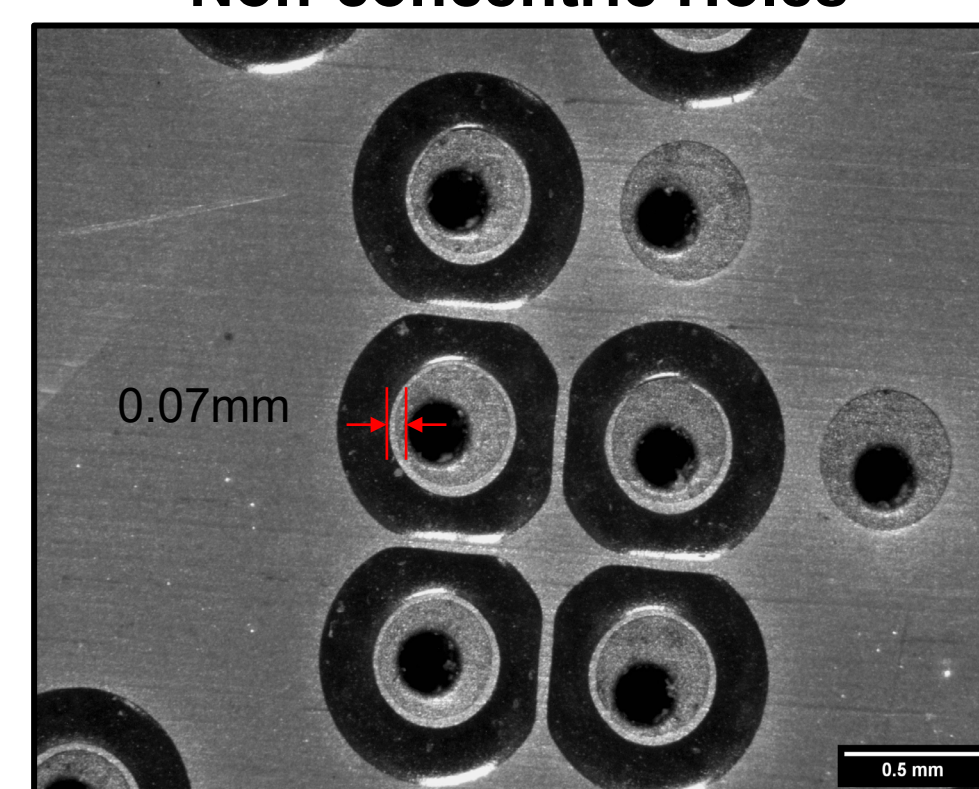
This capacitor likely suffered an impact. Due to the shearing of the conformal coating, this likely occurred during handling rather than fabrication. The damage could affect the component's functionality and would **not conform** to IPC standards<sup>3</sup>.

#### Contaminated Connection



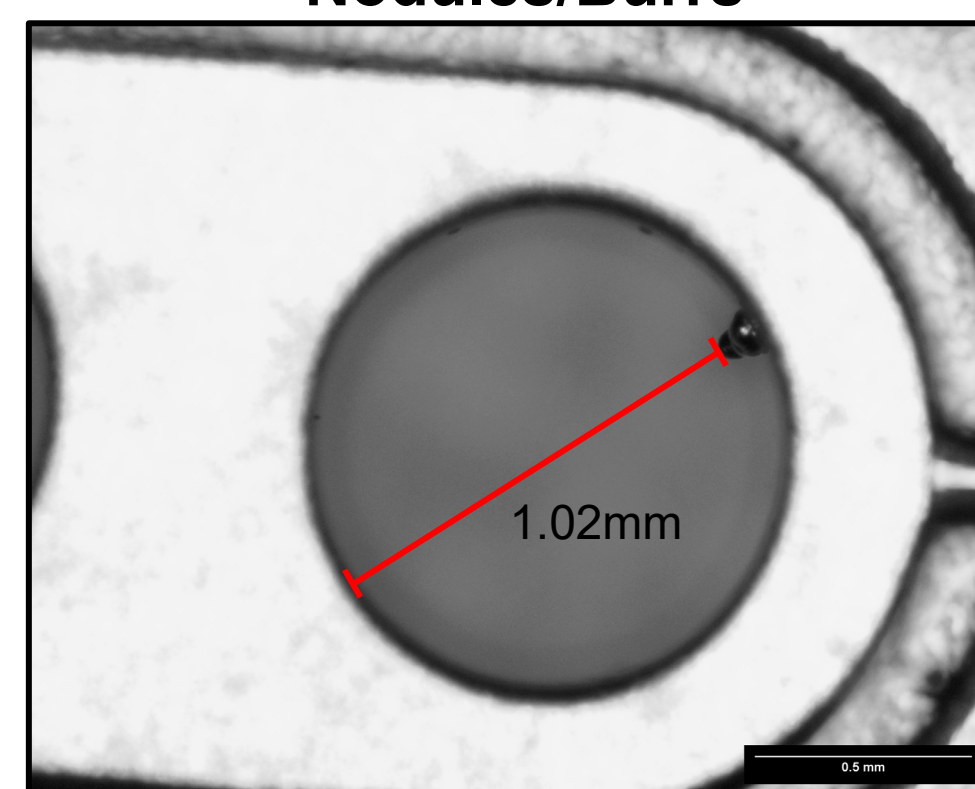
Contamination threatens device functionality. From visual inspection, this solder joint is likely to be **nonconforming**. The degree of nonconformance could be quantified by measuring the ionic conductivity of the contaminants<sup>4</sup>.

#### Non-concentric Holes



Non-centered holes are a byproduct of the alignment variability during manufacturing. Such occurrences are deemed acceptable given the annular ring a minimum of 0.050mm. These holes **conform** to IPC standards<sup>3</sup>.

#### Nodules/Burrs



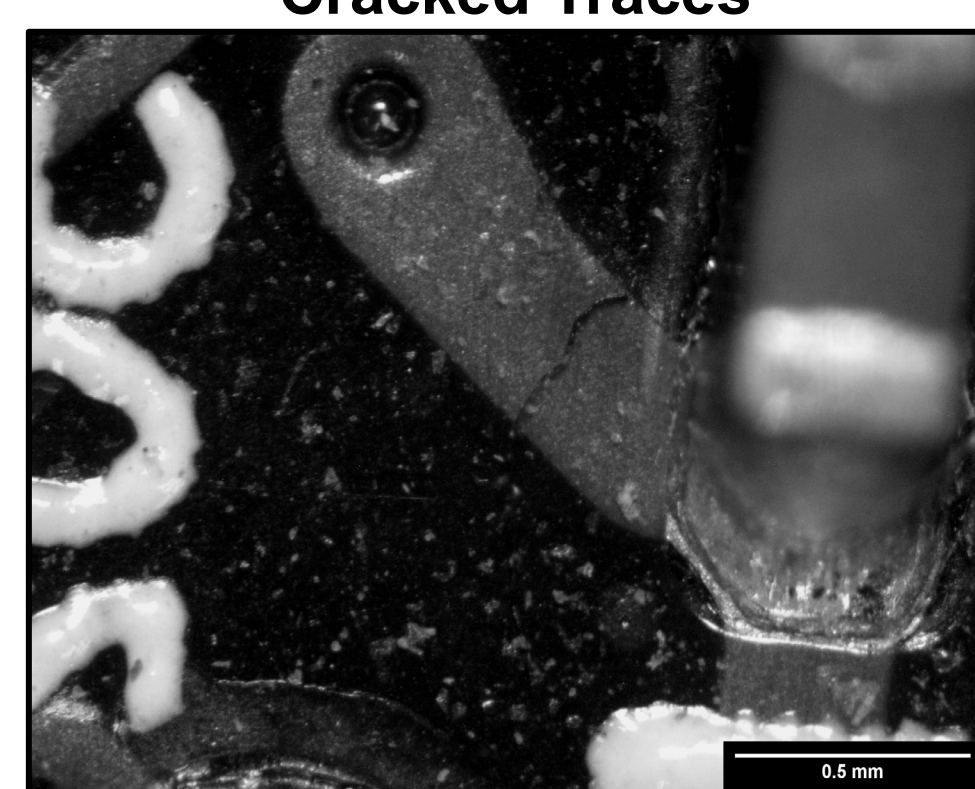
For plated through holes, the target condition is no nodules or burrs. The presence of nodules in this case still **conforms** to IPC standards<sup>3</sup>, as the minimum finished hole diameter is still met.

#### Burn Mark



This burn was likely caused by a soldering iron during a manual touchup in fabrication. XRF analysis revealed elevated levels of copper, indicative of the erosion of the solder mask, thereby exposing the underlying plane. However, as no adjacent conductive patterns have been exposed, this defect is permissible, and **conforms** to IPC standards<sup>3</sup>.

#### Cracked Traces

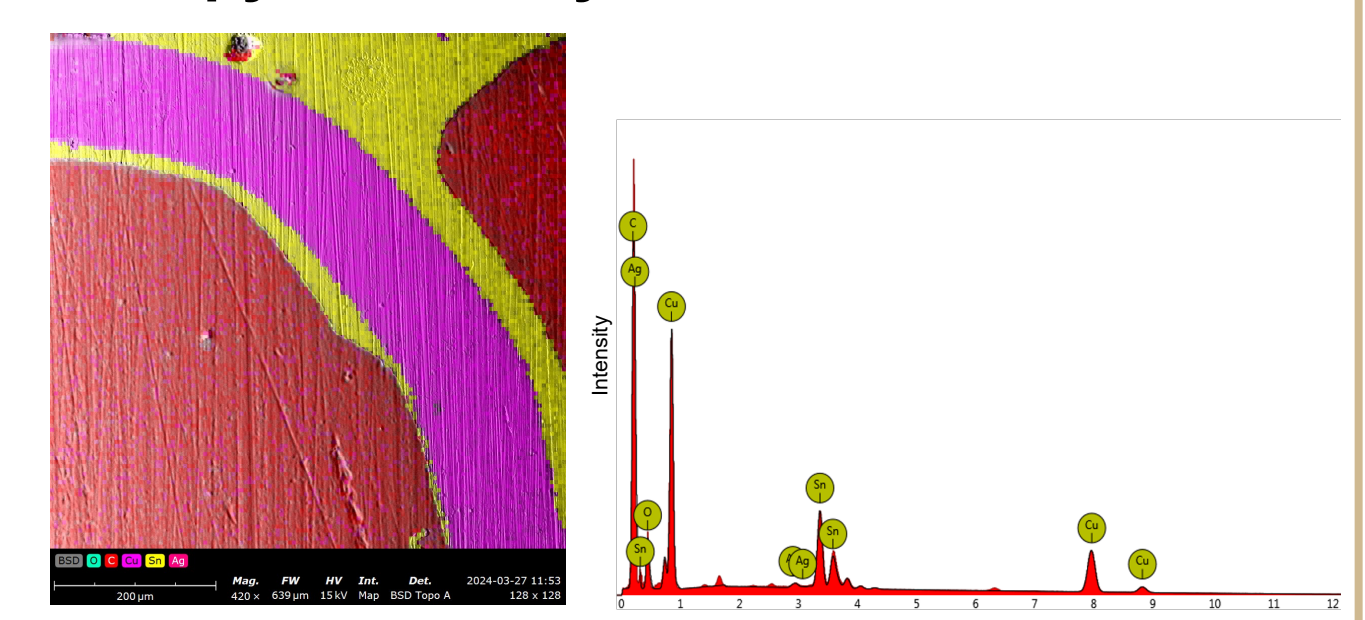


The presence of this crack is **nonconforming** to IPC standards<sup>3</sup> as it severs a trace, disrupting the flow of electrical signals along the intended path. This crack was likely a result of mechanical stress during assembly or handling. Inadequate curing or adhesion could also leave the board susceptible to these kinds of cracks.

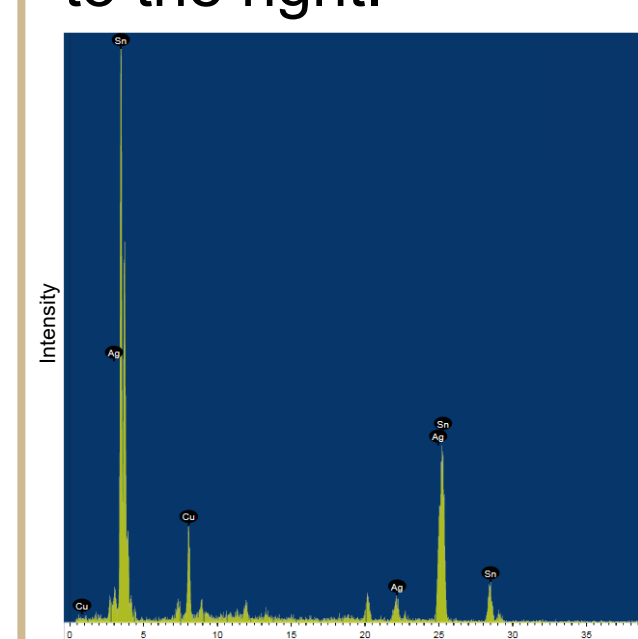
## Results & Discussion

### Energy Dispersive Spectroscopy and X-Ray Fluorescence

EDS can elementally analyze specified area of interest, such as a cross section of a solder joint. EDS can provide both image identification and spectra, as pictured to the right.



EDS elemental map of a solder joint on the Arduino Uno R4

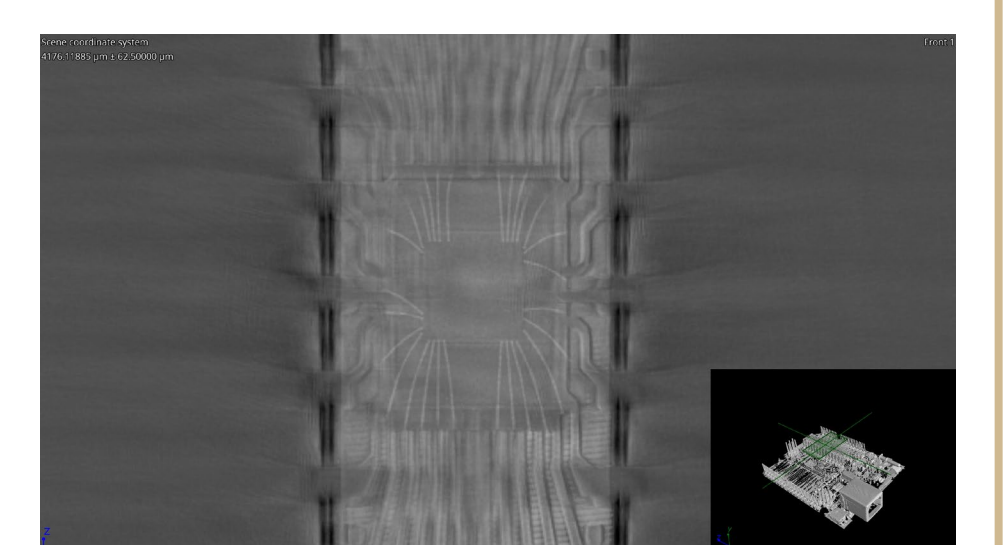


XRF spectra from GPU solder joint

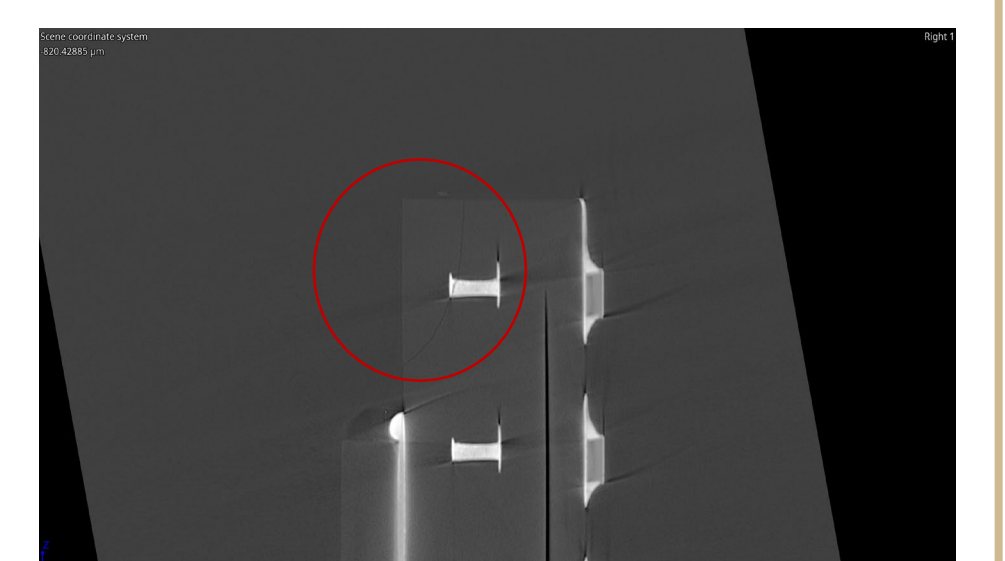
Similarly, XRF can be utilized for elemental analysis, including for solder joints. When used on the GPU, XRF exhibited high amounts of tin, small amounts of silver and copper, and no lead content. This can be useful in identifying solder type, likely SAC305 in this case, but it can also be used to identify impurities. EDS and XRF are both used in circuit card analysis given their differences in sensitivity and penetration depth.

### Computed Tomography (CT) X-Ray

CT X-Ray serves as a non-destructive testing method offering insights beyond optical inspection. It enables the isolation of conductive pathways by filtering out non-conductive material, facilitating examination inside component packaging. As illustrated by the cross-sectioned Arduino board to the top right, X-Ray CT allows inspection of the internal wiring of components like the microcontroller IC. While the Arduino exhibited no failures, X-Ray CT is invaluable for detecting internal failures such as the crack visible in the component to the bottom right, which went undetected through optical inspection despite the board's malfunction.



CT Scan of an Arduino Uno R3 circuit board



Example of an internal fracture found through CT X-ray

## Conclusions & Future Work

With the increasing complexity of printed circuit boards, establishing acceptance criteria becomes imperative to ensure their capability to fulfill intended tasks, particularly in long-service-life equipment for defense applications. Adhering to IPC standards enabled the team to identify common defects and develop a systematic process for assessing a board's integrity. While optical inspection suffices for detecting most circuit board defects leading to nonconformance, Non-Destructive Testing methods offer heightened accuracy and risk reduction, although they involve more demanding processes.

Looking ahead, a more comprehensive procedure could incorporate additional methods such as Raman spectroscopy, scanning acoustic microscopy, or contaminant analysis via resistivity testing. Moreover, training AI models to flag nonconformance to existing acceptance criteria promises more precise assessments of circuit assemblies. Ultimately, given the criticality of defense products ensuring absolute confidence in the function of each circuit assembly remains paramount and the implementation and enhancement of acceptance criteria facilitates this.

## References

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## Acknowledgements

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