Advanced 3D Integrated Packaging: Manufacturing and Reliability

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High bandwidth memory chips were used to investigate the reliability of advanced 3D integrated packaging for NSWC Crane. The chips were annealed at 125ºC for 5, 10, and 15 weeks. The microbumps were imaged to measure IMC thickness, and a plot of IMC thickness over time was generated. It was found that industry criteria for resistance failure was reached in 5 weeks. Due to lab shutdowns, the effect of thermomechanical stresses on microbumps and TSVs was inconclusive off of data alone. Therefore, expansive literature compilation was created. As a consensus of the FEA and annealing papers about 3D packaging, it was shown that TSVs plastically deform when annealed from 25ºC to 450ºC, as well as create high stress concentrations in silicon.

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Project Background

Advanced 3D integrated packaging is a type of electronic architecture used in modern processing units to increase performance by shortening signal distance via stacked dies. With a greater density of electrically active material comes a greater concern for thermally dependent reliability. One recurrent concern present in all packaging technologies is intermetallic growth (IMC) in solder joints. Figure 1 shows the typical material found in these joints.

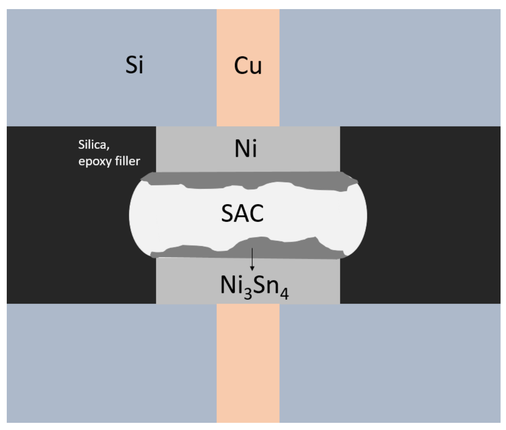


Figure 1: Schematic of microbump solder joint showing materials involved

Due to the materials involved, and the temperature required for bonding, a thin layer of Ni_3Sn_4 intermetallic will form during manufacturing. Furthermore, diffusion of tin to the nickel interface will continue to thicken the IMC layer throughout the component lifetime. Since the IMC has a higher resistance than the solder[1], too much IMC growth could make the component unreliable. A common industry standard is that a 20% resistance increase from the as-manufactured value constitutes failure of the part. Another concern for advanced 3D packaging is thermomechanical stress induced deformation, which may occur because of the large CTE mismatch between materials, Table 1.

Table 1: Thermal expansion coefficients and resistivity of common interconnect materials

Material	CTE (10^{-6}/K)	Resistivity (μΩ*cm)
SAC	21.6	13
Ni_3Sn_4	13.7	28.5
Cu	16.6	-
Si	3	-

Experimental Procedure

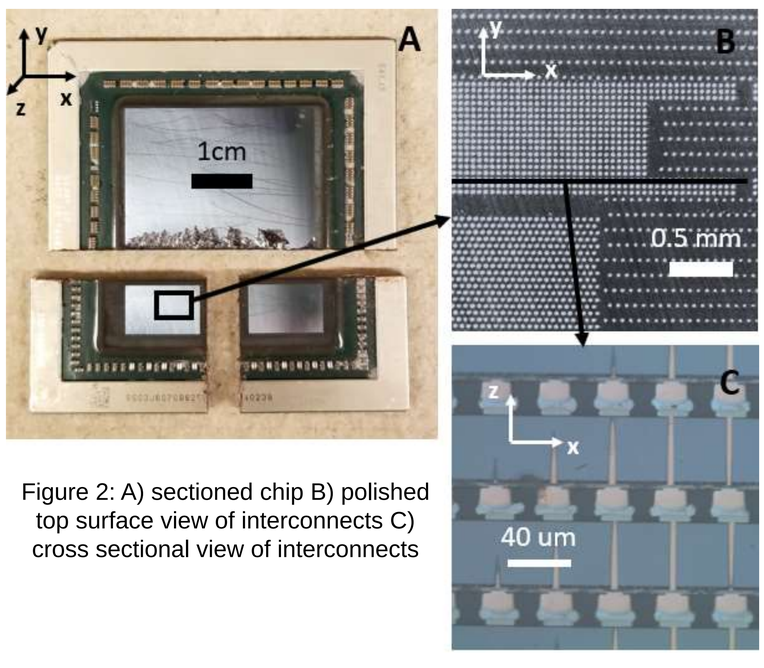
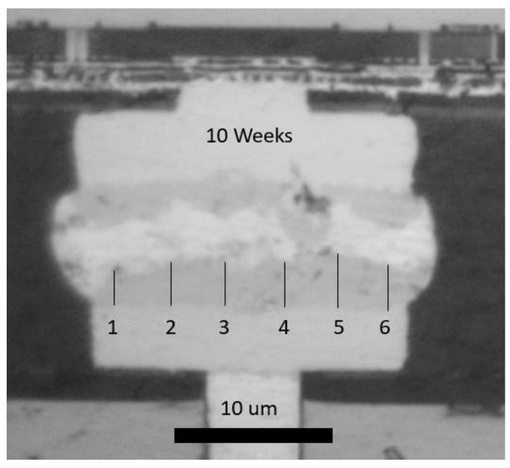


Figure 2: A) sectioned chip B) polished top surface view of interconnects C) cross sectional view of interconnects

To test reliability concerns of advanced 3D integrated packaging, the AMD Radeon RX Vega GPU was observed. The structure of this package is shown in figure 2. Images of the electrical interconnects were taken as manufactured, as well as at 5, 10, and 15 week annealing intervals at 125ºC. IMC length at each anneal period was measured by line averaging using ImageJ, as shown in figure 3.



Line	Length (μm)
1	3.19
2	3.22
3	4.79
4	4.93
5	5.14
6	4.36

Avg. Length = 4.27 um

Std. Dev. = 0.8 um

Figure 3: Process of averaging IMC length using example of 10-week annealed sample

Results

It was found that the electrically active area of each DRAM die consists of 4062 interconnects. The thickness of each interconnect is made of 5 μm of SAC solder, and 2 μm of the intermetallic phase Ni3Sn4. The area of the interconnect is 314 μm^2 , the Ni3Sn4 resistivity is 28.5 μΩ*cm, and the SAC resistivity is 12.3 μΩ*cm. Using the simple series and parallel resistor equations, and assuming that all of the interconnects are active at once, a total IMC growth of just 1 μm would lead to a 20% increase in overall component resistance. After averaging the IMC thicknesses from all annealed samples, Figure 4 was generated to show thickness over time. At 125ºC, it takes just 5 weeks to reach the criteria for failure.

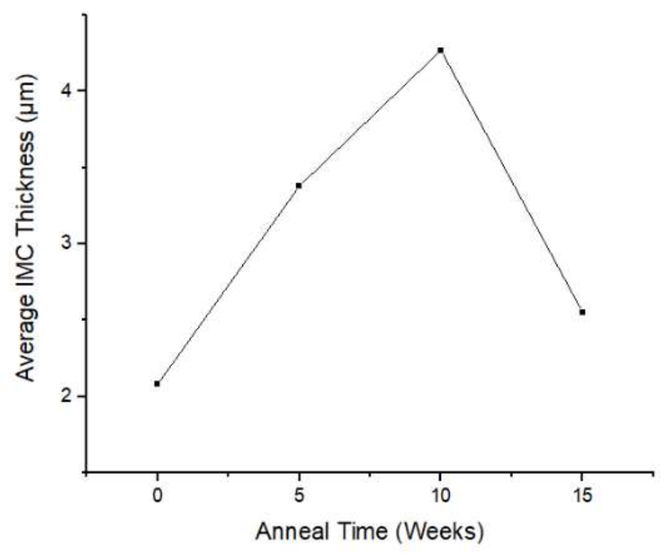


Figure 4: Graph of average IMC thickness at 5, 10, and 15 week anneal at 125ºC

TSV deformation was not observed, however there are many papers on the subject indicating what TSV failure might look like. TSV failure occurs in specific vulnerable areas, due to stresses that come from thermal expansion of copper in silicon as shown in Table 1. One vulnerable area is the growth seam, which is a seam created when copper deposits from the walls to the middle of the via during manufacturing. Another vulnerable area is the area in which the TSV connects to the copper pillar.

Figure 5: 2D stress modeling of solder joints from literature

Figure 5 shows an example of solder joints in a finite element 2D model. This model is used to show the basic geometry of the solder joint as well as where stress may occur based thermal expansion mismatch. Stresses should be in the area where IMC growth occurs.

Discussion

Figure 4 shows an increase in IMC growth from 0 to 10 weeks which is an expected trend as the intermetallic faces undergo transient diffusion during aging. After just 5 weeks of aging, the IMC grew enough to increase resistance of the chip by 20%, which is an industry benchmark for reliability failure. The drop in IMC growth in the 15-week aged sample is irregular. This anomalous data is due to differing GPU architecture that went unnoticed in the early stages of the experiment. While the 0 to 10 week interconnects appeared as in Figrue 1 and 3, the week 15 interconnects appeared as in Figure 2. That is, the 15 week sample contained a large copper bond pad at the top of the interconnect instead of a thinner nickel pad. Although this was not desirable for creating a consistent trend, it could still be something useful to take note of. For example, this result means that using copper as the bonding surface could reduce the amount of IMC growth, thereby increasing the performance of the chip.

The thermal stress and TSV literature gives an abundance of stress ditribution maps and pictures of deformed TSVs, however there is no definite lifetime prediction framework for these types of chips. If long term reliability is a concern, the best information on TSVs says to be wary.

Recommendations

Although the COVID-19 pandemic discontinued plans to take more images of the annealed chips, some conclusions have been made. First, the resistance increase of stacked dies due to IMC growth could pose a problem to long term performance. This would most likely only present a problem when dealing with high operating loads over long periods. Second, the presence of TSVs could also reduce the chip lifetime. All of the literature concludes that at elevated temperatures thermal expansion of copper creates stress concentrations in silicon. There are also reports of TSV deformation. Since TSV technology is still young, it might be wise to wait some time for more conclusive data to come out before using in military applications. Future work on this topic might include varying anneal temperature and time.