Three-dimensional logic and memory devices are increasing in popularity due to increases in computational power while minimizing space. However, this change in structure plays into the question of reliability of the solder joints within each layer of the device. This project seeks to explore the effects of various extended use regimes on small 3D solder joints. Intermetallic compound (IMC) growth is measured after thermal aging and the relative damage in the solder joint is assessed to provide a better qualitative and quantitative measure of the joint reliability.

**Project Motivation & Goals**

By stacking layers of logic and memory devices in a 3-Dimensional architecture, systems can utilize less space and increase computation via shorter signal pathways. However, it is relatively unknown how this new architecture will affect the reliability of the solder joints, a vital component. Statistically significant data must be obtained to analyze the response of the solder to different stress states. During fabrication, the tin alloy is refloved to attach each layer, the solder joint on the bottom level has seen 3 more heat cycles than the top level. As the 3D device thermally expands, the solder on the edges will experience a greater overall displacement and resulting in larger forces applied. Thermal aging can be utilized to assess solder damage. 

**Objectives:**

- Measure IMC growth relative to thermal aging
- Analyze damage to solder ball
- Characterize geometric effect to reliability

**Experimental Setup & Procedure**

Three tests were used to thermally age 3D memory chips: high temperature hold (HTH), thermal cycling (TC), and a sequential (SEQ) test of HTH and TC. At each read point, the analysis focused on four sections of the chip, the four sets of Through Silicon Vias (TSVs) and the solder bumps attaching them. The four points of interest consist of 16 solder bump/TSVs each, with the outer two and inner two being equivalent due to axisymmetric geometry. At each point, the solder is analyzed for relative damage and IMC growth. Using BSE SEM imaging, the IMC layers can be determined by contrast across the solder ball, hence, 100% damage (or the damage is measured. The damage exists as necking, large single cracks, and regions of numerous and their thickness measured. Using the same image, width, preventing electronic transport through the solder ball and TSV. Damage, especially cracking, will enable both electrical and mechanical failure of the device. Hence, it is vital to understand the effects of geometry and dimensionality on damage.

**Results & Discussion**

**Solder Ball Composition**

Via EDS scans, the solder ball composition can be confirmed, defining the regions from top to bottom as Cu, Ni, NiSn, IMCs, tin, NiSn, IMCs, Ni, and Cu. More precise scans are necessary to determine the specific IMC compositions.

**Mechanical Damage of the Solder**

By analyzing the mechanical damage in the solder due to cracking and necking, the damage can be mapped to the location of the solder ball. The lowest layers and near the perimeter appear more susceptible to mechanical damage over extended use. This is due to additional tin refloows and increased displacement during thermal cycling.

**Solder Necking Damage**

The nickel present is more than double the necessary size to consume the tin. The ratio minimizing boundaries values from the uncertainty still produce a significantly large ratio. Hence, the IMC regions analyzed in this study should be from the Ni-Sn system, exclusively. Through the thermal tests, the IMC growth was measured on various read points and plotted against a numerical model for constant temperature growth at 150°C fit from an Arrhenius relationship.

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X = X_0 + At^{1/2}e^{-E_A / RT}
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The Ni-Sn system is known to have n value of 0.46 as well as an activation energy of -47.1 kJ/mol. The fitting constant of A was found to have a value of ~19,000. The HTH was expected to have the highest IMC growth rate, followed by SEQ, due to the largest time spent at high temperature. The difference in expected and actual trends shown can possibly be attributed to the large uncertainty in X parameter value from the received samples.

**Summary & Recommendations**

Through damage analysis, it is shown that damage is more likely on solder balls near the edges of the chips and at the lower layers. This is most likely due to both increased displacement fields and multiple refloows of the solder during fabrication. It is recommended that use conditions similar to the sequential testing be avoided to prevent severe damage to the solder.