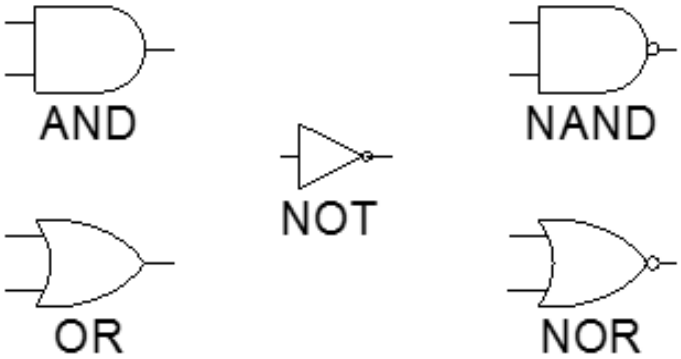
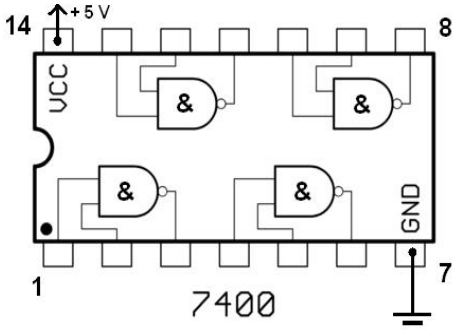
FROM LAST TIME…

Computer Systems

- Implementing Boolean Logic

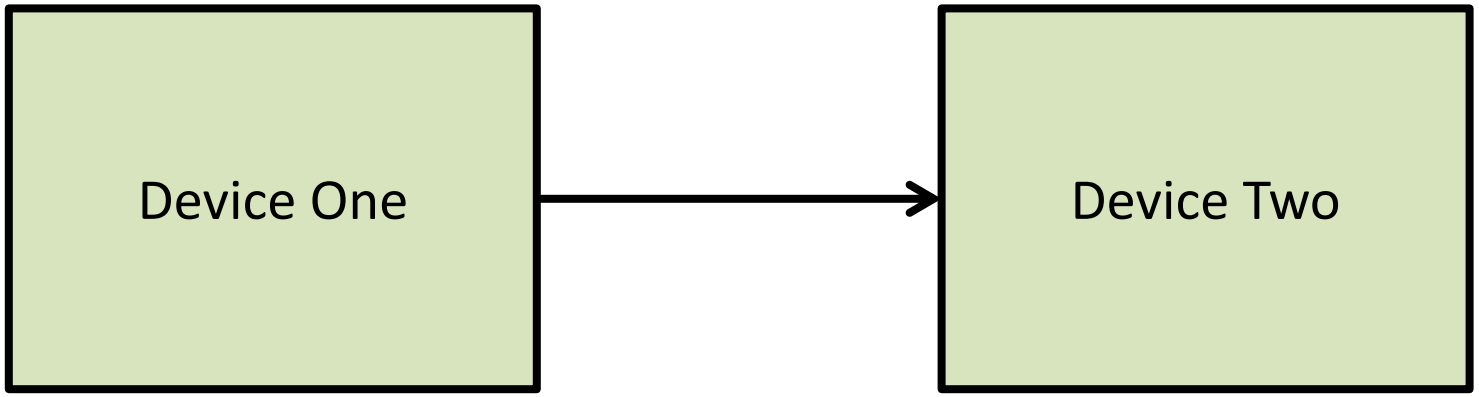




UNIT 3:
COMBINATIONAL LOGIC

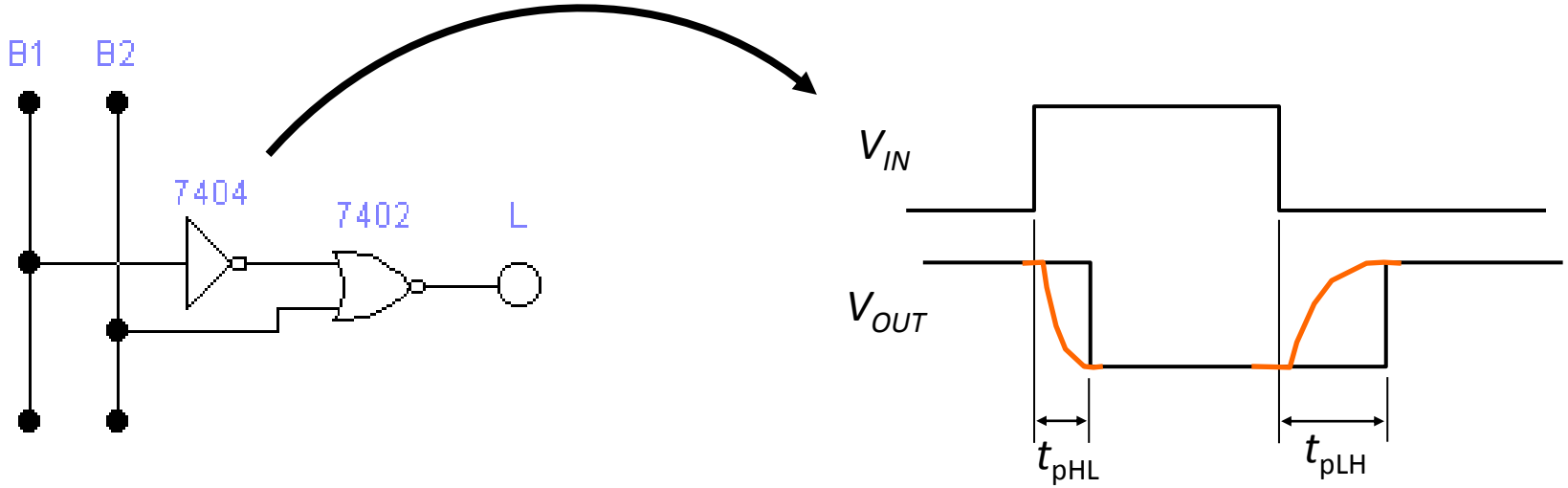
PART D:
DIGITAL INTERFACING

IDEAL DEVICES ARE INSTANTANEOUS AND NOISE-FREE

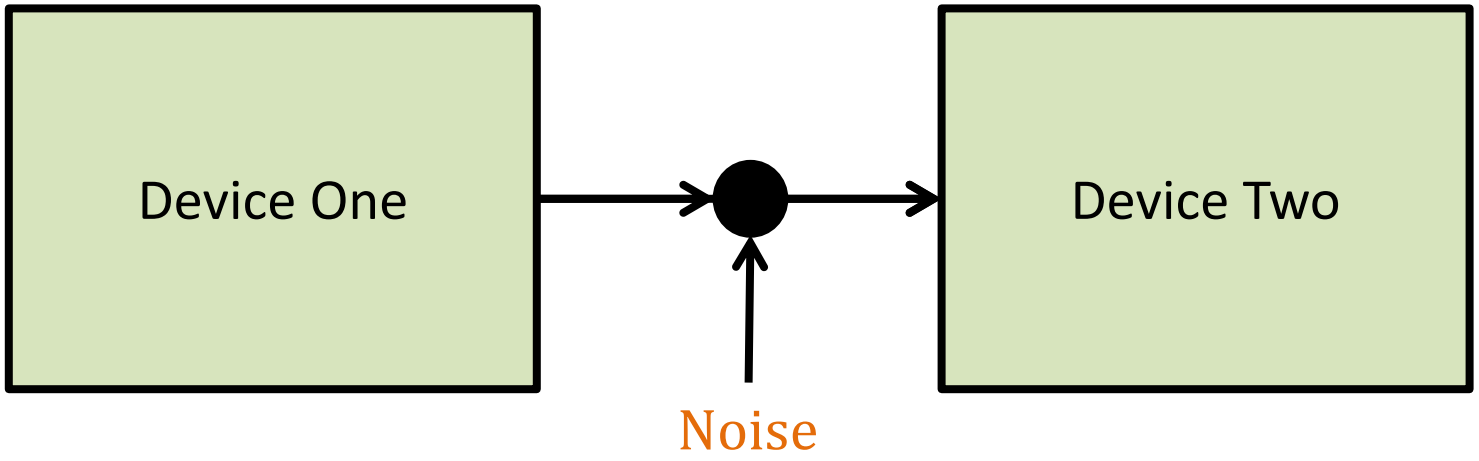


- Device One sends a “0” ⇒ Device Two reads exactly “0”
- Device One sends a “1” ⇒ Device Two reads exactly “1”

REAL DEVICES EXPERIENCE PROPAGATION DELAY

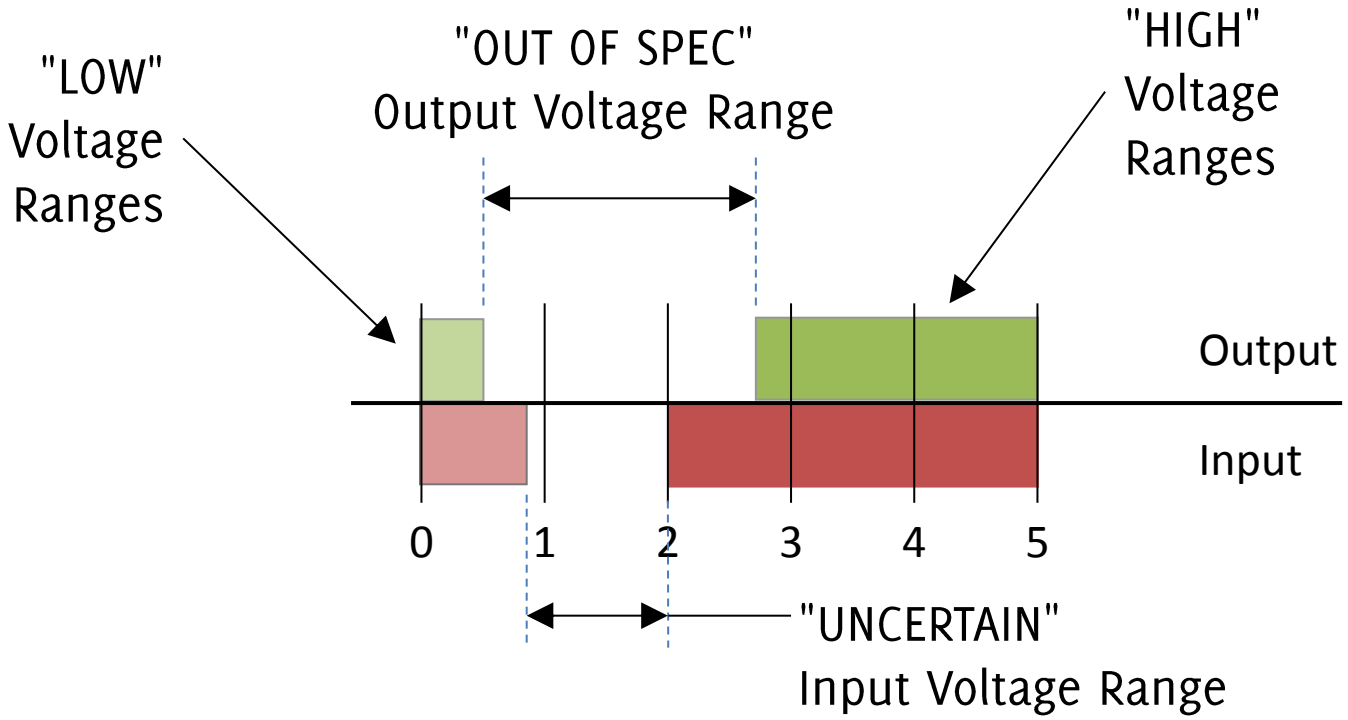


REAL DEVICES EXPERIENCE NOISE



- Device One sends a “0” ⇒ Device Two may read a “0” or “1”
- Device One sends a “1” ⇒ Device Two may read a “1” or “0”

VOLTAGE RANGES DEFINE LOGIC LEVELS FOR “0” AND “1”



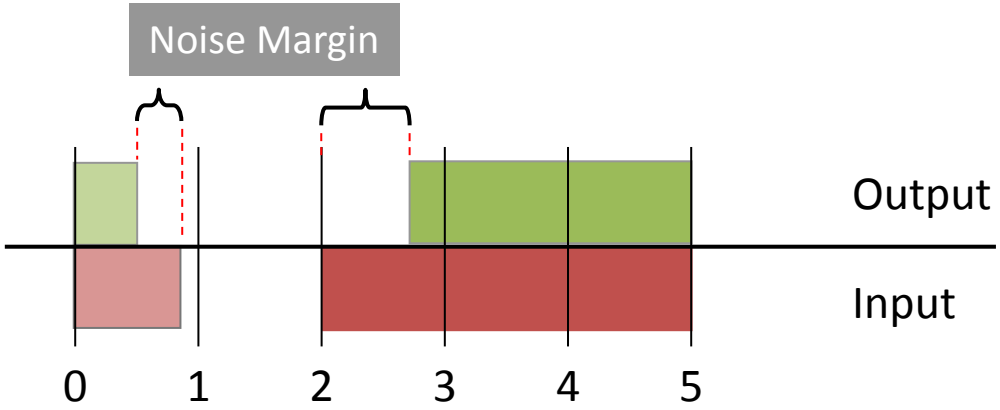
VOLTAGE RANGES DEFINE LOGIC LEVELS FOR "0" AND "1"

Table 2–5 Characteristics of TTL families.

		Family						
Description	Symbol	74	74L	74H	74S	74LS	74AS	74ALS
Typical propagation delay (ns)		9	33	6	3	9	1.6	5
Power consumption per gate (mW)		10	1	22	20	2	20	1.3
Speed-power product (pJ)		90	33	132	60	18	32	6.5
LOW-level input voltage (V)	V_{ILmax}	0.8	0.7	0.8	0.8	0.8	0.8	0.8
LOW-level output voltage (V)	V_{OLmax}	0.4	0.4	0.4	0.5	0.5	0.5	0.5
HIGH-level input voltage (V)	V_{IHmin}	2.0	2.0	2.0	2.0	2.0	2.0	2.0
HIGH-level output voltage (V)	V_{OHmin}	2.4	2.4	2.4	2.7	2.7	2.7	2.7
LOW-level input current (mA)	I_{ILmax}	−1.6	−0.18	−2.0	−2.0	−0.4	−2.0	−0.2
LOW-level output current (mA)	I_{OLmax}	16	3.6	20	20	8	20	8
HIGH-level input current (μA)	I_{IHmax}	40	10	50	50	20	200	20
HIGH-level output current (μA)	I_{OHmax}	−400	−200	−500	−1000	−400	−2000	−400

NOISE MARGIN IS THE PEAK ALLOWABLE VOLTAGE VARIABILITY

- Binary 0: Max. Output < Max. Input
- Binary 1: Min. Output > Min. Input



NOISE MARGINS VARY WITH DEVICE FAMILY

Family	Guaranteed Voltages				Noise Margin	
	V_{IH}	V_{OH}	V_{IL}	V_{OL}	High (1)	Low (0)
74 TTL	2.0	2.4	0.8	0.4	0.4	0.4
74LS TTL	2.0	2.7	0.8	0.5	0.7	0.3
74ALS TTL	2.0	2.7	0.8	0.5	0.7	0.3
74F TTL (Fast)	2.0	2.7	0.8	0.5	0.7	0.3
Hi-Speed CMOS	3.5	4.9	1.0	0.1	1.4	0.9

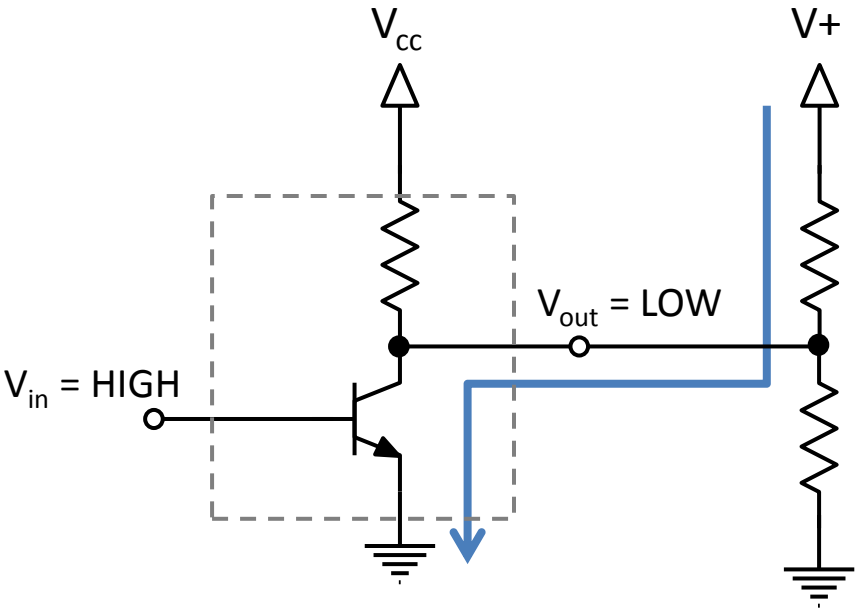
FAN-OUT AND FAN-IN

Fan-In – maximum number of inputs a logic gate can accept

Fan-Out – the maximum number of gate inputs a gate output can drive before logic levels are degraded beyond worst-case specifications

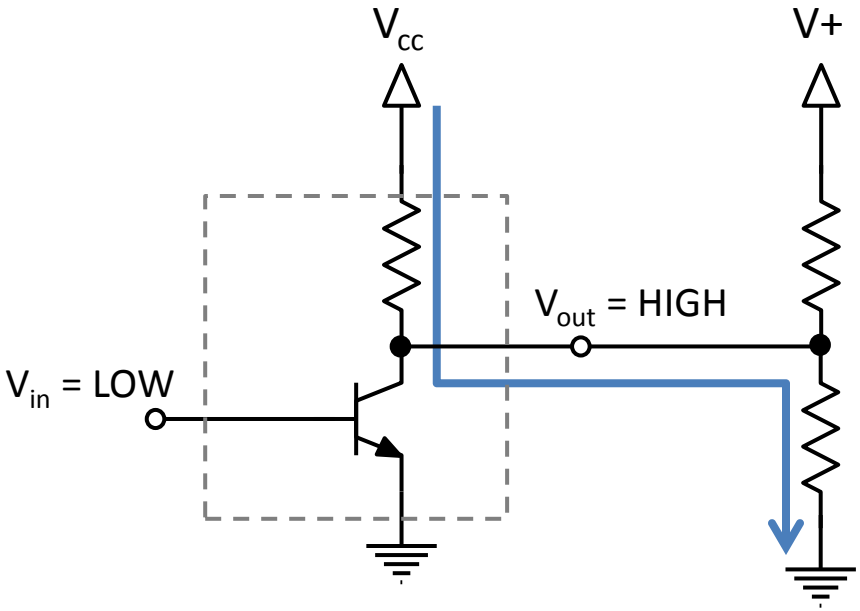
- Normally limited by current constraints
- TTL devices have a fan-out of between 2 and 10 other TTL devices of the same type
- CMOS devices have a typical DC fan-out of 50 other CMOS devices.

DC SINKS AND SOURCES



"Sinking" Output

Provides a path to ground

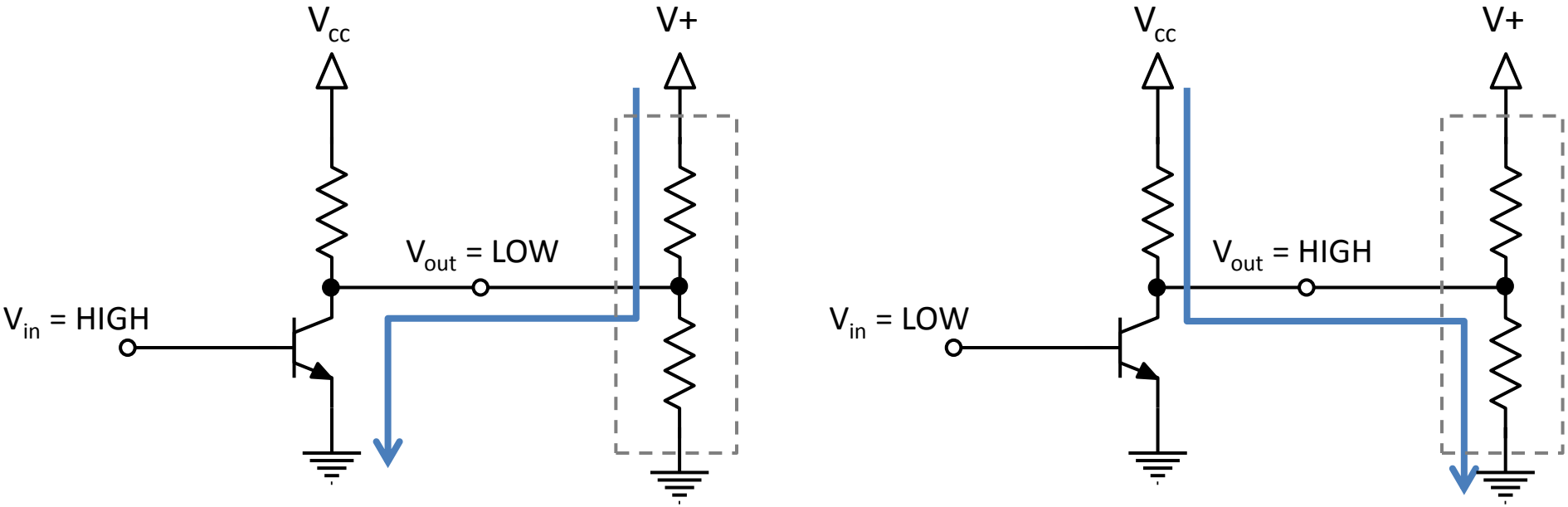


"Sourcing" Output

Provides a path from voltage source

Devices often have unequal capacities for sinking and sourcing current

DC SINKS AND SOURCES



"Sourcing" Input

Provides a path from voltage source

"Sinking" Input

Provides a path to ground

Sinking and sourcing of current is a device-specific phenomenon

ELECTRONIC LOGIC

Table 2–5 Characteristics of TTL families.

Description	Symbol	Family						
		74	74L	74H	74S	74LS	74AS	74ALS
Typical propagation delay (ns)		9	33	6	3	9	1.6	5
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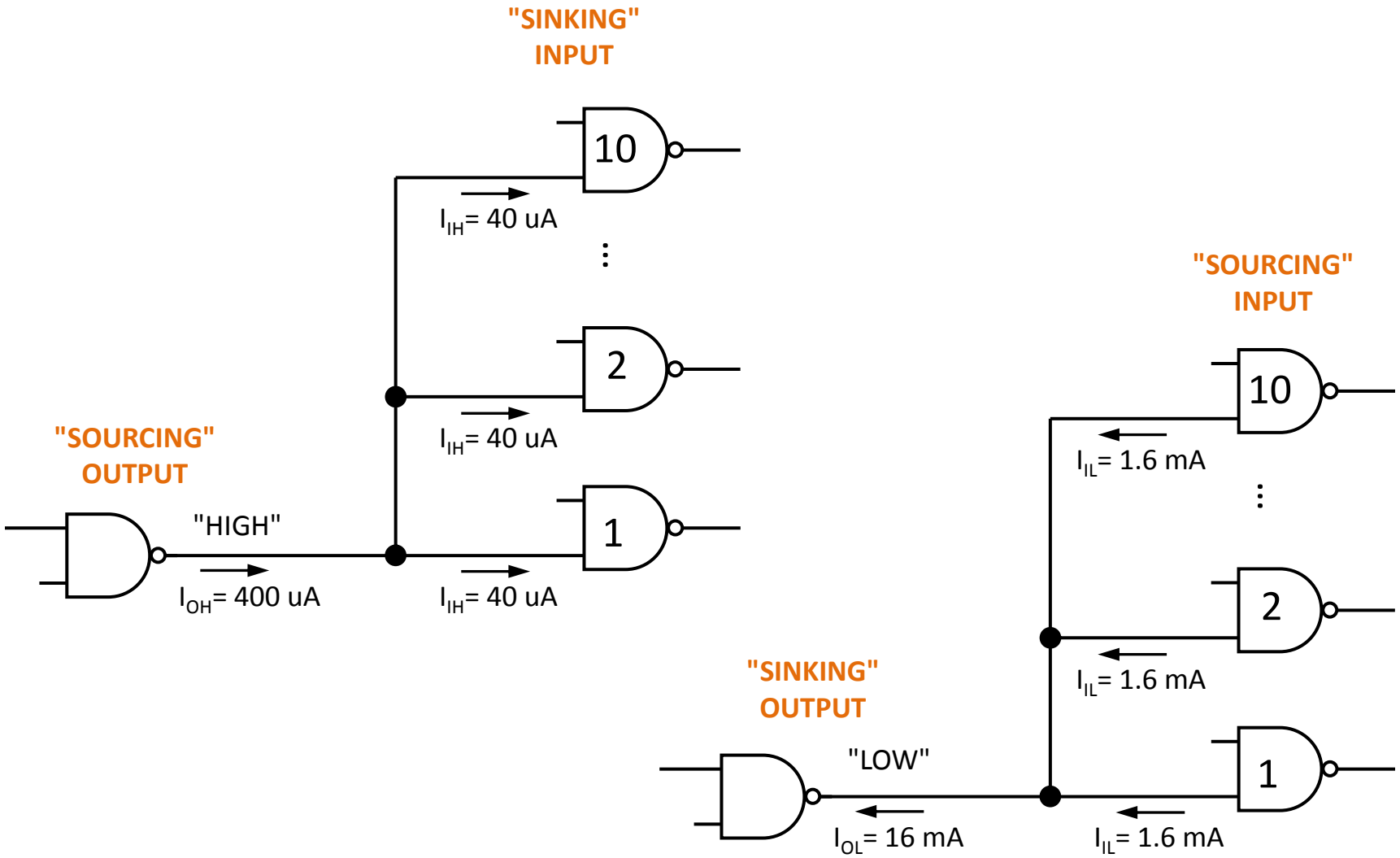
LOW-level output voltage (V)	V_{OLmax}	0.4	0.4	0.4	0.5	0.5	0.5	0.5
HIGH-level input voltage (V)	V_{IHmin}	2.0	2.0	2.0	2.0	2.0	2.0	2.0
HIGH-level output voltage (V)	V_{OHmin}	2.4	2.4	2.4	2.7	2.7	2.7	2.7
LOW-level input current (mA)	I_{ILmax}	−1.6	−0.18	−2.0	−2.0	−0.4	−2.0	−0.2
LOW-level output current (mA)	I_{OLmax}	16	3.6	20	20	8	20	8
HIGH-level input current (μA)	I_{IHmax}	40	10	50	50	20	200	20
HIGH-level output current (μA)	I_{OHmax}	−400	−200	−500	−1000	−400	−2000	−400

Currents going into device are considered positive

TTL SINKS AND SOURCES



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LOW-level output voltage (V)	V_{OLmax}	0.4	0.4	0.4	0.5	0.5	0.5	0.5
HIGH-level input voltage (V)	V_{IHmin}	2.0	2.0	2.0	2.0	2.0	2.0	2.0
HIGH-level output voltage (V)	V_{OHmin}	2.4	2.4	2.4	2.7	2.7	2.7	2.7
Input Sourcing current (mA)	I_{ILmax}	−1.6	−0.18	−2.0	−2.0	−0.4	−2.0	−0.2
Output Sinking current (mA)	I_{OLmax}	16	3.6	20	20	8	20	8
Input Sinking current (mA)	I_{IHmax}	40	10	50	50	20	200	20
Output Sourcing current (uA)	I_{OHmax}	−400	−200	−500	−1000	−400	−2000	−400

ELECTRONIC LOGIC

Table 2–6 Characteristics of CMOS families operating with V_{CC} between 4.5 and 5.5 V.

Description	Symbol	Condition	Family 74HC	74HCT	74AC	74ACT
Typical propagation delay (ns)			18	18	5.25	4.75
Quiescent power dissipation per gate (mW)		V_{in} = 0 or V_{CC}	0.0025	0.0025	0.005	0.005
		V_{in} = 2.4 V	n/a	12	n/a	7.5
Power dissipation capacitance (pF)	C_{PD}		24	24	30	30
Dynamic power dissipation per gate (mW/MHz)			0.60	0.60	0.75	0.75
Total power dissipation per gate (mW)		f = 100 kHz	0.0625	0.0625	0.080	0.080
		f = 1 MHz	0.6025	0.6025	0.755	0.755
		f = 10 MHz	6.0025	6.0025	7.505	7.505
Speed-power product (pJ)		f = 100 kHz	1.1	1.1	0.4	0.4
		f = 1 MHz	10.8	10.8	3.9	3.6
		f = 10 MHz	108	108	39	36
Input leakage current (μA)	I_{Imax}	V_{in} = any	±1	±1	±1	±1
LOW-level input voltage (V)	V_{ILmax}		1.35	0.8	1.35	0.8
HIGH-level input voltage (V)	V_{IHmin}		3.85	2.0	3.85	2.0
LOW-level output current (mA)	I_{OLmaxC}	CMOS load	0.02	0.02	0.05	0.05
	I_{OLmaxT}	TTL load	4.0	4.0	24.0	24.0
LOW-level output voltage (V)	V_{OLmaxC}	$I_{out} \le I_{OLmaxC}$	0	0.1	0.1	0.1
	V_{OLmaxT}	$I_{out} \le I_{OLmaxT}$		0.33	0.37	0.37
HIGH-level output current (mA)	I_{OHmaxC}	CMOS load		–0.02	–0.05	–0.05
	I_{OHmaxT}	TTL load	0	–4.0	–24.0	–24.0
HIGH-level output voltage (V)	V_{OHminC}	$\|I_{out}\| \le \|I_{OH}$	4.4	4.4	4.4	4.4
	V_{OHminT}	$\|I_{out}\| \le \|I$	3.84	3.84	3.76	3.76

Compatible w/ TTL Voltages!

ELECTRONIC LOGIC

Table 2–6 Characteristics of CMOS families operating with V_{CC} between 4.5 and 5.5 V.

Description	Symbol	Condition	Family 74HC	74HCT	74AC	74ACT
Typical propagation delay (ns)			18	18	5.25	4.75
Quiescent power dissipation per gate (mW)		V_{in} = 0 or V_{CC}	0.0025	0.0025	0.005	0.005
		V_{in} = 2.4 V	n/a	12	n/a	7.5
Power dissipation capacitance (pF)	C_{PD}		24	24	30	30
Dynamic power dissipation per gate (mW/MHz)			0.60	0.60	0.75	0.75
Total power dissipation per gate (mW)		f = 100 kHz	0.0625	0.0625	0.080	0.080
		f = 1 MHz	0.6025	0.6025	0.755	0.755
Speed-power product (pJ)		f = 10 MHz	108	108	39	36
Input leakage current (μA)	I_{Imax}	V_{in} = any	±1	±1	±1	±1
LOW-level input voltage (V)	V_{ILmax}		1.35	0.8	1.35	0.8
HIGH-level input voltage (V)	V_{IHmin}		3.85	2.0	3.85	2.0
LOW-level output current (mA)	I_{OLmaxC}	CMOS load	0.02	0.02	0.05	0.05
	I_{OLmaxT}	TTL load	4.0	4.0	24.0	24.0
LOW-level output voltage (V)	V_{OLmaxC}	$I_{out} \le I_{OLmaxC}$	0.1	0.1	0.1	0.1
	V_{OLmaxT}	$I_{out} \le I_{OLmaxT}$	0.33	0.33	0.37	0.37
HIGH-level output current (mA)	I_{OHmaxC}	CMOS load	–0.02	–0.02	–0.05	–0.05
	I_{OHmaxT}	TTL load	–4.0	–4.0	–24.0	–24.0
HIGH-level output voltage (V)	V_{OHminC}	$\|I_{out}\| \le \|I_{OHmaxC}\|$	4.4	4.4	4.4	4.4
	V_{OHminT}	$\|I_{out}\| \le \|I_{OHmaxT}\|$	3.84	3.84	3.76	3.76

Very low static power consumption!

EXCESS LOADING HAS NEGATIVE EFFECTS

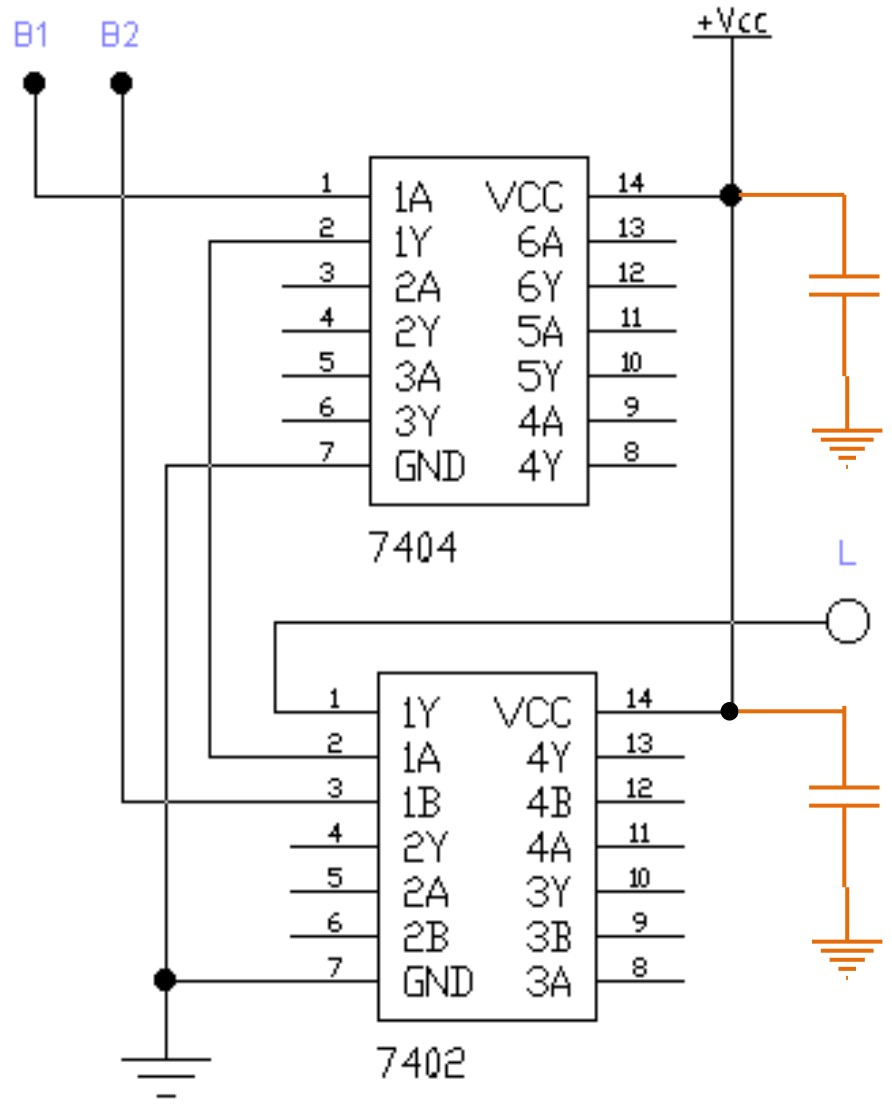
Loading an output with more than rated fan-out or current capacity has the following effects:

- In the LOW state, the output voltage (V_{OL}) may increase beyond the rated maximum
- In the HIGH state, the output voltage (V_{OH}) may drop below the rated minimum
- The propagation delay from the input to the output may increase beyond the rated maximum
- The rise and fall time from LO-to-HI and HI-to-LO transition may increase beyond the rated maximum

DECOUPLING CAPACITORS

Provide local power to meet transient needs of ICs during operation

- As components operate, their need for current varies. These transients can cause component interaction through the power supply circuitry
- General rule of thumb: decoupling capacitor for each IC to be 0.01 – 0.1 μF
- Need to be placed across the +5 V and GND for each IC chip (with short leads!)
- More sophisticated approaches needed above 50 MHz



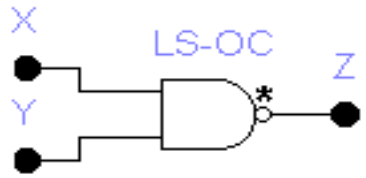
A FLOATING INPUT CAN ACT AS AN ANTENNA

Never leave unused inputs unattached (floating), as they can pick up noise…

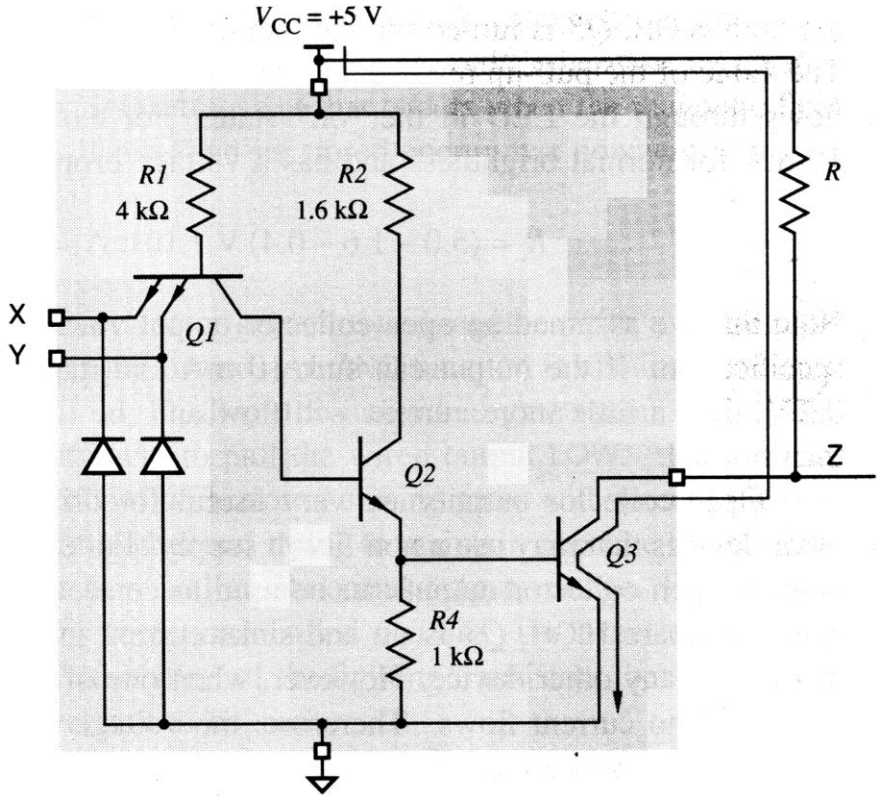
- To force a HI:
  - for TTL, connect input to V_{CC} through a 1 kΩ resistor
  - for CMOS, connect input directly to V_{CC}
- To force a LO:
  - connect inputs directly to digital ground

OPEN COLLECTOR OUTPUT

- Gate output without the active pull-up transistor. The output of the gate is the open collector terminal of the output transistor.
- To convert open collector output to voltage, an external pull-up resistor (on the order of 1 kΩ) is used to connect the output to a 5 volt source.

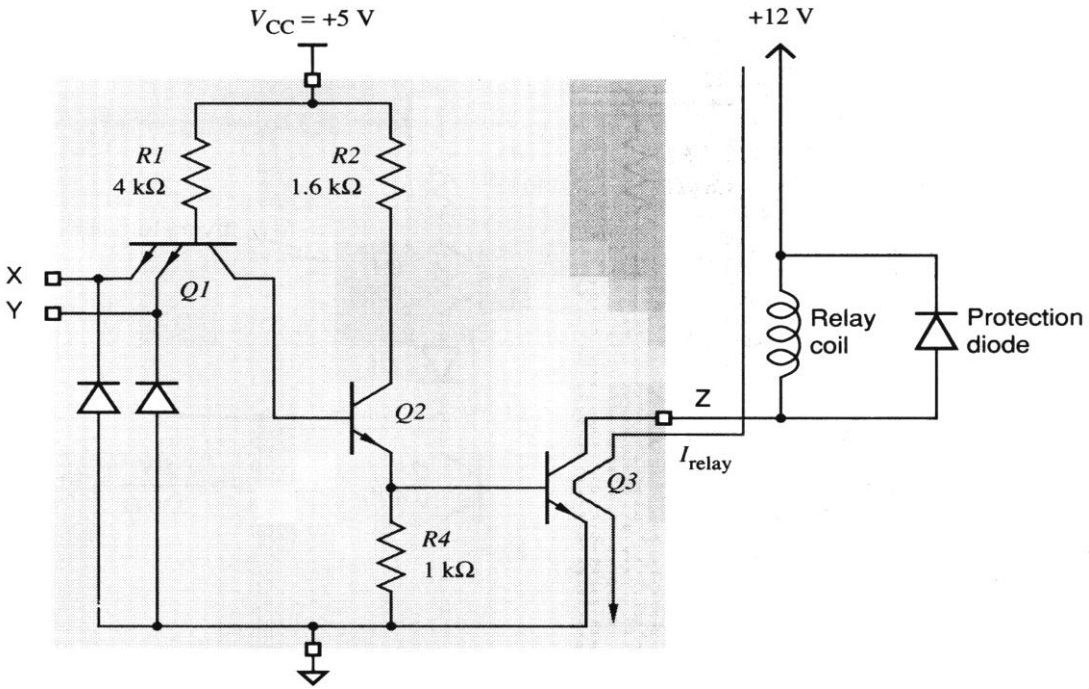


- Pull-up resistor choice is lower bounded by the maximum allowable current sink of the device.
- Smaller pull-up for higher speed, but with higher power drain.

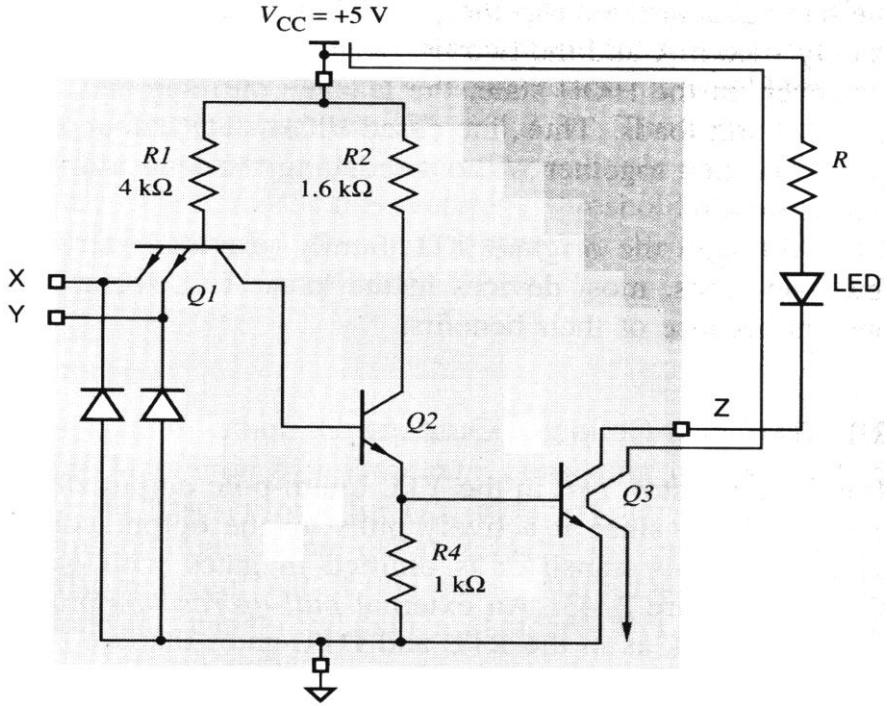


OPEN COLLECTOR OUTPUT

Drive light-emitting diodes (LEDs), relays and other devices



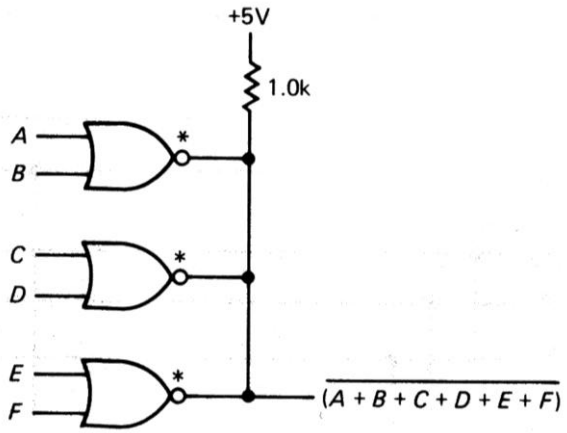
Can Q3 safely sink the necessary current?



OPEN COLLECTOR OUTPUT

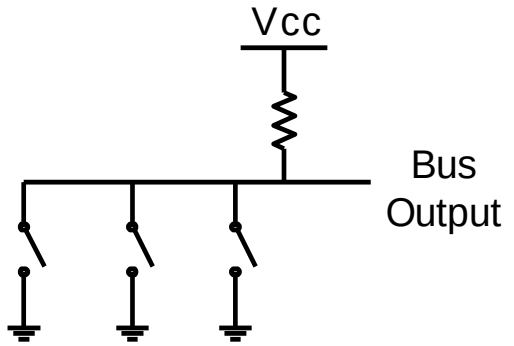
Wired Logic

- Depends on the logic convention, a free AND/OR gate can be constructed by wiring the open collector outputs together



Bus Connection

- Allowing several device to share an output wire. Any device that closes its switch determines the state of the output



THREE STATE OUTPUT DISCONNECTS DEVICE FROM BUS

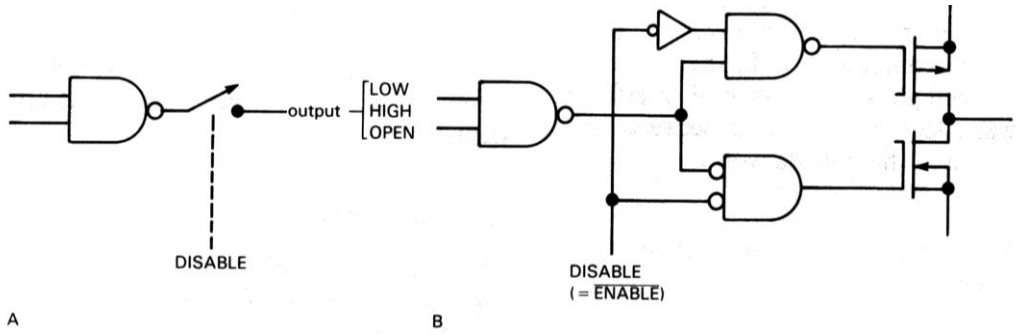
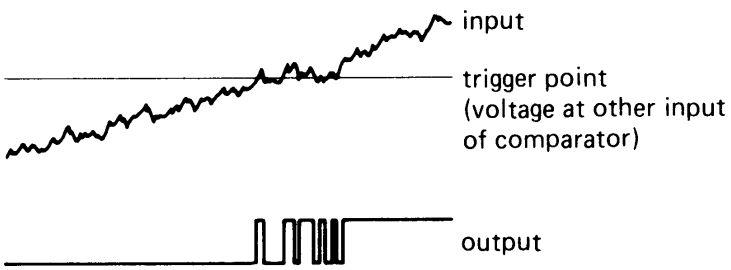


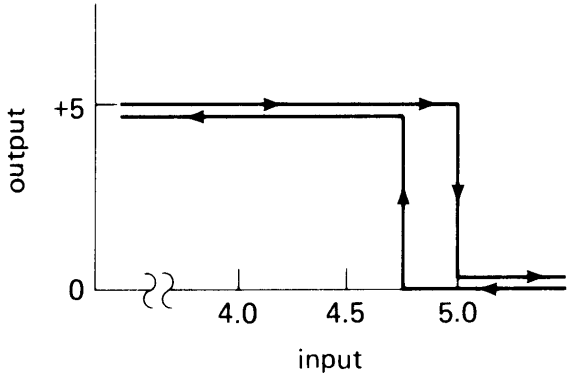
Figure 8.19. Three-state CMOS NAND gate.
A. Conceptual diagram.
B. Realization with internal CMOS gates.

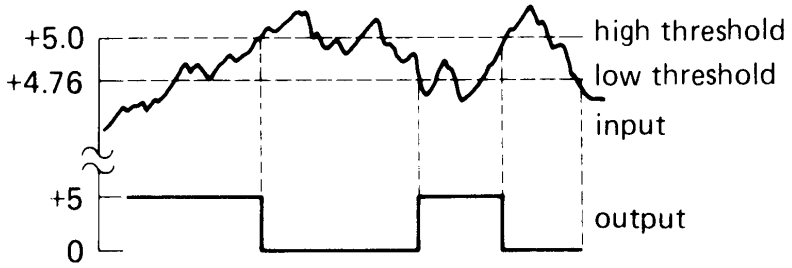
- When disconnected, the device is referred to as being in the high impedance state – Does not mean three logic states!
- Uses a separate ENABLE input to determine the status of the output – a more complicated circuit
- More noise immune and faster than open collector outputs. Also called Tri-State Logic (trade name of Nat'l Semiconductor)

SCHMITT TRIGGER



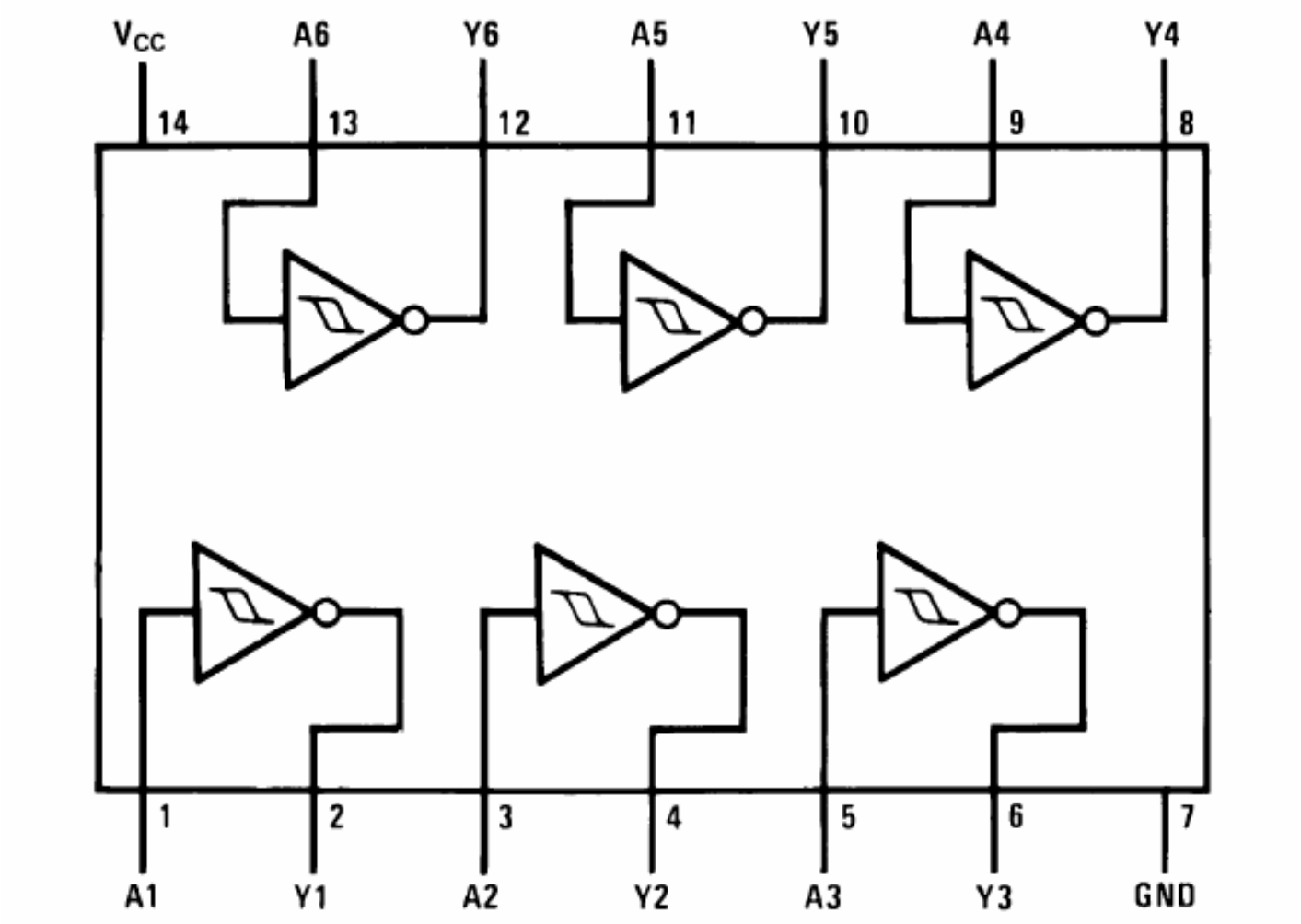
- 1-bit analog-to-digital conversion
- The "converter" is the switching device
- Sharp switching boundary can cause multiple switches if there are oscillations in the analog signal





- Schmitt trigger uses a boundary defined with hysteresis to minimize the switching transients

SCHMITT TRIGGER



7414 – Hex Inverter with Schmitt Trigger Inputs

INTEGRATED CIRCUIT (IC) PACKAGES

DIP (Dual Inline Package)

SMD (Surface Mount Device)

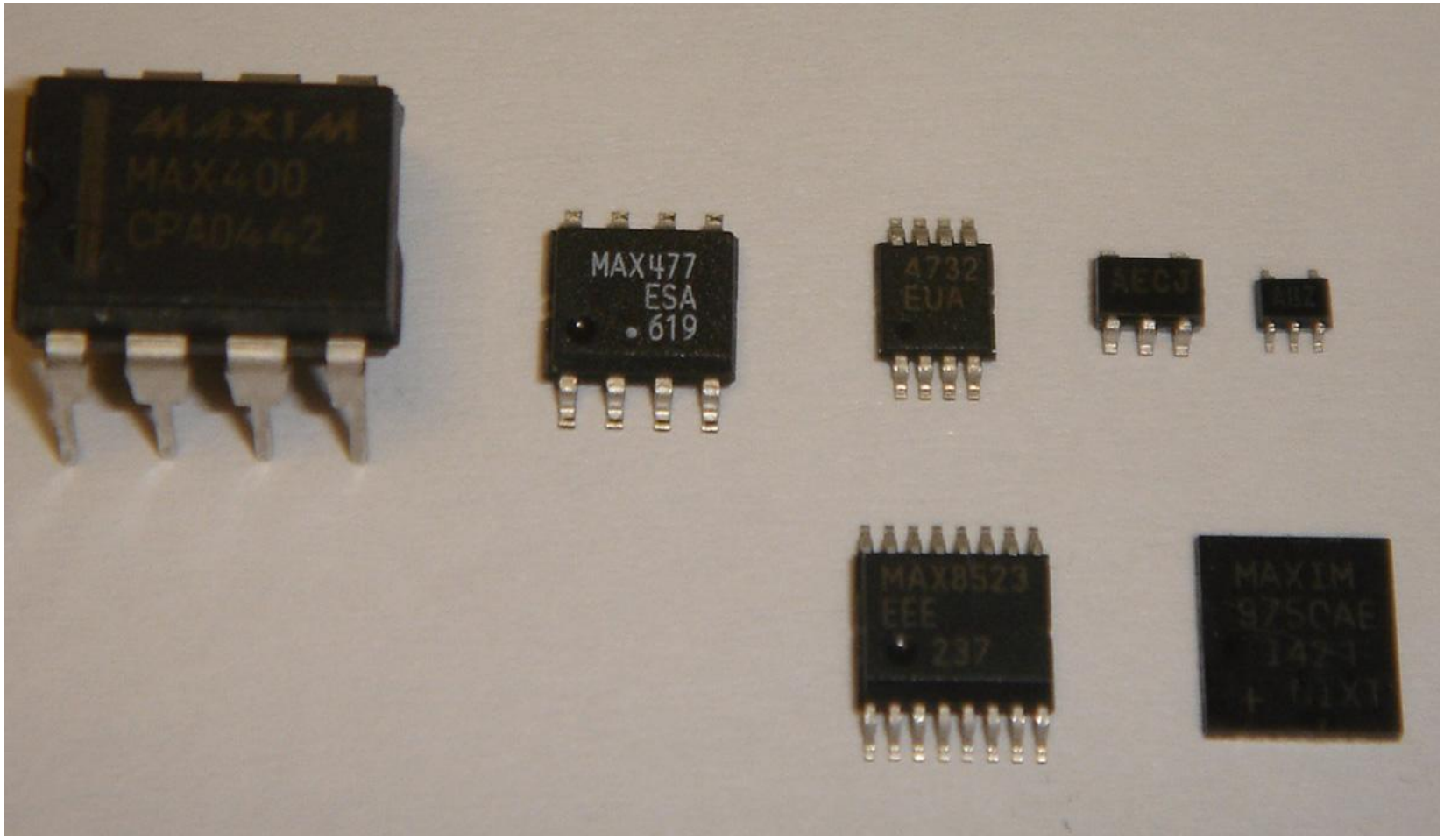
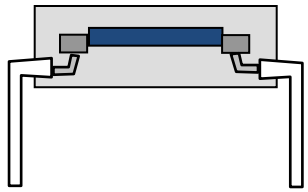


Image: https://i.cmpnet.com/planetanalog/2006/04/C0039-Figure%201.jpg

INTEGRATED CIRCUITS

One or more gates fabricated on a single silicon chip:



Small-Scale Integration (SSI)

- 1 to 20 gates, basic building blocks of digital design
- Uses dual in-line package (DIP), standard pinout for 7400 series ICs
- Gradually been replaced by programmable logic devices (PLDs)

Medium-Scale Integration (MSI)

- 20 to 200 gates
- Functional building blocks, e.g. decoder, multiplexer, counter, …

Large-Scale Integration (LSI)

- 200 to 20,000 gates
- Memories, microprocessors, PLDs, …

Very Large-Scale Integration (VLSI)

- Any thing above 500,000 transistors

WHY PROGRAMMABLE LOGIC DEVICES?

- Electronic systems often consist of a few small logic circuits that "glue" together large-scale ICs. Not infrequently, the precise system configuration needs to be "tweaked" to account for application-specific inputs or data formatting.

- Programmable logic devices (PLDs) allow systems to be easily configured, often late in the design cycle. Rather than possessing a fixed function at the time of manufacture, a PLD must be "programmed" prior to use.

- Very fast — much faster than a microcontroller.

COMING UP…

Computer Systems

- Programmable devices
- Sequential logic
- Finite state machines