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June 18 – 20, 2012
The Pennsylvania State University
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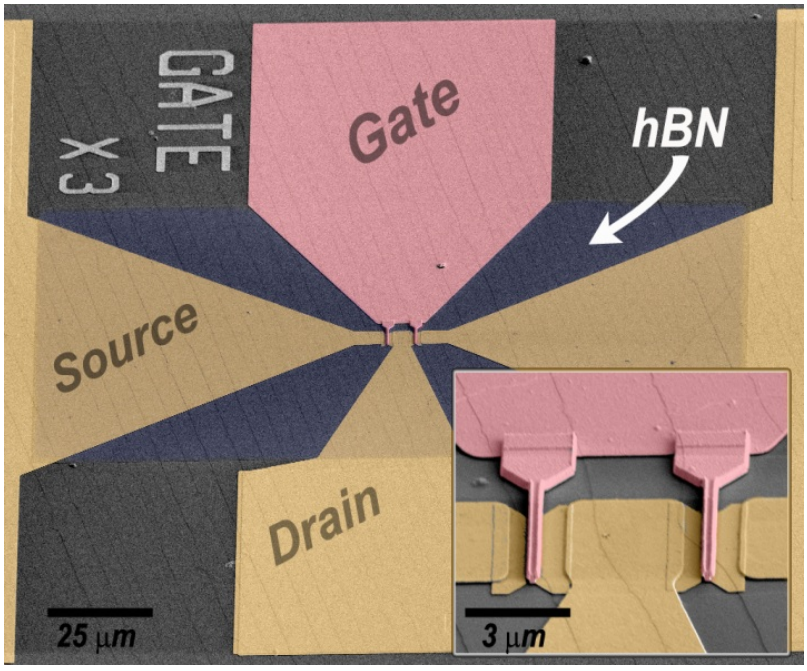
70th DRC

IEEE

DEVICE RESEARCH CONFERENCE



Conference Digest

Front Cover Image: False color SEM image of a high frequency graphene FET utilizing h-BN as the dielectric material. © 2012 Penn State

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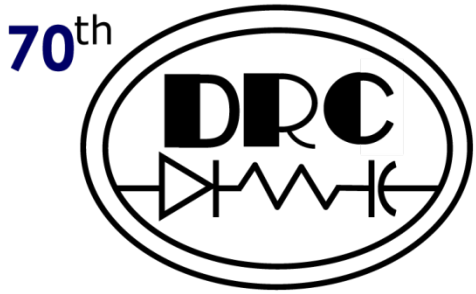

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Schedule of Events

SUNDAY PM, JUNE 17TH, 2012

Check-In/Registration ..... 3:00 – 6:00 PM
Location ..... Registration Desk – Conference Wing

Welcoming Reception ..... 5:00 PM – 6:30 PM
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G. Li, R. Wang, J. Verma, H. Xing, D. Jena, Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA

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T. J. Anderson[1], K. D. Hobart[1], M. J. Tadjer[2], T. I. Feygelson[3], E. A. Imhoff[1], D. J. Meyer[1], D. S. Katzer[1], J. K. Hite[1], F. J. Kub[1], B. B. Pate[1], S. C. Binari[1], and C. R. Eddy, Jr[1], [1] Naval Research Laboratory, Washington District of Columbia, USA, [2] Universidad Politécnica de Madrid, Madrid, SPAIN and [3] SAIC, Inc., Washington, District of Columbia, USA

IV.A-4 9:20 AM **Record low tunnel junction specific resistivity (< 3X10-4 Ocm2) in GaN inter-band tunnel junctions**
S. Krishnamoorthy[1], F. Akyol[1], J. Yang[2], P. S. Park[1], R. C. Myers[2,1], S. Rajan[1,2], [1]Department of Electrical & Computer Engineering, The Ohio State University, Columbus, Ohio, USA and [2]Department of Material Science & Engineering, The Ohio State University, Columbus, Ohio, USA

IV.A-5 9:40 AM **Ga_2O_3 Schottky barrier diodes fabricated on single-crystal ß-Ga_2O_3 substrates**
K. Sasaki[1,2], M. Higashiwaki[2,3], A. Kuramata[1], T. Masui[4], and S. Yamakoshi[1], [1]Tamura Corporation, Sayama, Saitama, JAPAN, [2]National Institute of Information and Communications Technology, Koganei, Tokyo, JAPAN, [3]PRESTO, Japan Science and Technology Agency, Chiyoda, Tokyo, JAPAN, and [4]Koha Co., Ltd., Nerima, Tokyo, JAPAN

IV.A-6 10:20 AM **Quaternary nitride enhancement mode HFET with 260 mS/mm and a threshold voltage of +0.5 V**
N. Ketteniss[1], B. Reuters[1], B. Holländer[2], H. Hahn[1], H. Kalisch[1], and A. Vescan[1], [1]GaN Device Technology, RWTH Aachen University, Aachen, GERMANY and [2]Forschungszentrum Juelich GmbH, Juelich, GERMANY

IV.A-7 10:40 AM **Methods for Attaining High Interband Tunneling Current in III-Nitrides**
T. A. Growden, S. Krishnamoorthy, D. N. Nath, A. Ramesh, S. Rajan, and P. R. Berger
Department of Electrical and Computer Engineering, The Ohio State University, Columbus, Ohio, USA

IV.A-8 11:00 AM **Experimental Demonstration of a Wafer-Bonded Heterostructure based Unipolar Transistor with In0.53Ga0.47As Channel and III-N Drain**
S. Lal[1], J. Lu[1], B. Thibeault[1], S. P. Denbaars[2], and U. K. Mishra[1], [1]Department of Electrical and Computer Engineering and [2]Materials Department, University of California, Santa Barbara, California, USA

IV.A-9 11:20 AM **Electrical Evidence of Disorder at the SiO2/4H-SiC MOS Interface and its Effect on Electron Transport**
S. Swandono, A. Penumatcha, and J. A. Cooper, School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana, USA

IV.A-10 11:40 AM **Asymmetric Dual-Grating Gate InGaAs/InAlAs/InP HEMTs for Ultrafast and Ultrahigh Sensitive Terahertz Detection**
S. Boubanga-Tombet[1], Y. Tanimoto[1], T. Watanabe[1], T. Suemitsu[1], W. Yuye[2], H. Minamidev[2], H. Ito[2], V. Popov[3], and T. Otsuji[1], [1]Research Institute of Electrical Communication, Tohoku University, Aoba-Ku, Sendai , JAPAN, [2]RIKEN Sendai, Aoba-ku, Sendai, JAPAN, and [3]Institute of Radio Engineering and Electronics (Saratov Branch), Saratov, RUSSIA

Session IV.B. **1/2-Dimensional FETs** 171-190

IV.B-1 **Role of Screening, Heating, and Dielectrics on High-Field Transport in Graphene**
8:20 AM A. Y. Serov, Z.-Y. Ong, V. E. Dorgan and E. Pop, Dept. of Electrical and Computer Engineering, University of Illinois, Urbana-Champaign, Illinois, USA and Micro and Nanotechnology Lab, Urbana Illinois, USA

IV.B-2 **Graphene field-effect transistors with self-aligned spin-on-doping of source/drain access regions**
8:40 AM H. C. P. Movva[1], M. E. Ramón[1], C. M. Corbet[1], F. S. Chowdhury[1], G. Carpenter[2], E. Tutuc[1], and S. K. Banerjee[1], [1]Microelectronics Research Center, The University of Texas at Austin, Texas, USA and [2]IBM Research, Austin, Texas, USA

IV.B-3 **High Performance, Large Area Graphene Transistors on Quasi-Free-Standing Graphene Using Synthetic Hexagonal Boron Nitride Gate Dielectrics**
9:00 AM M. J. Hollander, A. Agrawal, M. S. Bresnehan, M. LaBella, K. A. Trumbull, R. Cavalero, S. Datta, and J. A. Robinson, The Pennsylvania State University, University Park, Pennsylvania , USA

IV.B-4 **MoS_2-based devices and circuits**
9:20 AM B. Radisavljevic, D. Krasnozhon, M.B. Whitwick, A. Kis, Electrical Engineering Institute, School of Engineering, EPFL, Lausanne, SWITZERLAND

IV.B-5 **Extraction of Near Interface Trap Density in Top Gated Graphene Transistor Using High Frequency**
10:20 AM **Current Voltage Characteristics**
H. Madan[1], M. J. Hollander[1], J. A. Robinson[2], and S. Datta[1], [1]Elec4ical Engineering, The Pennsylvania State University, University Park, Pennsylvanis, USA and [2]Material Science and Engineering. The Pennsylvania State University, University Park, Pennsylvnia, USA

IV.B-6 **Pulsed Nanosecond Characterization of Graphene Transistors**
10:40 AM E. Carrion, A. Malik, A. Behnam, S. Islam, F. Xiong and E. Pop, Dept. of Electrical and Computer Engineering, University of Illinois, Urbana-Champaign, Illinois, USA and Micro and Nanotechnology Lab, Urbana Illinois, USA

IV.B-7 **Graphene Nanomesh Contacts and Its Transport Properties**
11:00 AM T. Chu and Z. Chen, ECE Department and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana, USA

IV.B-8 **First Demonstration of Two-Dimensional WS2 Transistors Exhibiting 105 Room Temperature**
11:20 AM **Modulation and Ambipolar Behavior**
W. S. Hwang[1], M. Remskar[2], R. Yan[1], V. Protasenko[1], K. Tahy[1], S. D. Chae[1], H. Xing[1], A. Seabaugh[1], and D. Jena[1], [1]Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA and [2]Solid State Physics Department, Jozef Stefan Institute, Ljubljana, SLOVENIA

IV.B-9 **Low-frequency Noise in Contact and Channel Regions of Ambipolar InAs Nanowire Transistors**
11:40 AM C. J. Delker[1], Y. Zi[2], C. Yang[2,3], D. B. Janes[1], [1]School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana, USA, [2]Department of Physics, Purdue University, West Lafayette, Indiana, USA, and [3]Department of Chemistry, Purdue University, West Lafayette, Indiana, USA

Session V.A **III-V MOSFETs/FETs** 191-208

V.A-1 **High Performance III-V FETs for Low Power CMOS Applications**
1:30 PM M. Radosavljevic, Intel Corporation, Technology and Manufacturing Group, Hillsboro, Oregon, USA

V.A-2 **Vertical InAs Nanowire MOSFETs with I_{DS} = 1.34 mA/μm and gm = 1.19 mS/μm at V_{DS} = 0.5 V**
2:10 PM K.-M. Persson, M. Berg, M. Borg, J. Wu, H. Sjöland, E. Lind and L.-E. Wernersson, Department of Electrical- and Information Technology, Lund University, Lund, SWEDEN

V.A-3 **Possible Observation of Ballistic Contact Resistance in Wide Si MOSFETs**
2:30 PM A. Majumdar[1] and D. A. Antoniadis[2], [1]IBM Research Division, T. J. Watson Research Center, Yorktown Heights, New York, USA and [2]Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, Massachusetts, USA

V.A-4 **Regrown Ohmic Contacts to InxGa1-xAs Approaching the Quantum Conductivity Limit**
2:50 PM J. J. M. Law, A. D. Carter, S. Lee, A. C. Gossard, M. J. W. Rodwell, ECE and Materials Departments, University of California, Santa Barbara, California, USA

V.A-5 **Simulation Study of Nanowire Tunnel FETs**
3:30 PM A. Schenk[1], R. Rhyner[1], M. Luisier[1], and C. Bessir[2], [1]Integrated Systems Laboratory, ETH Zürich, Zürich, SWITZERLAND and [2]IBM Research-Zürich, Rüschlikon, SWITZERLAND

V.A-6 **Flicker Noise Characterization and Analytical Modeling of Homo and Hetero-Junction III-V Tunnel FETs**
4:10 PM R. Bijesh, D. K. Mohata, H. Liu and S. Datta, Pennsylvania State University, University Park, Pennsylvania, USA

V.A-7 **High Current Density InAsSb/GaSb Tunnel Field Effect Transistors**
4:30 PM A. W. Dey[1], B. M. Borg[2], B. Ganjipour[2], M. Ek[3], K. A. Dick[2,3], E. Lind[1], P. Nilsson[1], C. Thelander[2] and L.-E. Wernersson[1], [1]Dept. of Electrical and Information Technology, [2]Dept. of Solid State Physics and [3],Division of Polymer and Materials Chemistry, Lund University, Lund, SWEDEN

V.A-8 **Gate-first implant-free InGaAs n-MOSFETs with sub-nm EOT and CMOS-compatible process suitable**
4:50 PM **for VLSI**
L. Czornomaz, M. El Kazzi, D. Caimi, C. Rossel, E. Uccelli, M. Sousa, C. Marchiori, M. Richter, H. Siegwart and J. Fompeyrine, IBM Zurich Research Laboratory, Rüschlikon, SWITZERLAND

Session V.B **Spin/Memory Devices** **209-222**

V.B-1 **Ultrafast Spin Torque Memory Based on Magnetic Tunnel Junctions with Combined In-plane and**
1:30 PM **Perpendicular Polarizers**
I. N. Krivorotov[1], G. E. Rowlands[1], T. Rahman[2], J. A. Katine[1], J. Langer[4], A. Lyle[4], H. Zhao[2], J. G. Alzate[5], A. A. Kovalev[6], Y. Tserkovnyak[6], Z. M. Zeng[6], H. W. Jiang[6], K. Galatsis[5], Y. M. Huai[7], P. Khalili Amiri[5], K. L. Wang[5], and J.-P. Wang[2], [1]Physics and Astronomy, University of California, Irvine, California, USA, [2]Electrical and Computer Engineering, University of Minnesota, Minneapolis, Minnesota, USA, [3]Hitachi Global Storage Technologies, San Jose, California, USA, [4]Singulus Technologies,Kahl am Main, GERMANY, [5]Electrical Engineering, University of California, Los Angeles, California, USA, [6]Physics and Astronomy, University of California, Los Angeles, California, USA, and [7]Avalanche Technology, Fremont, California, USA

V.B-2 **NanoMagnet Logic**
2:10 PM W. Porod, P. Li, F. Shah, M. Siddiq, E. Varga, G. Csaba, V. Sankar, G. H. Bernstein, X. S. Hu, M. Niemier, J. Nahas, and A. Orlov, Center for Nano Science and Technology, University of Notre Dame, Notre Dame, Indiana, USA

V.B-3 **Late News**
2:50 PM

V.B-4 **Nanowire Phase Change Memory with Carbon Nanotube Electrodes**
3:30 PM F. Xiong[,1,2,3], M.g-H. Bae[1,2], Y. Dai[1,2], A. D. Liao[,2], A. Behnam[1,2,] E. Carrion[1,2], S. Hong[1,2], D. Ielmini[4] and E. Pop[1,2,3], [1]Micro & Nanotechnology Lab, Univ. Illinois, Urbana-Champaign, Illinois, USA, [2]Dept. of Electrical & Computer Engineering, Univ. Illinois, Urbana-Champaign, Illinois, USA, [3]Beckman Institute, Univ. Illinois, Urbana-Champaign, Illinois, USA, and [4]Dipartimento di Elettronica e Informazione, Politecnico di Milano, Milano, ITALY

V.B-5 **A very reliable multilevel YSZ resistive switching memory**
3:50 PM Feng Pan, Jaewon Jang, Vivek Subramanian, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, California, USA

V.B-6 **A Comprehensive Model for Crossbar Memory Arrays**
4:10 PM A. Chen, Z. Krivokapic, and M.-R. Lin, TD Research, GLOBALFOUNDRIES, Sunnyvale, California, USA

V.B-7 **Spin Neuron for Ultra Low Power Computational Hardware**
4:30 PM M. Sharad, G. Panagopoulos and K. Roy, School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana , USA

Rump Sessions 223-224

R.1 **Wells vs. Sheets vs. Tubes** Session Organizers**:** Joshua Robinson, Penn State and
8:30 PM Debdeep Jena, University of Notre Dame

R.2 **Compound semiconductors on Si: "A Happy Marriage" or "Keep Your Filthy Materials Out Of My Fab"?**
8:30 PM Session Organizers: Seth Bank, The University of Texas at Austin and Yanning Sun, IBM

Joint DRC/EMC Plenary Session 225-226

8:30 AM **Nonpolar and Semipolar GaN Materials and Devices: The Journey So Far**
James S. Speck, University of California, Santa Barbara

Session VI.A Transistor Modeling 227-234

VI.A-1 **Dissipative Quantum Transport in Nanoscale Transistors**
10:00 AM Jing Guo, Department of ECE, University of Florida, Gainesville, Florida, USA

VI.A-2 **Will Strong Quantum Confinement Effect Limit Low VCC Logic Application of III-V FINFETs?**
10:40 AM A.Nidhi[1], V.Saripalli[1], V. Narayanan[1], Y. Kimura[2], R. Arghavani[2] and S. Datta[1], [1]The Pennsylvania State University, University Park, Pennsylvania, USA and [2]Lam Research, California, USA

VI.A-3 **Exploration of Vertical MOSFET and Tunnel FET Device Architecture for Sub 10nm Node Applications**
11:00 AM H. Liu, D. K. Mohata, A. Nidhi, V. Saripalli, V. Narayanan and S. Datta, The Pennsylvania State University, University Park, Pennsylvania, USA

VI.A-4 **Late News**
11:20 AM

VI.A-5 **Late News**
11:40 AM

Session VI.B Thin- Film Devices 235-246

VI.B-1 **Organic Thin-Film Transistors for Flexible Displays and Circuits**
10:00 AM H. Klauk, Max Planck Institute for Solid State Research, Stuttgart, GERMANY

VI.B-2 **Low-Voltage ZnO Double-Gate Thin Film Transistor Circuits**
10:40 AM Y. V. Li[1,2], J. I. Ramirez[1,2], K. G. Sun[1,2] and T. N. Jackson[1,2], [1]Center for Thin Film Devices and Materials Research Institute and [2]Department of Electrical Engineering, Penn State University, University Park, Pennsylvania, USA

VI.B-3 **High Performance Solution-Processed Thin-Film Transistors Based on In_2O_3 Nanocrystals**
11:00 AM S. L. Swisher, S. Volkman, K. Braam, J. Jang, and V. Subramanian, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, California USA

VI.B-4 11:20 AM **Characterization and Modeling of Metal-Insulator Transition (MIT) Based Tunnel Junctions**
E. Freeman[1], A. Kar[1], N. Shukla[1], R. Misra[1], R. Engel-Herbert[1], D. Schlom[2], V. Gopalan[1], K. Rabe[3], and S.Datta[1], [1]Pennsylvania State University, Pennsylvania, USA, [2]Cornell University, Ithaca, New York, USA, and [3]Rutgers University, New Brunswick, New Jersey, USA

VI.B-5 11:40 AM **Two-stage Model for Lifetime Prediction of Highly Stable Amorphous-Silicon Thin-Film Transistors under Low-Gate Field**
T. Liu, S. Wagner and J. C. Sturm, Princeton Institute for the Science and Technology of Materials (PRISM), and Department of Electrical Engineering, Princeton University, Princeton, New Jersey, USA

Session VII.A **Optoelectronic Devices** 247-258

VII.A-1 1:30 PM **Tunnel Injection GaN/AlN Quantum Dot UV LED**
J. Verma, P. K. Kandaswamy, V. Protasenko, A. Verma, H. Xing and D. Jena, Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA

VII.A-2 1:50 PM **Characterization and Impact of Traps in Lattice-Matched and Strain-Compensated In1-xGaxAs/GaAs1-ySby Multiple Quantum Well Photodiodes**
W. Chen[1], B. Chen[2], J. Yuan[2], A. Holmes[2], and P. Fay[1], [1]University of Notre Dame, Notre Dame, Indiana, USA and [2]University of Virginia, Charlottesville, Virginia, USA

VII.A-3 2:10 PM **InAs Avalanche Photodiode with Improved Electric Field Uniformity**
S. J. Maddox[1], W. Sun[2], Z. Lu[2], H. P. Nair[1], J. C. Campbell[2], S. R. Bank[2], [1]Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, Texas, USA and [2]Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, Virginia, USA

VII.A-4 2:30 PM **<278 nm Deep Ultraviolet LEDs with 11% External Quantum Efficiency**
M. Shatalov[1], W. Sun[1], A. Lunev[1], X.g Hu[1], A. Dobrinsky[1], Y. Bilenko[1], J. Yang[1], M. Shur[2], R. Gaska[1], C. Moe[3], G. Garrett[3], and M. Wraback[3], [1]Sensor Electronic Technology, Inc., Columbia, South Carolina, USA, [2]Department of Electrical, Computer, and Systems Engineering and Center of Integrated Electronics, Rensselaer Polytechnic Institute, New York, USA, and [3]U.S. Army Research Laboratory, Adelphi, Maryland, USA

VII.A-5 2:50 PM **Unipolar Barrier-Integrated HgCdTe Infrared Detectors**
A. M. Itsuno[1,3], J. D. Phillips[1], and S. Velicu[2], [1]Department of Electrical Engineering, University of Michigan-Ann Arbor, Ann Arbor, Michigan, USA and[2]EPIR Technologies, Inc., Bolingbrook, Illinois, USA

VII.A-6 3:10 PM **Late News**

Session VII.B **Biological Devices** 259-268

VII.B-1 1:30 PM **Physics and Scaling Prospects of pH-Based Genome Sequencers**
J. Go and M. A. Alam, School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana, USA

VII.B-2 1:50 PM **Biologically-inspired Learning Device using Three-terminal Ferroelectric Memristor**
M. Ueda[1], Y. Kaneko[1], Y. Nishitani[1], T. Morie[2] and E. Fujii[1], [1]Advanced Technology Research Laboratory, Panasonic Corporation, Seika-cho, Soraku-gun, Kyoto, JAPAN and [2]Graduate School of Life Science and Systems Engineering, Kyushu Institute of Technology, Wakamatsu-ku, Kitakyushu, JAPAN

VII.B-3 2:10 PM **Fabrication and Characterization of Field Effect Reconfigurable Nanofluidic Ionic Diodes: Towards Digitally-Programmed Manipulation of Biomolecules**
W. Guan[1], R. Fan[2], and M. A. Reed[1,3], [1]Department of Electrical Engineering, [2] Biomedical Engineering, and [3]Applied Physics, Yale University, New Haven, Connecticut, USA

VII.B-4 **Transparent Diamond-based Electrolyzer for Integration with Solar Cell**
2:30 PM C. Pietzka, Z. Gao, Y. Xu, and E. Kohn, Inst. of Electron Devices and Circuits, Ulm University, Ulm, GERMANY

VII.B-5 **Late News**
2:50 PM

VII.B-6 **Late News**
3:10 PM

(Dean's Hall I & II)

Plenary Session

Monday AM, June 18th, 2012

Session Chairs: Miguel Urteaga, Teledyne Scientific and Suman Datta, Penn State

8:20 AM Welcoming Remarks
Presentations: IEEE Fellows, Best Student Paper Awards, and IEEE EDS

8:50 AM I.-1 Plenary Paper
Mapping a Path to the Beyond-CMOS Technology for Computation
I. A. Young, Components Research, Intel Corporation, Hillsboro, Oregon, USA

9:50 AM Break

10:10 AM I.-2 Plenary Paper
Solid-State Electronics and Single-Molecule Biophysics
K. Shepard, Department of Electrical Engineering, Columbia University, New York, New York, USA

11:10 AM I.-3 Plenary Paper
Advanced Device Technologies for Defense Systems
J. C. Zolper, Raytheon Company, Waltham, Massachusetts, USA

Mapping a Path to the Beyond-CMOS Technology for Computation.

Ian A. Young
Components Research, Intel Corporation, Hillsboro, Oregon, USA.

The CMOS device technology used for computation is at an inflexion point. Although this is the technology which enabled the Semiconductor industry to make vast progress for the past 30-plus years, it is likely to see challenges going beyond the ten year horizon, particularly with regard to device scaling and energy efficiency. Thus it is extremely important for the semiconductor industry to search for a new device which can carry us to the beyond CMOS era as soon as possible. Currently, researchers are exploring novel device concepts and new information tokens as an alternative for CMOS technology. Examples of areas being actively researched are; quantum electronic devices, such as the tunneling FET, and devices based on spintronics and nano-magnetics. It is clear that choices will need to be made in the next few years to identify viable alternatives for CMOS by 2020. In order to achieve such a goal, benchmarking methodology and metrics need to be defined urgently to guide the research.

This paper describes a methodology for benchmarking beyond CMOS exploratory devices for computation using metrics that can provide insights about the device fundamental operation. A more detailed investigation of circuits based upon two beyond-CMOS devices is given in the paper. First tunneling FET (TFET) circuits are compared to low power CMOS circuits. Then the All-Spin Logic device (ASLD) is described and a spin circuit theory based simulator is used to show the functional transient operation of an all spin logic circuit.

I. BENCHMARKING BEYOND-CMOS DEVICES

The challenges of CMOS logic scaling, operating with ever lower power supply voltage to enable more energy efficient logic/computation, are more than the intrinsic transport delay of the signal propagation through the source and drain of the device and it's "on" drive current to off-state leakage ratio. There are extrinsic resistance and capacitance of the device (figure 1 (a) and (b)) together with the circuit interconnect for connecting MOSFETs to form logic gates and connecting the gates to implement the logic. These are increasing and will become a major contributor to circuit delay and energy [1]. Addressing these resistances and capacitances as dimensions scale is going to be critically important to ensure continued improvements in CMOS delay and energy.

The extrinsic resistance and capacitance is not only a challenge for CMOS, it is also a challenge for any electronic charge based switch since it also requires electron transport to charge the interconnect between devices. Even if the new device is extremely small, which is good for reducing the length of the interconnect between devices, the requirement of charging the interconnect above the switching threshold voltage can limit the benefits of a new switch device. Power delivery is also an issue that is often ignored when researching new switch device alternatives to CMOS, especially for low voltage devices. This can lead to misleading results.

Benchmark circuits for the beyond-CMOS devices that have been proposed are the inverter and the combinatorial logic such as 2-input NAND, 1 bit Adder and the 32 bit Adder [2]. In addition to combinatorial logic, a state element is required for the MUX and DEMUX circuits. The MUX/DEMUX and state element functions are needed in order to implement the fundamental logic unit in computing, a finite state machine such as an Arithmetic Logic Unit (ALU). **C**omputational performance, power (efficiency), area and scaling can be compared with these benchmark circuits. Also the interconnect solution (means of signal propagation, speed and power) must be investigated when the signal token is not charge.

To estimate the extrinsic parasitics (and the device density) for a charge-based device you need to do the device and circuit layout (figure 2). The semiconductor process generations are labeled by the critical lithography size described by the DRAM's half-pitch F. Scalable design rules are formulated in units of maximum mask misalignment λ, where typically $\lambda=F/2$. The pitch of metal 1 in a contacted transistor for example is $p_m=8\lambda$. Since the metal 1 contacted transistor pitch scales with the process generation, we approximately obtain that the metal 1 device pitch is $p_m=4F$. Since all the logic circuits (even spintronic circuits) need metal contacts at the terminals of their logic gates, their size will be determined by the metallization pitch much more than by their intrinsic device sizes. The layout area of the circuits can be estimated by drawing layouts for the most important

lines (diffusion, transistor gate ("poly"), metal 1). In most cases the contacted pitch for all these lines proves to be $8\lambda = 4F$. From these layout principles, sizes of the inverter with fanout of 4, 2-input NAND fanout-1, and 1b and 32b adder can be calculated for the beyond-CMOS switches [2] and are summarized in Table I.

Switching time and energy must be calculated for a device, taking into account whether charge, magnetization, electron spin, or any other quantity serves as the signal token. In some cases when the beyond-CMOS device does not use charge as the signal token, a charge-based clocking control might be required to enable the signal to propagate through the logic or to cut off the current supply when no logic operation is occurring, and therefore the power consumed by the clocking must be accounted for in the correct calculation.

II. TFET CIRCUITS

TFET and CMOS circuits were compared under low supply voltage operation (0.25-0.50V) using TFET and MOSFET transistor models that were extracted from atomistic and device simulations respectively, together with an interconnect model to predict the parasitic capacitive output loading from the interconnect [3]. Circuit simulations were performed for the inverter, NAND, and NOR basic logic building blocks and the simulation results were combined to predict a typical microprocessor logic path delay, its switching energy and standby power. For the CMOS analysis, high performance (low-Vt), low operating power / low standby power (high-Vt) devices were used to generate different standby power curves by sweeping supply voltage, while TFET results were achieved by varying Vt (gate work-function) and supply voltage. As the switching energy target is decreased by lowering power supply, CMOS performance degrades rapidly since it moves into the sub-threshold region of operation. In this operating region (Vdd ~ 0.35V), the TFET provides >8x performance advantage over CMOS at the same standby power and switching energy as summarized in Table II. The use of III-V broken gap heterojunctions in the TFET will improve its performance [4]; however the implications of scaling to technology nodes beyond 2020 needs to be explored.

III. ALL SPIN LOGIC CIRCUITS

A lateral spin injection-detection device proposed recently is the all spin logic device (ASLD). The device consists of two nanomagnets communicating via a non-magnetic channel [5] as shown in figure 3 (a) and (b). Currents through the magnets create populations of spin polarized carriers underneath them and setup spin diffusion (or drift) currents through the channel. The direction of this spin current is determined by the densities of spin polarized carriers under the two magnets. If a ground terminal is set near the first input magnet, it can be shown that it acts as a fixed magnetic terminal, while the second magnet responds to the spin diffusion current, depending on the applied voltages. For a positive voltage applied to both the magnets, the device acts like an inverting gate, where the output becomes a logical opposite of the input magnetization. For negative applied voltages, the output becomes a copy of the input magnetization. The sectioned structure of the spin diffusion channel is required to isolate spin logic gates, where the interconnection between gates (concatenation) is achieved by connecting them with a spin diffusion channel. The non-reciprocity of (input to output signal transport) ASLD comes from an asymmetry in the device due to the asymmetric location of the ground terminal. This can also be achieved via other structural techniques.

Spin circuit simulation modeling with thermal effects [6] (figure 3 (c) and (d) and figure 4), predicts the variable and asymmetric transient delay of an ASLD based all spin logic circuit. The ASLD has an energy-delay metric of approximately 30 fJ/bit and can operate with up to 2 GHz clocking rate while having zero leakage power (ignoring overheads) with existing nominal material parameters [6]. Compared to a CMOS technology with 60 nW of idle power per transistor, non-volatile spin logic has 0W idle power in the hold state with a 7 year retention time. This will outperform CMOS logic in idle power by several orders of magnitude. However the energy-delay metric of the ASLD will need to be improved with enhanced spin-electrical transduction methods, materials and anisotropy engineering, so that it could achieve the performance (computational efficiency) needed for a beyond-CMOS device.

References:

[1] I. Young, "MOSFET Extrinsic Parasitic Elements", Short Course, IEDM, December 2011.
[2] K. Bernstein, et al., "Device and Architecture Outlook for Beyond-CMOS Switches", Proceedings IEEE v. 98, pp. 2169-84 (2010).

[3] U. Avci, et al., “Comparison of Performance, Switching Energy and Process Variations for TFET and MOSFET Logic”, Symposium on VLSI Technology, June 14-16th, 2011, Page(s): 124 - 125.
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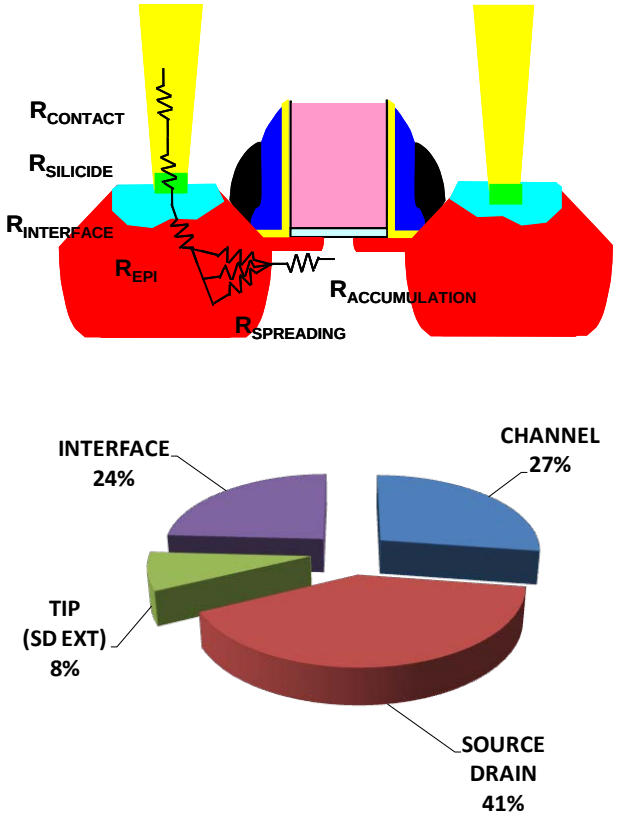

Figure 1(a). Sources of MOSFET Extrinsic Resistance and its breakdown relative to the channel resistance.

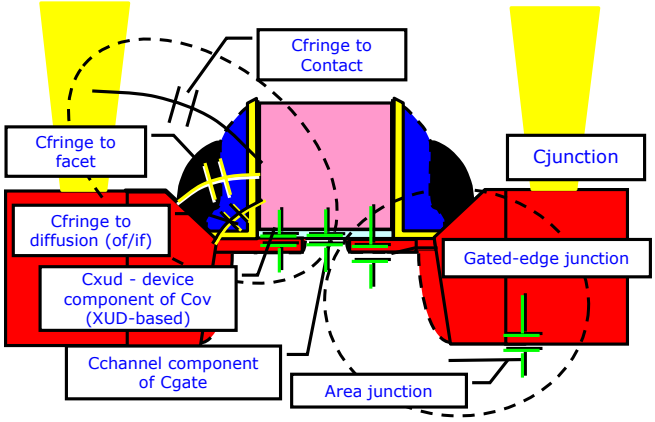

Figure 1(b). MOSFET Extrinsic Capacitance

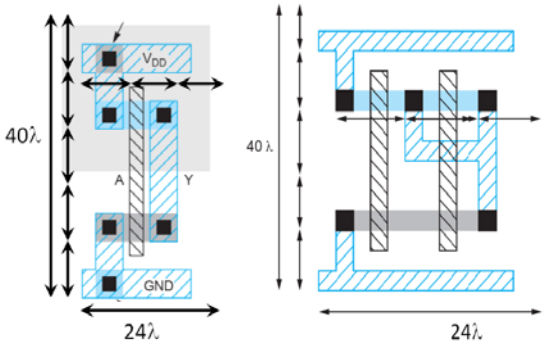

Figure 2. Layout and area estimation for an inverter and a 2-input NAND gate.

	Device	INVFO4	NAND2	Adder1	Adder32
CMOS HP	30	792	360	3780	181440
CMOS LP	30	792	360	3780	181440
IIIvTFET	30	792	360	3780	181440
HJTFET	30	792	360	3780	181440
gnrTFET	30	792	360	3780	181440
GpnJ	108	390	162	2430	116640
BisFET	30	792	360	3780	181440
SpinFET	30	792	360	3780	181440
STT/DW	20	120	30	630	30240
STMG	81	121	121	547	26244
STTtriad	81	486	121	1640	78732
STOlogic	81	121	121	547	26244
ASLD	81	121	121	364	17496
SWD	81	121	121	182	8748
NML	162	243	243	1093	52488

Table I.
Estimate of size of logic circuits in units of F^2 for the beyond-CMOS switches described in [2].

TFET @0.35V	Stage Delay (ps)	Switching Energy (fJ)	Leakage Power (nW)
INV (FO=3)	105	0.26	0.37
NAND (FO=3)	149	0.32	0.57
NOR (FO=3)	158	0.34	0.54
Combined	129	0.29	0.46

CMOS @0.3V	Stage Delay (ps)	Switching Energy (fJ)	Leakage Power (nW)
INV (FO=3)	830	0.25	0.37
NAND (FO=3)	1364	0.32	0.56
NOR (FO=3)	1389	0.33	0.53
Combined	1103	0.29	0.46

Table II. Comparison of TFET and CMOS results at low voltage, where they have same standby power (**0.5nW**) and switching energy (**0.3fJ**). At this point, TFET has **8x** higher performance.

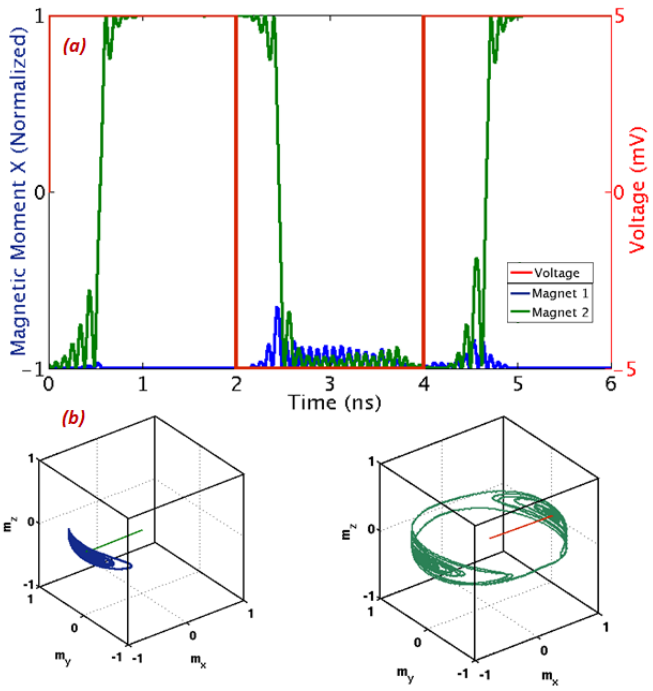

Figure 4. a) Transient self-consistent simulation of a spin circuit device b) Trajectory of the magnetic moment of the nanomagnets

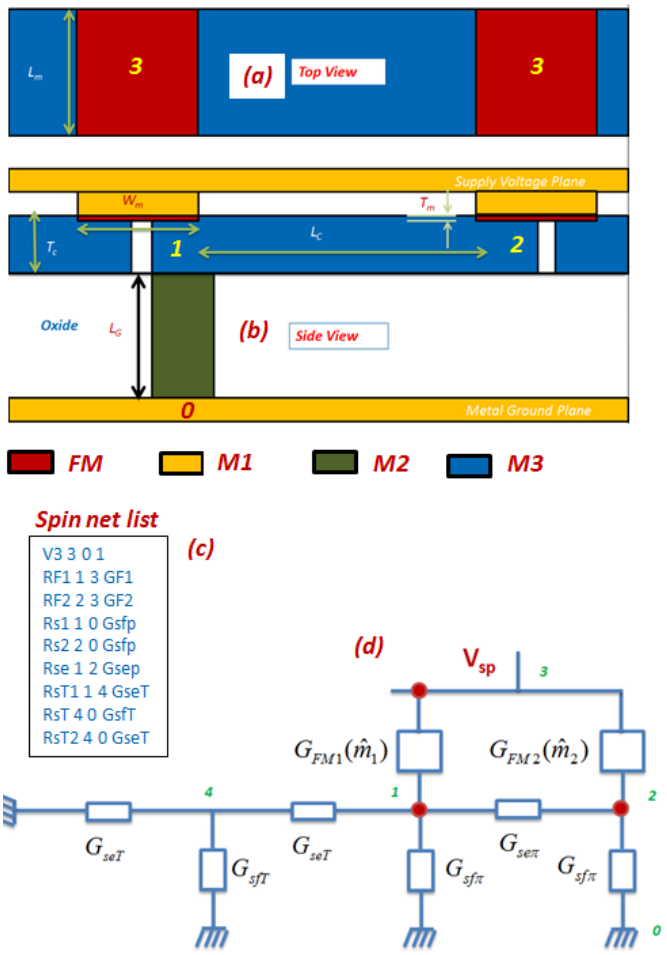

Figure 3.
A lateral spin logic device comprised of two nano-magents and non-magnetic channels. Channel connecting node 1 to node 2 acts as an interconnect between the two nano-magnets transporting spin polarized current.
(a) Top view of an all spin logic device.
(b) Side view of a lateral all spin logic device.
(c) Netlist of the circuit model that can be parsed by a spin Modified Nodal Analysis algorithm to simulate.
(d) Circuit model of spin logic device.

Solid-State Electronics and Single-Molecule Biophysics

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Biomolecular systems are traditionally studied using ensemble measurements and fluorescence-based detection. Among the most common *in vitro* applications are DNA microarrays to identify target gene expression profiles [1] and enzyme-linked immunosorbent assays (ELISA) to identify proteins [2]. While much can be determined with ensemble measurements, scientific and technological interest is rapidly moving to single-molecule techniques. When probing at the single-molecule level, observations can be made about the inter- and intramolecular dynamics that are usually hidden in ensemble measurements. In molecular diagnostic, single-molecule techniques often do not require amplification and simplify sample preparation. The most popular single-molecule techniques based on fluorescence [3, 4] are fundamentally limited in resolution and bandwidth by the countable number of photons emitted by a single fluorophore (typically on the order of 2500 photons/sec). Instrumentation is complex, expensive, and large-form-factor. Furthermore, most optical probes photobleach, limiting observation times and pump powers. Single-molecule measurements of the kinetics of fast biomolecular processes are often unavailable through fluorescent techniques, as they lack the required temporal resolution.

Solid-state nanoscale devices, which are now on the scale of individual molecules, now provide a unique opportunity to transduce the behavior of single molecules to electrons without photons as an intermediary. Solid-state nanopores represent one such technique, which can monitor when a single molecule translocates through a nanoscale pore in a thin dielectric membrane [5]. In our own recent work, we have shown how these solid-state nanopores can be integrated with CMOS electronics to significantly improve the fidelity of nanopore measurements[6]. Fig. 1 shows this integrated configuration. Measured noise spectra are shown in Fig. 2 and compared with started rack-mounted electrophysiological amplifiers. Fig. 3 shows typical time domain waveshapes of DNA molecules translocating through these pores. Another recent technique is based on attaching biomolecules directly to a defect in a carbon nanotube field-effect transistor, which is sensitive to local charge density down to the single molecule level[7]. Fig. 4 shows this configuration. Fig. 5 shows typical time-domain waveshapes for the tube conductance in the presence of DNA-DNA binding. Fig. 6 shows the typical dynamic disorder observed in these studies in which there are periods of time characterized by different microscopic kinetics. Both nanopore and field-effect sensors have two essential attributes for single-molecule detection, transistor action in the sensing platform and a very localized region of charge sensitivity in the detector. By providing direct interfaces to the solid-state, much higher bandwidth of detection can be achieved than in fluorescence-based approaches. In addition to improving the fidelity of the electronic interfaces, integrating these sensors with CMOS electronics allows for highly multiplexed arrays and parallelism at least comparable with what is achieved with fluorescence-based approaches but with dramatically smaller and less expensive instrumentation.

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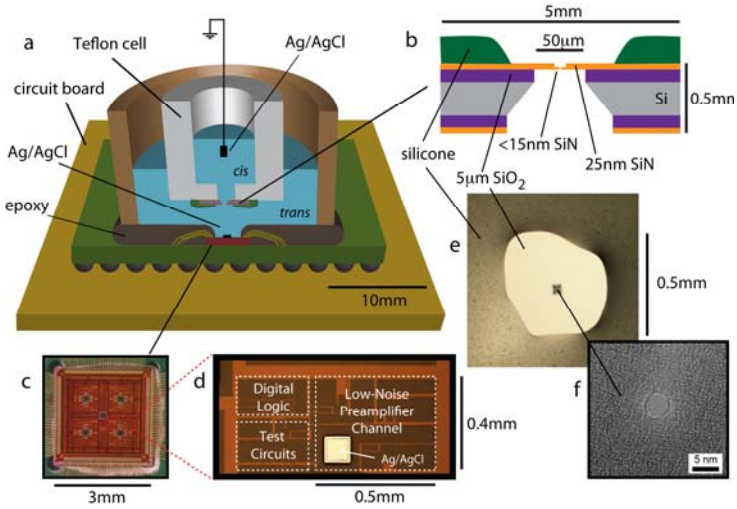

Figure 1. **(a)** Graphical representation of the compact nanopore measurement platform. **(b)** an illustrated cross-section of the low-capacitance thin membrane chip **(c)** optical micrograph of the 8-channel CMOS voltage-clamp current preamplifier **(d)** a magnified image of one preamplifier channel **(e)** an optical image of a solid-state silicon nitride membrane chip mounted in the fluid cell **(f)** a TEM image of a 4nm-diameter nanopore

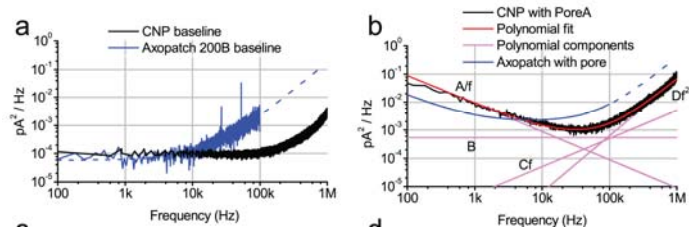

Figure 1. Current noise spectra for nanopores. (a) Input-referred open headstage current noise spectrum for integrated nanopore. Also shown is the measured open-headstage of an Axopatch 200B. (b) Measured noise floor of the integrated amplifier together with a solid-state nanopore.

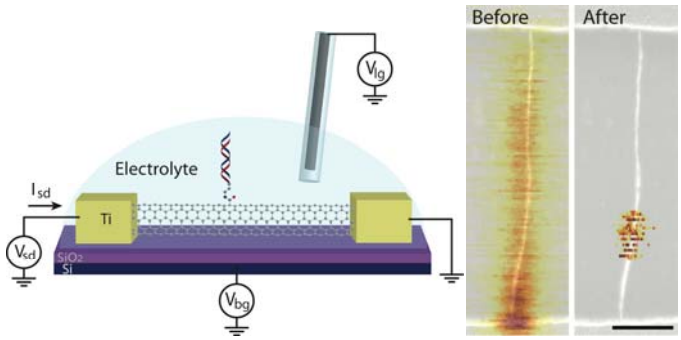

Figure 4. Carbon nanotube FET system illustration and (b) scanning gate microscopy images before and after oxidation

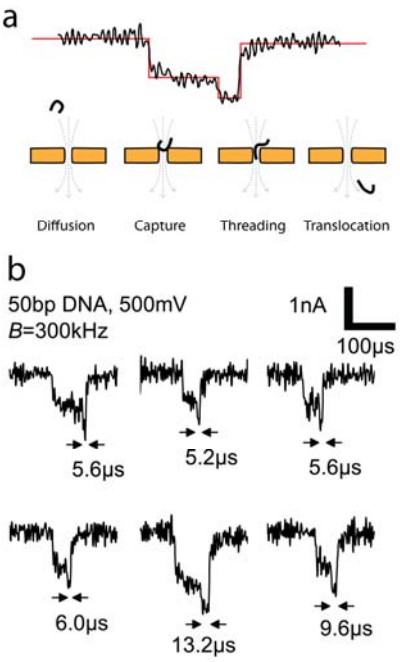

Figure 3. A presentation of intra-event structure observed with short oligomers and small nanopores. (a) An illustration of the sequential processes of nanopore translocation. First a molecule diffuses near the pore, where it is captured by the electric field. The molecule is trapped at the mouth of the pore until it finds a conformation which allows one of its ends to thread through the pore. (b) Typical signals observed for 50bp dsDNA fragments. The events have a characteristic shallow level followed by a deeper tail.

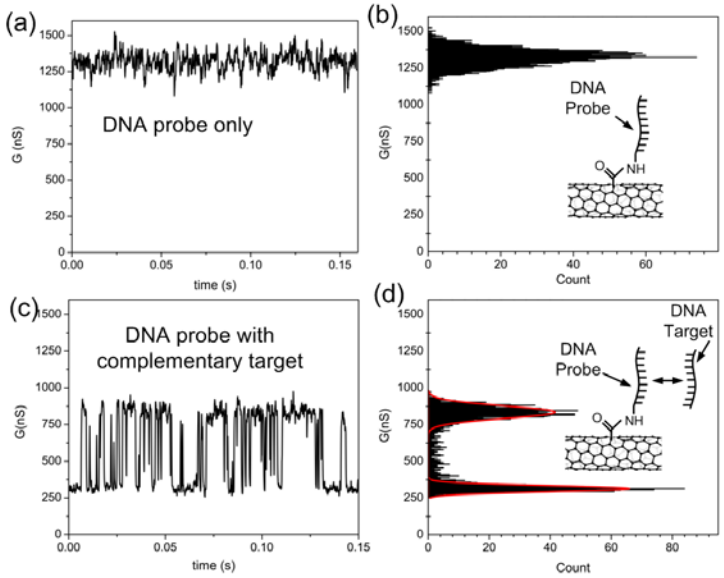

Figure 5. Carbon nanotube FET time-domain measurements showing the two-level response to single-molecule hybridizations

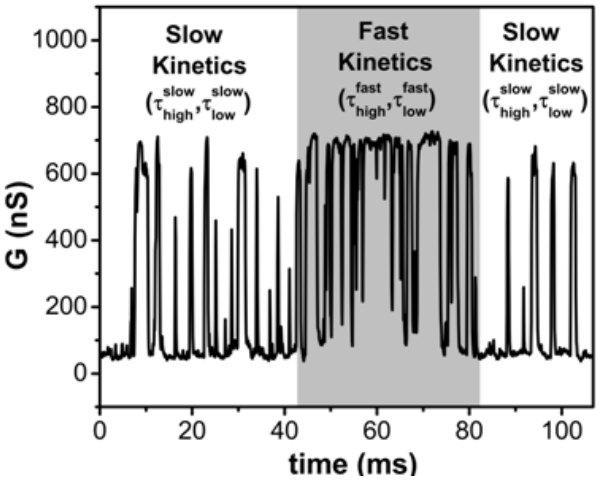

Figure 6. Dynamic disorder observed with carbon nanotube transducers.

Advanced Device Technologies for Defense Systems

John C. Zolper
Vice President, Research and Development
Raytheon Company

Abstract: The performance requirements of defense systems to detect small signals in the presence of clutter or large interferers, to see further than the adversary, and discriminate between targets in a complex environment, has driven the need for ever more capable device technologies for focal plane arrays (FPAs) and monolithic microwave integrated circuits (MMICs). This paper discusses the history, and current state, of several key technologies developed at Raytheon to enable our systems to meet mission needs. The technologies include Gallium Nitride (GaN) MMICs and Mercury Cadmium Telluride (MCT) Infrared Focal Plane Arrays (FPAs). Emerging technologies for heterogeneous integration and Short Wave Infrared (SWIR) FPAs are also discussed.

Background:

There is a long history of defense system requirements driving semiconductor technology development. Examples include the development of silicon Complementary Metal Oxide Semiconductor (CMOS) integrated circuit design and fabrication under the Very High Speed Integrated Circuit (VHSIC) program,[1] the production of GaAs MMICs for solid state radars[2] and the investment in a wide range of infrared FPA technologies for military imaging. These developments, and many others, spanning from fundamental materials growth and characterization, to device design and processing, to module integration, to system demonstrations and production, have resulted in a breadth of technical expertise across the defense industry. In many cases, the technologies initially developed for defense applications also resulted in commercial products whose market size often dwarfed the original defense market. While some of these technology developments can be traced back 30 or 40 years, the pace of technology maturation has increased, partly by leveraging the knowledge based from previous developments and the advancements across the semiconductor industry.

GaN MMICs:

GaN, considered the “third generation of electronic materials”, after silicon and GaAs/InP, is poised to revolutionize defense radar, electronic warfare, and communication systems. The fundamental materials properties of GaN, principally its high breakdown field, electron saturated velocity, and good thermal conductivity, were recognized over 20 years ago as attractive for producing transistors for high frequency power amplification. However the lack of a process to grow bulk GaN, owing to the large vapor pressure of nitrogen at suitable growth temperatures, limited the development of GaN devices until the early 1990’s. In the early 1990’s GaN and related materials (InGaN, AlGaN) caught the attention of the semiconductor research community when the first GaN light emitting diode (LED) was reported (Figure 1). These first blue GaN LEDs were grown on sapphire substrates and involved some of the first controlled production of p-type GaN. The market potential of efficient blue, and later UV and white, LEDs sparked an international race to mature the underlying materials and device technology.

The progress in GaN LEDs also re-invigorated the interest in AlGaN/GaN for high frequency transistors with the first microwave GaN power transistor reported in 1996 followed by the first microwave integrated circuit in 1999.[3]

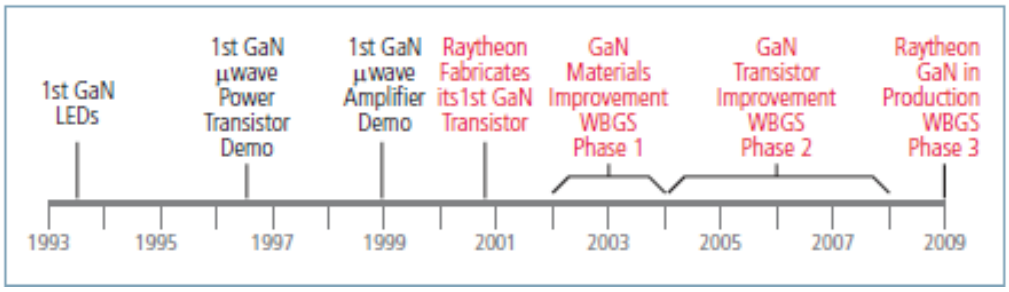

Figure 1: GaN microwave technology development timeline.

While GaN-based LEDs continued to mature and move into commercial production, GaN-based electronics had additional technical challenges to overcome. First among these was the need for better thermal management for high power MMICs. This issue was significantly addressed with the development of SiC semi-insulating substrates and their use for growth of AlGaN/GaN transistors. SiC substrates, with thermal conductivity seven times greater than GaAs, allowed GaN transistors to be demonstrated with record power densities exceeding 10 W/mm^2 and subsequently the first high performance GaN MMIC was realized. In this talk, recent results on GaN MMIC performance and reliability will be presented as well as the extension of the technology to operation at W-band and higher frequencies.[4]

Heterogeneous Integration of Semiconductor Materials and Devices

The ability to closely integrate semiconductor materials and devices on a Si CMOS host opens the door to new circuit performance capabilities to meet requirements for high dynamic range, high bandwidth mix signal circuits. Raytheon is a performer on DARPA's Compound Semiconductor Materials On Silicon (COSMOS) program whose goal is to enable a new class of mixed signal circuits by integrating high speed InP Heterojunction Bipolar Transistors (HBTs) with Si CMOS control electronics. The close integration of high breakdown voltage, high switching speed InP HBTs with high transistor count CMOS, enables increased dynamic range and bandwidth of mixed signal circuits. Digital-to-analog converters have been designed and built to achieve a low power dissipation (<2.5W), high resolution (14 bit, > 78 dB spur free dynamic range (SFDR) based in a COSMOS (InP HBT plus Si CMOS) technology.

Current work is looking at extending the materials and device types that can be integrated with Si CMOS to include GaN and InP High Electron Mobility Transistors (HEMTs). Integration of GaN HEMTs will enable on-chip linearization and self-calibration for rf systems.[5] Integration of InP HEMT will enable receivers with increased functionality and linearity through dynamic, on-chip, control.

Mercury Cadmium Telluride FPAs

Mercury Cadmium Telluride, HgCdTe or MCT, is another example of a long journey from early research discoveries to advanced device technologies, in this case infrared focal plane arrays[6]. Research and development of the MCT alloy system for 8-12 μm IR sensors was started in 1965 at the Santa Barbara Research Center, then a subsidiary of the Hughes Aircraft Company (HAC) and now Raytheon Vision Systems (RVS). At that time, the major materials for IR sensing were PbS for the 1-3 μm range, PbSe and InSb for the 3-5 μm range, and doped Germanium (Ge:Au, Ge:Hg and Ge:Cu) for longer wavelengths. MCT was attractive because its bandgap and absorption band could be tuned by varying its composition. Initial work focused on a $Hg_{(1-x)}Cd_{(x)}Te$ alloy with 20% cadmium (x = 0.2) to address the 8-12 μm wavelength band. Bulk MCT crystals were initially grown in close quartz ampoules where a critical challenge was dealing with the high Hg vapor pressure.

Over the course of many years, advances in bulk and epitaxial layer growth of MCT, coupled with advances in device design and processing, enabled several generations of leading edge IR FPAs. These advances included: Vertical Liquid Phase Epitaxy (VLPE) from large Hg melts, CdZnTe lattice matching substrates, junction formation with a Double Layer Heterojunctions (DLHJ) p-on-n design, mesa structures with CdTe passivation on side walls, backside illumination of arrays, In bump bonding to Read Out Integrated Circuits (ROIC), and Molecular Beam Epitaxy (MBE) on large area alternate substrates such as silicon (see ref 6). This work has led to the steady progress in MCT FPAs shown in Figure 2.

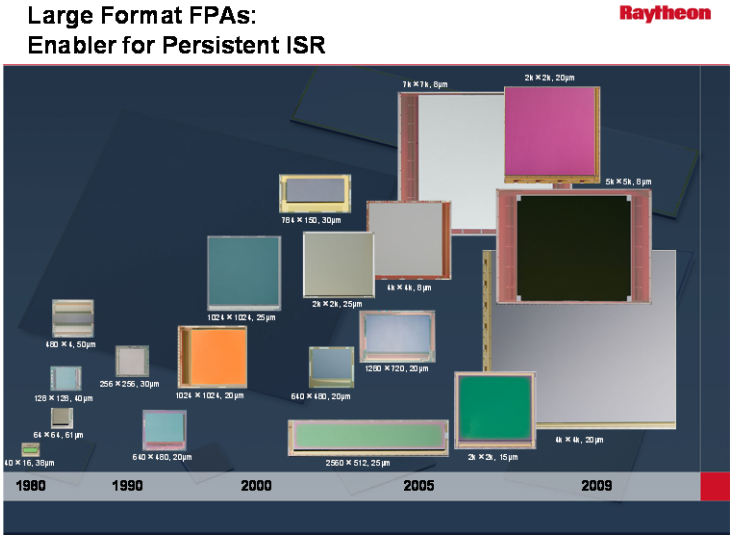

Figure 2: Progression of MCT Focal Plane Arrays.

Alternative IR Materials and Detectors:

While MCT has been the dominant material used for IR FPAs, extensive work has been done to develop alternative approaches to lower cost, increase operating temperature, or improve detector performance. Over the past several years, InGaAs detectors have

attracted significant interest for the Short Wave IR (SWIR) band from 1 to 3 micron as the understanding of the SWIR imaging phenomenology has increased.[7] Integrating low noise detectors with ultra-low noise read out electronics has enabled the detection of signal photons. Gating the read-out has further enhanced the overall image dynamic range.

Conclusion:

Semiconductor device technologies have played, and will continue to play, a critical role in defense sensing systems from radar to imagers. These technologies are continuing to be advanced to address emerging mission needs and can be expected to find their way into the commercial market as new uses are identified.

Acknowledgements: The information presented here is the work of a large group of dedicated engineers and scientists at Raytheon Company. Special thanks are due to P. R. Bratt, S. M. Johnson, D. R. Rhiger, T. Tung, M. H. KalisherW. A. Radford, G. A. Garwood, and C. A. Cockrum, Stefan Baur, Kevin Pettijohn, Michael Jack, Colin Whelan, Tom Kazior, Nick Kolias, Steve Brierley, and Mike Adlerstein, Ken Brown, and Andrew Brown.

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Session II.A (Dean's Hall I)

MEMs, SENSORS and HARVESTORS

Monday PM, June 18th, 2012

Session Chair(s): Ioannis Kymissis, Columbia University and Yongtaek Hong, Seoul National University

1:30 PM II.A-1 Invited Paper
High performance miniaturized NEMS sensors Toward co-integration with CMOS?
T. Ernst, J. Arcamone, J. Philippe, O. Martin, E. Ollier, P. Batude, V. Gouttenoire, C. Marcoux, F. Ricoul, C. Dupré, E. Colinet, O. Rozeau, G. Billiot, and L. Duraffourg, CEA, LETI, MINATEC Campus, Grenoble, FRANCE

2:10 PM II.A-2 Invited Paper
Silicon Monolithic MEMS + Photonic Systems
S. A. Bhave, OxideMEMS Lab, Cornell University, Ithaca, New York, USA

2:50 PM II.A-3 Paper
Highly Sensitive III-V Nitride Based Piezoresistive Microcantilever Using Embedded AlGaN/GaN HFET as Ultrasonic Detector
A. Talukdar[1], M. Qazi[2], and G. Koley[1], [1]University of South Carolina, Columbia, South Carolina, USA and [2]Intel Corp., Portland, Oregon, USA

3:10 PM Break

3:30 PM II.A-5 Invited Paper
Nanostructured thermoelectric energy conversion and refrigeration devices
A. Shakouri, Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana, USA

4:10 PM II.A-6 Invited Paper
Piezotronics and Piezo-phototronics
Z. L. Wang, School of Materials Science and Engineering, Georgia Institute of Technology, Atlanta, Georgia, USA

4:50 PM II.A-7
Late News

High performance miniaturized NEMS sensors Toward co-integration with CMOS?

T. Ernst, J. Arcamone, J. Philippe, O. Martin, E. Ollier, P. Batude, V. Gouttenoire, C. Marcoux, F. Ricoul, C. Dupré, E. Colinet, O. Rozeau, G. Billiot, and L. Duraffourg
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In this paper, we will present some possible emerging applications for Nano-Electro-Mechanical Systems (NEMS) and the interest of their co-integration with CMOS. We will compare some integration schemes and present mass sensing as a possible emerging application. In particular, experimental results on complex gas measurements with NEMS will be introduced. We will show that multi-physics simulations and compact modelling of NEMS components (including chemical and physical effects) can be efficiently used in circuit simulations standard tools for such system optimization.

NEMS devices open new opportunities for integrated solutions in emerging domains as autonomous, highly sensitive, or highly dense sensors. Up to now, the developments of MEMS and CMOS follow parallel paths with their own guidelines. Whereas CMOS technologies benefit from an economy of scale by miniaturisation and the development of generic solutions for a wide range of applications, MEMS look condemned to one technology per application. Moreover, the technical (and economical) interest of their co-integration with CMOS is still not clear.

On the other hand, some NEMS structures find their figure of merit (as sensitivity & frequency of operation) increased while reducing their dimension. With their critical dimensions ranging between 10 and 100 nm, those devices can be made at the VLSI scale. Moreover, their co-integration with a local CMOS amplification increases drastically their sensitivity (Fig 1, [1]). This is particularity true for electro-mechanical resonators used for mass sensing [2]. To follow their resonance frequency variation due to a mass adsorption, the nano-system is embedded in a closed loop [3] that can be either a phase-locked loop (PLL) or a self-oscillating loop (Fig. 2, [4])

For gas analysis, a heterogeneous integrated solution is proposed (Fig. 3, [5]). It includes a miniaturized pre-analytical module, namely a gas chromatography micro-column, for gas separation, NEMS sensors and an off-chip readout electronics for real-time tracking of the resonance frequency according to a PLL scheme. The adsorbed mass on the suspended beam induces a shift of its resonant frequency that is continuously measured. Fig. 4 sums up the fully-integrated NEMS CMOS performance and gives a comparison with state-of-the-art works. The measured CMOS-NEMS resonator offers a mass sensitivity nearly 1000-times better than the other fully-integrated structures making such NEMS very attractive for ultra sensitive mass sensing applications, as illustrated in Fig. 5.

NEMS-CMOS co-integration has already been implemented but for NEMS/MEMS made from an aluminium or a poly-silicon layer [6, 7]. The use of more advanced CMOS lithography enables to define and release very small and sensitive structures (about 40nm for piezoresistive gauges). We proved this concept on thin CMOS SOI technologies where the Si crystalline film is used both for CMOS and sensors. We reported ultra-scaled single-crystal Si NEMS resonators operating in the 100MHz frequency range. Their first monolithic integration at the front-end level with CMOS enables to extract the signal from the background (Fig.6) thanks to reduced losses and local amplification leading to a possible implementation of a direct measurement, for high-sensitivity sensing applications and portable systems [8]. The VLSI environment provides moreover an opportunity to build large dense NEMS array for ultra fast and high performance mass sensing [9].

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Acknowledgement This work was supported by the FP7 European Projects ERC DELPHINS and NEMSIC.

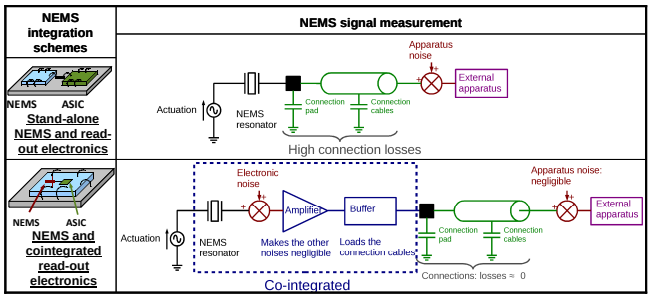

Fig. 1. Stand-alone NEMS suffer from high connection losses due to pad and cables capacitances. These losses are strongly reduced when the NEMS is cointegrated with a CMOS.

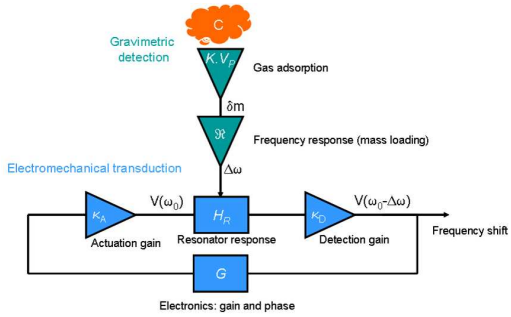

Fig. 2. General schematic of a gravimetric sensor based on frequency shift detection

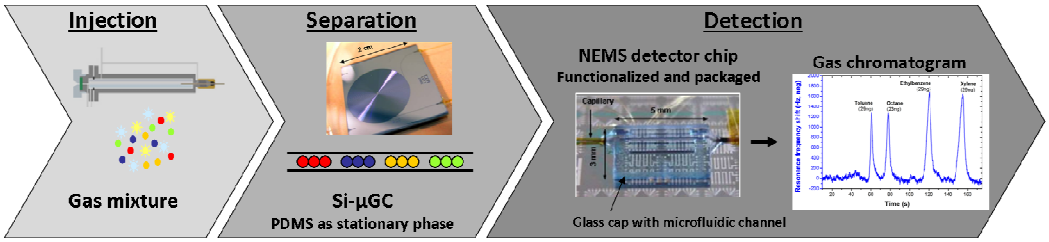

Fig. 3. Schematic representation of a multi-gas analyzer associating a silicon µGC and NEMS detectors. The all detection chain is simulated thanks to a multi-physics analytical model that can be used for the all system optimization

	[6]	[7]	**This work [8]**
Vibrating beam dimensions length × width x thickness	10×1×1 µm³	14×0.26×0.5 8 µm³	**1.2×0.08×0.030 µm³**
NEMS resonance frequency	≈60 MHz	≈1.5 MHz	**≈100 MHz**
Mass sensitivity $S = \frac{df}{dm} = \frac{f_0}{2M_{eff}}$	≈1.8Hz/ag	≈0.2Hz/ag	**≈1200Hz/ag**
NEMS material	Aluminum	Polysilicon	**Single-crystal silicon**
NEMS quality factor	30	NA	**100**
Measurement conditions	Atmospheric pressure	Atmospheric pressure	**Atmospheric pressure**
Actuation DC voltage	50-90 V	10-20 V	**5-10V**
NEMS-CMOS pixel area	NA	0.32 mm²	**30×30 µm²**

Fig. 4. Comparison of different NEMS fully-integrated with their CMOS circuitry

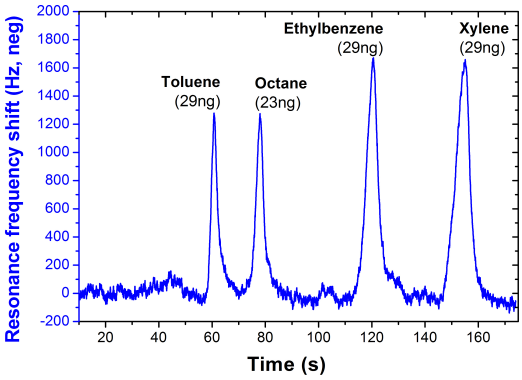

Fig. 5. Chromatogram obtained with a GC+NEMS gas sensor: the NEMS is placed behind a miniaturized 1m long silicon µGC (Fig.3).

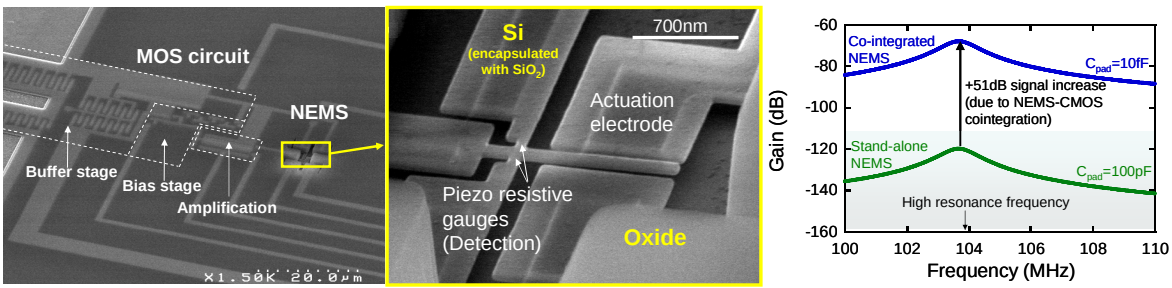

Fig. 6. Left: Tilted SEM pictures showing co-integration of NEMS with CMOS. This has been obtained from the same single Si crystal layer to benefit from enhanced performances of NEMS and to avoid a high background level due to the pad capacitances. Right: Calculated S12 parameter vs frequency. The stand-alone NEMS output signal is not measurable while co-integrated NEMS is.

Silicon Monolithic MEMS + Photonic Systems

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Opto-mechanical systems offer one of the most sensitive methods for detecting mechanical motion using shifts in the optical resonance frequency of the optomechanical resonator. Presently, these systems are used for measuring mechanical thermal noise displacement or mechanical motion actuated by optical forces. Meanwhile, electrostatic capacitive actuation and detection is the main transduction scheme used in RF MEMS resonators. The use of electrostatics is convenient as it allows direct integration with electronics used for processing the RF signals.

In this presentation, I will introduce a method for actuating an opto-mechanical resonator using electrostatic forces and sensing of mechanical motion by using the optical intensity modulation at the output of an optomechanical resonator, integrated into a monolithic system fabricated on a silicon-on-insulator (SOI) platform. I will discuss new applications enabled by this hybrid system including opto-acoustic oscillators [1-3] and opto-mechanical accelerometers [4].

[1] Suresh Sridaran and Sunil A. Bhave, "Opto-acoustic oscillator using silicon MEMS optical modulator," 16th International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers'11), Beijing, China, June 5-9, 2011, pp. 2920-2923.

[2] Siddharth Tallur, Suresh Sridaran and Sunil A. Bhave, "A silicon nitride optomechanical oscillator with zero flicker noise," 25th IEEE International Conference on Micro Electro Mechanical Systems (MEMS 2012), Paris, France, January 29-Feb 2, 2012, pp. 19-22.

[3] Suresh Sridaran and Sunil A. Bhave, "1.12 GHz opto-acoustic oscillator," 25th IEEE International Conference on Micro Electro Mechanical Systems (MEMS 2012), Paris, France, January 29-Feb 2, 2012, pp. 644-647.

[4] David N. Hutchison and Sunil A. Bhave, "Z-axis optomechanical accelerometer," 25th IEEE International Conference on Micro Electro Mechanical Systems (MEMS 2012), Paris, France, January 29-Feb 2, 2012, pp. 615-619.

HIGHLY SENSITIVE III-V NITRIDE BASED PIEZORESISTIVE MICROCANTILEVER USING EMBEDDED AlGaN/GaN HFET AS ULTRASONIC DETECTOR

Abdul Talukdar[1], Muhammad Qazi[2], and Goutam Koley[1]
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We report, for the first time, an ultra high gauge factor of more than 3500 observed using AlGaN/GaN Heterostructure Field Effect Transistor (HFET) embedded GaN piezoresistive microcantilever. In addition, the deflection transduction signal from the HFET was utilized to determine dynamic bending as well as AC frequency response of the cantilever. Finally, the piezoresistive microcantilver was used to detect very small acoustic pressure waves generated by a piezo chip oscillated at sub nm amplitude at the resonance frequency of the cantilever positioned 1 cm away, highlighting the utility of these cantilevers as highly sensitive ultrasonic transducers.

FET embedded microcantilevers are ideal for developing integrated electronic detection platform for biological and chemical analytes. GaN microcantilever with integrated AlGaN/GaN HFET deflection transducer offers very high mechanical, thermal, and chemical stability, in addition to extraordinary deflection sensitivity due to its strong piezoelectric properties. The piezoelectric property of III-V Nitrides causes a highly mobile (>1500 cm^2/Vs) two dimensional electron gas (2DEG) to form at the AlGaN/GaN interface, which gets strongly affected by the deflection induced strain. In addition, the electron mobility also changes due to the change in effective mass. The combined changes in 2DEG and mobility offer very high deflection sensitivity, verified through COMSOL finite element simulations and experimental observations. The effect of mechanical strain caused by microcantilever bending on the 2DEG and the AlGaN/GaN HFET characteristics has been reported experimentally [1] and theoretically [2] earlier, but this for the first time we have obtained such a high Gauge Factor.

Microcantilevers were fabricated using III-V Nitride layers on Si(111). The layer structure consisted of i-GaN (2 nm)/AlGaN (17.5 nm, 26% Al)/i-GaN (1 µm)/Transition layer (1.1 µm)/Si (111) substrate (500 µm). Fig. 1 (a) shows the SEM image of the fabricated device with the HFET shown in the inset. The HFET was fabricated with initial 200 nm mesa etching, followed by Ti(20 nm)/Al(100 nm)/Ti(45 nm)/Au(55 nm) metal stack deposition and rapid thermal annealing for ohmic contact formation. For gate contact, Ni(25 nm)/Au(375 nm) Schottky barrier was used. The fabricated microcantilever dimension is 350×50×2 µm. The GaN cantilever pattern was etched down using Cl_2 based inductively coupled plasma etch process.

Fig. 1 (b) shows the schematics of the experimental setup using our wire bonded device (shown as inset in Fig. 2) and Nanopositioner's (PI-611 Z). Fig. 2 shows the I_d-V_d characteristics of one of our best devices for different gate bias. In Fig. 3 the static bending performance is shown where the drain current is found to change by 6.3 % in magnitude, which gives a gauge factor of 3532. Both the downward and upward bending of cantilever exhibited similar changes. The movement of the nanopositioner was controlled using a Labview program, which was modified to also perform low frequency dynamic bending (up to 40 Hz). Fig. 4 shows the low frequency (0.5 Hz) response of a more typical device when the bending magnitude (both downward and upward) was 25 µm. We found that the low frequency upward and downward bending does not alter the gauge factor, and the response up to 40 Hz is also quite similar. We previously reported [3] a gauge factor of -38 (at V_g=0 V) and -860 in steady state and transient conditions, respectively. But our second generation devices consistently exhibit much higher gauge factor in both static and dynamic bending conditions at zero gate bias. We also extracted the AC response of the cantilevers using a miniature peizo actuator (PL055.31 from PI) and a lock-in amplifier (SR 850). The ac response of the microcantilever, determined from direct contact oscillation of the piezo chip revealed a resonant peak of the cantilever at 45 KHz (Fig. 5) and a high quality factor of more than 200. The piezo chip was also used as an ultrasonic source and our microcantilever sensor was able to detect sub nm vibrational amplitude of the piezo chip from a distance of 1 cm. These results highlight the possibility of using III-V Nitride based piezoresistive microcantilevers as highly sensitive ultrasonic sensor for harsh environment, with wide ranging applications in acoustic spectroscopy and imaging.

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2. M. Chu et al., *J. Appl. Phys.* 108(10), p. 104502 (2010).
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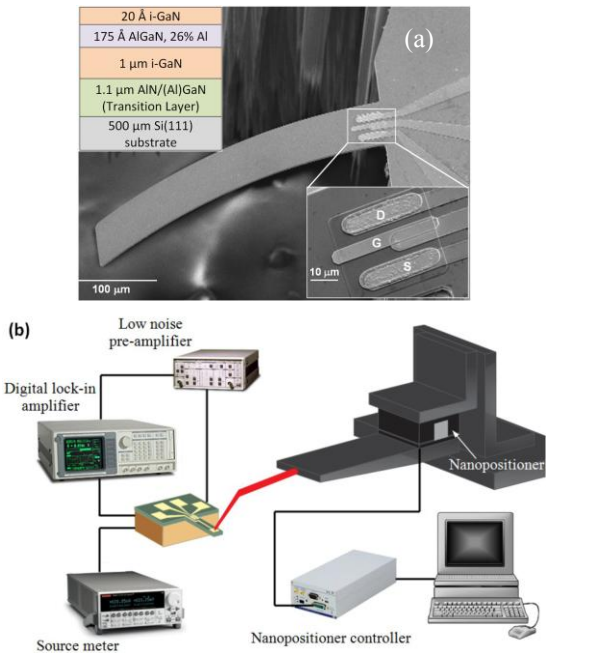

Figure 1: (a) SEM image of GaN microcantilever with embedded AlGaN/GaN HFET at the base. Top inset shows the layer structure of the wafer. Bottom inset shows the magnified image of the AlGaN/GaN HFET. The source drain length, L_{DS} = 17 µm, the channel width, W_{ch} = 29 µm, and the gate length, L_G = 6 µm. (b) Schematics of the experimental setup.

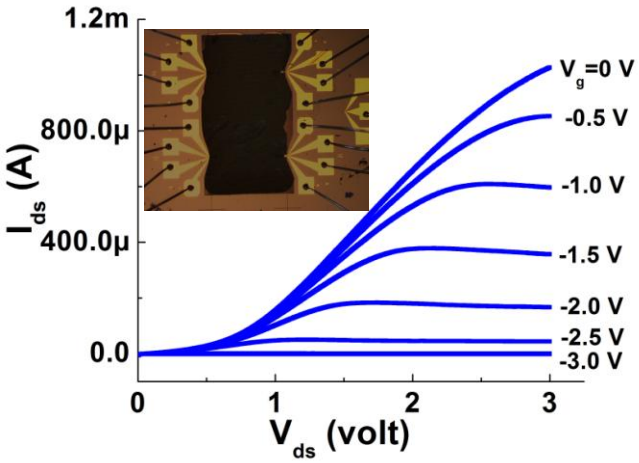

Figure 2. I_d-V_d curve for an HEFT device integrated at the cantilever base. Inset shows the top view of a wire-bonded sensor chip with 4 microcantilevers.

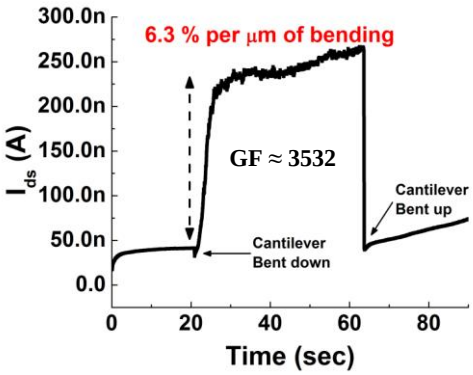

Figure 3. Static bending response when cantilever is bent by 75 µm downward or upward.

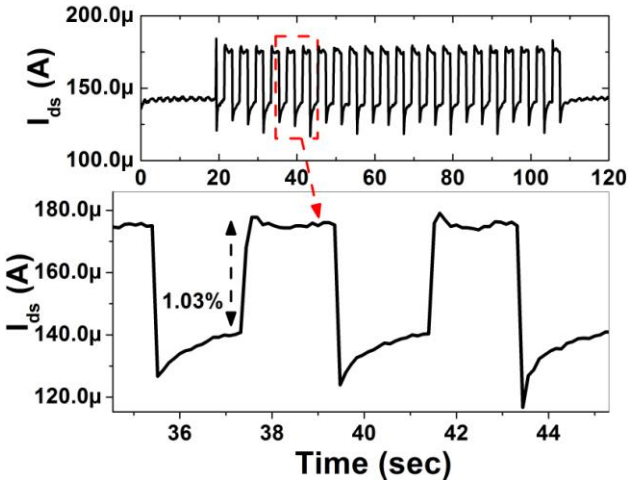

Figure 4. Static bending response when cantilever is bended (both downward and upward) 25 µm and 0.5 Hz frequency.

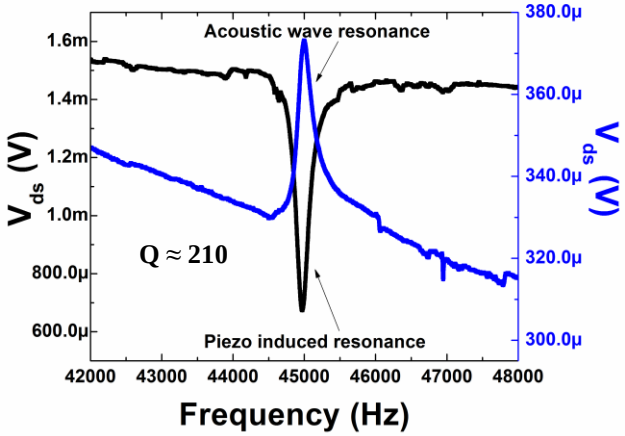

Figure 5. Resonant peaks for both Piezo induced and acoustic wave induced resonance observed in the AC response of the microcantilever.

Nanostructured thermoelectric energy conversion and refrigeration devices

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Birck Nanotechnology Center
Purdue University, West Lafayette, IN

Energy consumption in our society is increasing rapidly. A significant fraction of the energy is lost in the form of heat. In this talk we introduce thermoelectric devices that allow direct conversion of heat into electricity. A key requirement to improve the efficiency is to increase the Seebeck coefficient (S) and the electrical conductivity (σ) while reducing the electronic and lattice contributions to thermal conductivity ($\kappa_e+\kappa_L$). Some new physical concepts and nanostructures make it possible to modify the trade-offs between the bulk material properties through the changes in the density of states, scattering rates and interface effects on the electron and phonon transport. We will review recent experimental and theoretical results on nanostructured materials of various dimensions: superlattices, nanowires, nanodots, as well as solid-state thermionic power generation devices [1]. Most of the recent success has been in the reduction of lattice thermal conductivity while maintaining good electrical conductivity. Several theoretical and experimental results to improve the thermoelectric power factor ($S^2\sigma$) and reduce Lorenz number (σ/κ_e) are presented. Novel metal-semiconductor nanocomposites are developed where the heat and charge transport are modified at the atomic level. Theory and experiment are compared for several III-V and nitride nanocomposites and multilayers [2]. Potential to increase the energy conversion efficiency and bring the cost down to $0.1-0.2/W will be discussed [3]. We also describe how similar principles can be used to make micro refrigerators with cooling power densities exceeding 500 watts per centimeter square [4] in order to selectively remove dynamic hot spots and decrease significantly the requirements for overall cooling of the chip. We also describe some recent advances in nanoscale thermal characterization. Thermoreflectance imaging is used to measure the transient temperature distribution in power transistors. Resolution down to 100ns in time, submicron spatial and 0.1C in temperature are achieved using megapixel CCDs. Finally, the transition between energy and entropy transport in nanoscale devices will be briefly discussed.

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[3] K. Yazawa and A. Shakouri, "Optimizing Cost-efficiency Trade-offs in the Design of Thermoelectric Power Generators," Environmental Science and Technology, July 2011.
[4] A. Shakouri, "Nanoscale Thermal Transport and Microrefrigerators on a Chip", Proceedings of IEEE, August 2006.

Piezotronics and Piezo-phototronics

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Piezoelectricity, a phenomenon known for centuries, is an effect that is about the production of electrical potential in a substance as the pressure on it changes. The most well known material that has piezoelectric effect is the provskite structured Pb(Zr, Ti)O_3 (PZT), which has found huge applications in electromechanical sensors, actuators and energy generators. But PZT is an electric insulator and it is less useful for building electronic devices. Wurtzite structures, such as ZnO, GaN, InN and ZnS, also have piezoelectric properties but they are not extensively used as much as PZT in piezoelectric sensors and actuators due to their small piezoelectric coefficients. In fact, due to the polarization of ions in a crystal that has non-central symmetry, a piezoelectric potential *(piezopotential)* is created in the crystal by applying a stress. For materials such as ZnO, GaN, InN in the wurtzite structure family, the effect of piezopotential to the transport behavior of charge carriers is significant due to their multiple functionalities of piezoelectricity, semiconductor and photon excitation. By utilizing the advantages offered by these properties, a few new fields have been created. Electronics fabricated by using inner-crystal piezopotential as a "gate" voltage to tune/control the charge transport behavior is named *piezotronics*, with applications in strain/force/pressure triggered/controlled electronic devices, sensors and logic units. *Piezo-phototronic effect* is a result of three-way coupling among piezoelectricity, photonic excitation and semiconductor transport, which allows tuning and controlling of electro-optical processes by strain induced piezopotential. The objective of this talk is to introduce the fundamentals of piezotronics and piezo-phototronics and to give an updated progress about their applications in energy science (LED, solar cell), electronics and sensors.

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[3] W.Z. Wu, Y.G. Wei and Z.L. Wang, *Adv. Materials*, 22 (2010) 4711.
[4] W.Z. Wu, Y.G. Wei and Z.L. Wang, *Nano Letters*, 11 (2011) 2779
[5] Y.F. Hu, Y.L. Chang, P. Fei, R.L. Snyder and Z.L. Wang, *ACS Nano*, *4* (2010) 1234.
[6] Q. Yang, X. Guo, W.H. Wang, Y. Zhang, S. Xu, D.H. Lien, Z.L. Wang, *ACS Nano*, 4 (2010) 6285.
[7] Q. Yang, W.H. Wang, S. Xu, Z.L. Wang, *Nano Letters*, dx.doi.org/10.1021/nl202619d.
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[9] Personal website: www.nanoscience.gatech.edu

Session II.B (Dean's Hall II)

Alternate Transistor Concept

Monday PM, June 18th, 2012

Session Chair(s): Sayeef Salauddin, University of California, Berkeley and Siyu Koswatta, IBM

1:30 PM II.B-1 Invited Paper
Novel Double Layer Graphene Transistors-Bilayer Pseudospin FETs and 2D-2D Tunnel FETs
S. K. Banerjee[1], L. F. Register[1], E. Tutuc[1], D. Reddy[1], S. Kim[1], D. Basu[1], C. Corbet[1], L. Colombo[2], G. Carpenter[3] and A. H. MacDonald[1], [1]University of Texas at Austin,[2]Texas Instruments, Incorporated, Dallas, Texas, USA, and [3]IBM Research, Austin, Texas, USA

2:10 PM II.B-2
Effect of Interfacial Phonon-Plasmon Modes on Electrical Transport in Supported Graphene
Z.-Y. Ong and M. V. Fischetti, Department of Materials Science and Engineering, University of Texas at Dallas, Richardson, Texas, USA

2:30 PM II.B-3
Possible Applications of Topological Insulator Thin Films for Tunnel FETs
J. Chang, L. F. Register, and S. K. Banerjee, Microelectronics Research Center, The University of Texas at Austin, Austin, Texas, USA

2:50 PM II.B-4
SymFET: A Proposed Symmetric Graphene Tunneling Field Effect Transistor
P. Zhao[1], R. M. Feenstra[2], G. Gu[3] and D. Jena[1], [1]Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA, [2]Dept. Physics, Carnegie Mellon University, Pittsburgh, Pennsylvania, USA and [3]Dept. Electrical Engineering and Computer Science, University of Tennessee, Knoxville, Tennessee, USA

3:10 PM Break

3:30 PM II.B-5 Invited Paper
Hybrid straintronics and spintronics: An ultra energy-efficient paradigm for logic and memory
S. Bandyopadhyay[1] and J. Atulasimha[2], [1]Department of Electrical and Computer Engineering and [2]Department of Mechanical and Nuclear Engineering, Virginia Commonwealth University, Richmond, Virginia, USA

4:10 PM II.B-6 Invited Paper
Graphene and Topological Insulator Based Transistors: Beyond Computing Applications
Y. P. Chen, Department of Physics and Birck Nanotechnology Center and School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana, USA

4:50 PM II.B-7
Late News

Novel Double Layer Graphene Transistors- Bilayer Pseudospin FETs and 2D-2D Tunnel FETs

S.K. Banerjee, L.F. Register, E.Tutuc, D.Reddy, S.Kim, D.Basu, C.Corbet,
L. Colombo[*], G. Carpenter[#] and A.H. MacDonald
University of Texas at Austin, [*]TI, [#]IBM

The semiconductor industry is placing increasing emphasis on emerging materials and devices that may provide solutions to end-of-the-CMOS-roadmap problems beyond 2020 [Table 1]. The remarkable electronic properties of graphene can lead to novel beyond-CMOS logic device concepts, such as the Bilayer pseudoSpin FET (BiSFET), which can potentially be an ultra-low power replacement for the MOSFET [1]. The BiSFET is based on many-body tunneling of an excitonic Bose condensate in double layer graphene [2]. One can also have single particle 2D-to-2D tunneling FETs based on the BiSFET architecture, with similar current-voltage behavior demonstrating negative differential resistance.

Graphene has a single-atom thickness and a symmetric conduction and valence band structure around the Dirac point, with zero bandgap and low bandedge density of states, which combined makes it theoretically attractive for the formation of an excitonic condensate. Recent studies, using the Random Phase Approximation, have shown that this condensate should survive above 300K, even after accounting for dynamic screening of carriers in the graphene double layers system, provided we can have a low-k dielectric environment (~1-2), and an interlayer tunnel dielectric ~1 nm thick.

Figure 1 shows the device structure, equivalent circuit, and model current-voltage characteristics of the BiSFET. SPICE simulations demonstrate that fundamental Boolean gates such as inverters, OR and NAND gates can be implemented with the BiSFET, using a 4-phase clocked power supply, with much lower power dissipation and comparable or faster switching than CMOS [3]. In addition, more complicated circuits such as 4-bit adders, as well as simple memory elements, can be achieved leading to the possibility of both sequential and combinatorial logic. Figure 2 shows the schematic of a BiSFET based inviter and SPICE simulated verification of a one-bit full adder [3].

Experimentally, the BiSFET structure has been fabricated, and tests for the condensate done using Coulomb drag measurements in the double layer graphene system [4]. This measurement technique involves driving current in one graphene layer, and probing a "drag" voltage in the opposite layer, separated by the interlayer dielectric, induced by the momentum transfer due to electron-electron scattering [Fig. 3]. Theory predicts that if a condensate were to form, the drag resistance should jump to a value comparable to the layer resistance. Experimentally the drag resistance reveals two regimes: diffusive drag at elevated temperatures, and mesoscopic fluctuations-dominated drag at low temperatures. The condensate, however, has not been observed so far, but nor should it have been according to the most recent theory, as noted above. Alternative experimental strategies will be discussed to achieve the required low-k environment and thin interlayer dielectric.

The basic BiSFET structure could also be used as 2D-2D single particle tunnel FETs [5]. For the single particle h-h and e-e 2D-2D tunnel FETs, graphene's single-atom thickness could lead to more ideal interlayer tunneling characteristics, provided the layers can be aligned. Single particle tunneling current calculations have been performed which show NDR characteristics, reminiscent of the BiSFET, albeit with higher operating powers as shown in figure 4. Circuit implications will be discussed.

This work was supported by the NRI SWAN program.

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[5] D.Reddy, L.Register, S.Banerjee, "Bilayer Graphene Vertical Tunneling Field Effect Transistor," submitted.

Table 1: Projected performance metrics for "End-of -the roadmap" CMOS Circa 2020

Energy	10 aJ/op
Power	10^7 W/cm^2
Speed	0.1 ps/op (10 THz f_T; 100 GHz circuit)
Size	L_g ~ 5 nm; Cell ~ 100 nm
I_{DN}	3 mA/μm
Density	10^{10} cm^{-2}
BIT	100 Gbit/ns/cm^2
Cost	10^{-12} $/gate

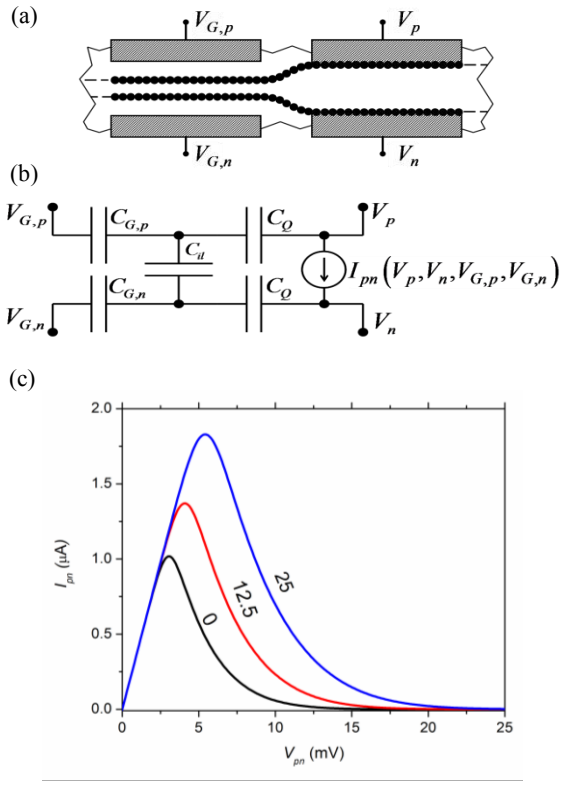

Figure 1 (a) Device schematic of BiSFET, (b) Equivalent circuit model of BiSFET, (c) *I-V* characteristics of BiSFET for three different gate voltages $V_{G,n}$ with $V_{G,p}$ = -25 mV. Note that while the region of condensate formation is indicated schematically in (a) by reduced spacing between layers here, there are others ways to localize the condensate including changes in dielectrics, charge densities, and/or initial degree of charge balance.

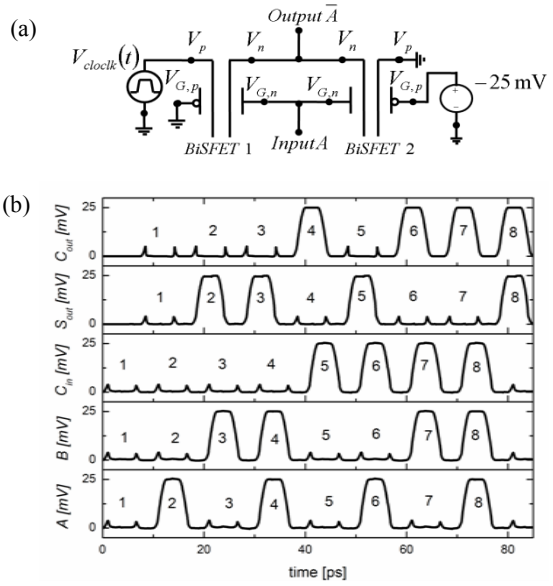

Figure 2 (a) Circuit schematic of BiSFET-based inverter, (b) SPICE simulated verification of 1-bit full adder for 8 different combinations of input bits, A, B and C_{in} giving the output bits, S_{out} and C_{out} (C=carry, S=Sum).

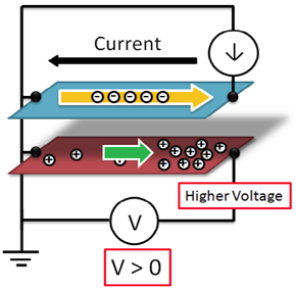

Figure 3 Illustration of Coulomb drag measurement scheme.

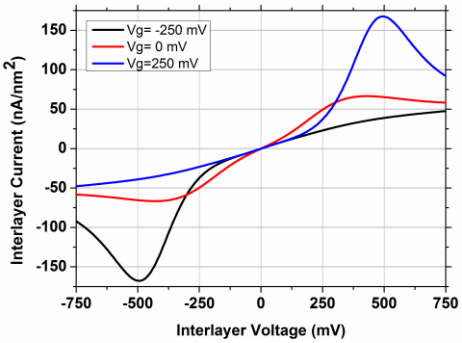

Figure 4 Interlayer tunneling current as a function of interlayer voltage illustrating the negative differential resistance for three different gate voltages split equally with opposite polarity between the gates.

Effect of Interfacial Phonon-Plasmon Modes on Electrical Transport in Supported Graphene

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Introduction: Graphene has been proposed as a candidate material for nanoelectronic applications on account of its excellent electrical transport properties [1]. Although the mobility in suspended graphene can reach up to ~200,000 $cm^2V^{-1}s^{-1}$ [2], the mobility in graphene supported on an insulating dielectric substrate (such as SiO_2) is typically about one order of magnitude lower [1] (~5,000 to 20,000 $cm^2V^{-1}s^{-1}$) due to scattering by charged impurities, surface roughness and surface polar phonon (SPP) modes. Although impurity scattering is the dominant factor limiting electron mobility [3], it can be reduced experimentally. On the other hand, interaction with the SPP modes is intrinsic to the substrate material, and limits the maximum mobility possible. Coupling between the SPP and graphene plasmon modes leads to the formation of interfacial phonon-plasmon (IPP) modes [4] which can also be interpreted as screened SPP modes. Within this theoretical framework, the phenomenon of dynamic screening and *anti-screening* emerges. We compute the IPP dispersion and use the electron-IPP scattering rates for different substrates (SiO_2, h-BN, HfO_2 and Al_2O_3) to calculate the substrate-limited conductivity (σ_{pp}) and field mobility (μ_{pp}) of supported graphene. Contrary to expectations [5-7], HfO_2, a high-κ dielectric, is not any worse than SiO_2.

Results and discussion: The geometry we have considered is depicted in Fig. 1. Graphene is modeled as an infinitely thin sheet floating above a flat semi-infinite substrate. The graphene-substrate gap is taken to be d = 0.0?35 nm. Figure 2 shows the SPP, plasmon and IPP dispersion at $n = 1\times10^{12}$ cm^{-2} for SiO_2. The SPP branches have a flat dispersion while the plasmons have a typically 2-dimensional ($\omega \propto Q^{1/2}$) dispersion. The IPP branches are a mix of the SPP and IPP branches. The corresponding scattering rates (Γ) for the SPP and IPP modes are shown in Fig. 2. The rates due to the IPP branches I and II are lower than the SPP branches because the electron-phonon coupling coefficients (M_Q) are smaller for the IPP modes at large Q. This can be seen in Fig. 4 where we plot $M_Q Q$. The smaller IPP M_Q can be interpreted as the screened SPP M_Q. At small Q, the coupling coefficient is actually larger for the IPP modes than for the SPP modes because the former frequencies are larger than the plasmon frequency, resulting in anti-screening which actually increases the coupling strength.

We compute the σ_{pp} and μ_{pp} for four commonly used dielectrics (SiO_2, h-BN, HfO_2 and Al_2O_3) at different carrier densities (n = 0.25 to 5.0×10^{12} cm^{-2}) at room temperature. Figure 5 shows the conductivity results. For all four dielectrics, the conductivity exhibits a strongly nonlinear behavior, implying the μ_{pp} (see Fig. 6) is carrier density dependent. Although HfO_2 is a high-κ oxide and interaction with its SPP modes is expected to degrade electrical transport, its mobility and conductivity are the highest of the four. This is because its SPP frequencies are small and the IPP modes undergo screening which reduces the coupling strength. Hexagonal BN has the next highest conductivity and mobility because of its SPP modes have high frequencies and are relatively unoccupied. However, the high frequencies lead to anti-screening which enhances the electron-IPP coupling. Al_2O_3 has the lowest conductivity and mobility because of its large dipole moment which leads to a large electron-IPP coupling.

Conclusions: We have computed the dispersion and scattering rates for the IPP modes. Compared to the uncoupled SPP modes, their scattering rates are significantly lower as a result of dynamic screening which emerges from the plasmon-SPP coupling. At small/large Q, dynamic screening enhances/weakens electron-phonon interaction. Despite being a high-κ oxide, HfO_2 seems to show the most promise in terms of IPP scattering according to our conductivity and mobility calculations for SiO_2, h-BN, HfO_2 and Al_2O_3.

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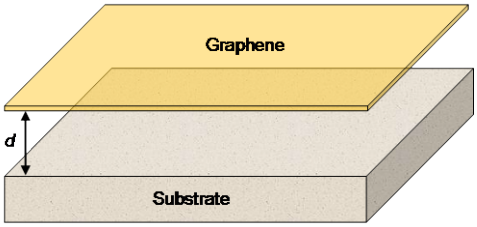

Figure 1: Configuration of graphene supported on a semi-infinite substrate. The graphene-substrate gap is assumed to be d = 0.35 nm.

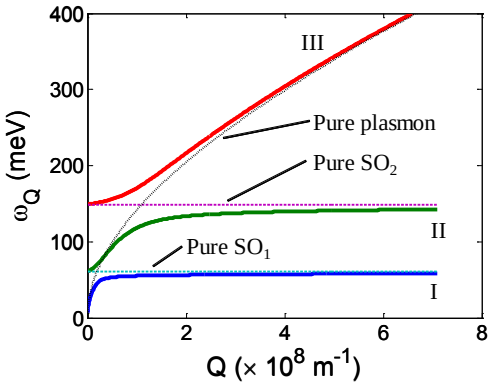

Figure 2: Dispersion of coupled IPP in graphene-on-SiO_2 at $n = 1\times10^{12}$ cm^{-2}. The IPP branches (I to III) are formed from the hybridization of the uncoupled SPP branches (SO_1 and SO_2) and the graphene plasmons. At large Q, branch III becomes plasmon-like while I and II stay phonon-like.

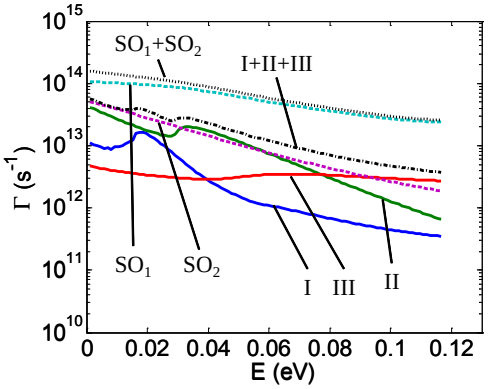

Figure 3: Scattering rates for graphene-on-SiO_2 at $n = 1\times10^{12}$ cm^{-2}. The sum of the SPP scattering rates is several times larger than the sum of the IPP rates.

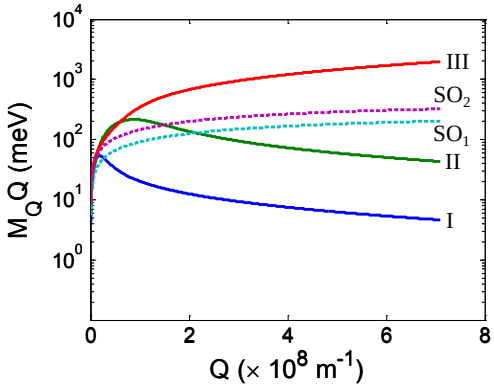

Figure 4: Plot of $M_Q Q$ where M_Q is the electron-IPP coupling coefficient and Q is the wave vector.

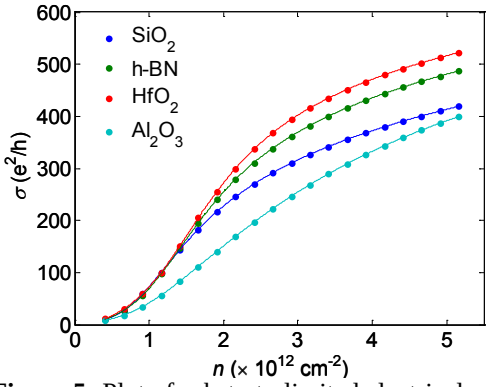

Figure 5: Plot of substrate-limited electrical conductivity. For $n < 1.5\times10^{12}$ cm^{-2}, the conductivities for SiO_2, h-BN and HfO_2 are similar. HfO_2 has the highest conductivity at higher n.

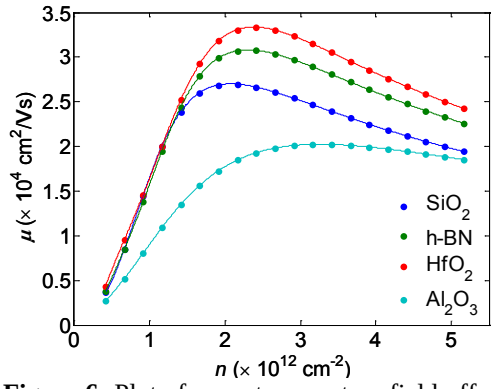

Figure 6: Plot of room temperature field-effect mobility ($\mu_{pp} = \sigma_{pp}/ne$) corresponding to Fig. 5. HfO_2 has the highest mobility.

Possible Applications of Topological Insulator Thin Films for Tunnel FETs

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We have begun to explore the possibility of thin film three dimensional (3D) topological insulator (TI) based tunnel FETs (TFETs), specifically Bi_2Se_3 here, using quantum ballistic transport simulations with a tight-binding Hamiltonian in the atomic orbital basis including spin degrees of freedom. TI-based TFETs would be analogous in some ways to graphene nanoribbon TFETs, but without the sensitivity to ribbon width and edge roughness, and in some ways to narrow gap III-V TFETs but with substantially thinner quantum well widths.

3-D TIs have gained substantial interest recently because of their novel electronic surface states. A 3-D TI is characterized by the presence of protected semi-metallic surface states with the conduction band (CB) and valence band (VB) meeting at a Dirac point, separated by an insulating bulk. Conducting surface states of TI are quite robust to the nonmagnetic disorder but open a gap in the presence of time-reversal symmetry breaking perturbations. However, recent theoretical and experimental studies have shown an induced gap within the surface bands in TI thin films even without magnetic disorders [1]. The gap originates from allowed VB to CB surface states interactions between the opposite surfaces, with a gap size determined by the thin film thickness. This gap opening allows for the possibility of TI-based band-to-band Tunnel FETs (TFETs). In this work, we consider the Bi_2Se_3, one of the most promising TI materials, with tunneling parallel to the surfaces within a p-i-n (source/gated-channel/drain) structure common for many TFET designs.

The building block of the hexagonal bulk Bi_2Se_3 crystal consists of five atomic layers, a "quintuple layer" (QL). A thin film structure can be formed from one up to a stack of several QLs. We consider 1QL (~0.7 nm) and 2QLs (~1.6 nm) thicknesses thin films. Fig. 1(a) and 1(b) show the rectangular unit cell in the top view of a thin film and the corresponding two-dimensional Brillouin Zone (BZ). In this coordinate system, transport is in the *x*-direction, and *z* is normal to the plane of the film. Fig. 1(c) shows the layout of the simulated Bi_2Se_3 TFETs with p-types source, approximately 20 nm long undoped gated channels, and n-type drain. The tight-binding hopping potentials are extracted from density functional calculations using maximally localized wannier functions. Fig. 2(a) and 2(b) show the one-dimensional band structures for the 1QL and 2QLs films, respectively, for transverse modes of $k_y = 0$, where the band gap minimum occurs at the Γ point—which also would be the Dirac point in thicker material—and $k_y = \pi/a_2$ which is the edge of the BZ. The band gaps are 497 and 136 meV for the 1 and 2 QLs thin films, respectively. We use recursive scattering matrices to propagate injected carrier wavefunctions from the source (drain), through the channel, to the drain (source) [2]. Current is calculated by integrating the transmission coefficients over k_x and k_y with a Fermi function weight. At the time of writing, these simulations are not electrostatically self-consistent, nor do we assume specific approaches to doping, chemical or electrostatic, or gating. Rather we consider channel potential shifts and pre-defined transition region lengths between the source and channel and channel and drain regions. Two different transition region lengths, about 2.1 nm and 4.1 nm, are considered.

With positive drain bias, the gating of the intrinsic channel region controls current flow via overlap (ON) or not (OFF) of the channel CB (VB) band with the source VB (drain CB) band. Under these simulation conditions, we find that the larger band gap 1QL film provides more favorable behavior, with a far below 60 mV subthreshold slope and large ON/OFF ratio in these 300 K ballistic simulations and a still potentially approaching MOSFET-like transconductance above threshold, as shown in Fig. 3 for three different drain biases. The Fermi level in the source (drain) are placed about 8 meV below (above) the CB (V) edge to suppress the OFF-state non-tunneling current. Fig. 4 shows the band edge profiles for different potential shifts with V_{DS}=0.3 V, and the corresponding transmission probabilities. With a 0 eV potential shift (red lines in Fig. 4), we have CB-to-VB overlap on the drain side allowing ON-state tunneling. Applying a 0.1 eV potential shift pushes down the entire band and removes the CB-to-VB overlap on drain side. With still more potential shift, the CB-to-VB overlap occurs on the source, turning the device back ON. Results for the 2QL TI film are shown in Fig. 5. The Fermi levels in the source and drain are in the same position relative to the band edges as for the 1QL device. However, due to the smaller band gap, there is a significant amount of non-tunneling OFF-state current, limiting the ON/OFF ratio to about 10~100 depending on drain bias. The corresponding band profiles with a 50 meV potential shift at V_{DS}=0.1 V, and the corresponding current distribution plot for the transverse modes at k_y =0 only are shown in Fig. 6. A higher n-type/p-type doping on the source/drain can reduce the non-tunneling current, but with a slight reduction in allowed peak drain voltage.

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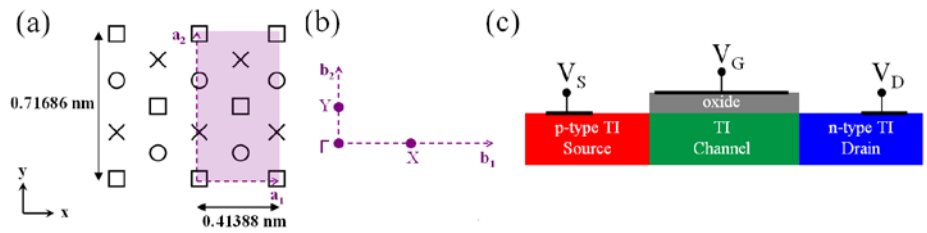

Fig. 1. (a) Top view of Bi_2Se_3 thin film. Three different symbols (○, □ and ×) are for atomic positions in different atomic layers. A Rectangular unit cell is denoted. (b) Two-dimensional rectangular Brillouin Zone (BZ) of Bi_2Se_3 thin film with high symmetry points Γ, X and Y. (c) Schematic structure of a TI (Bi_2Se_3 here) thin film tunnel FET.

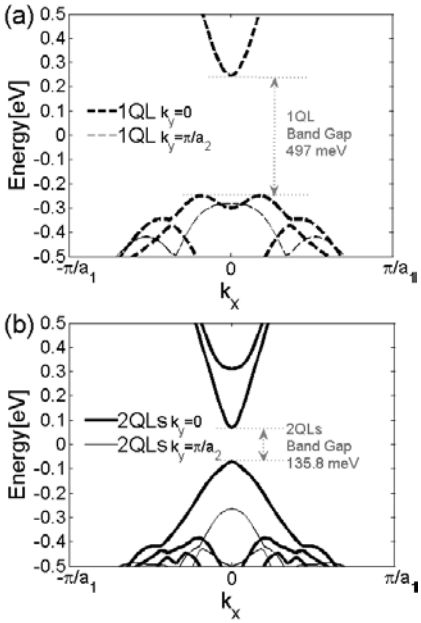

Fig. 2. One-dimensional band structures at two different transverse modes (k_y=0 and π/a_2) in the two-dimensional BZ of Fig. 1(b) for (a) 1QL and (b) 2QLs thin films.

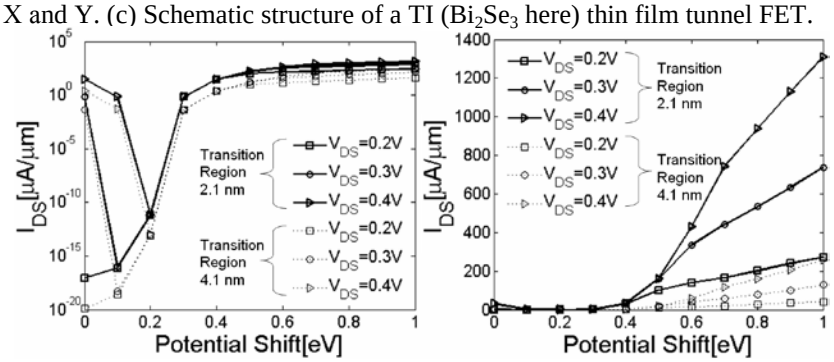

Fig. 3. I_{DS} vs channel potential for two different transition region lengths (about 2.1 and 4.1 nm) at different V_{DS} in the 1QL thin film device.

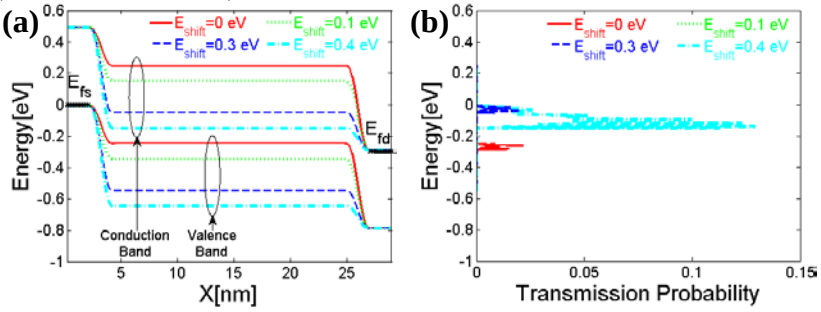

Fig. 4. (a) CB and VB edge profiles and (b) transmission probability plots of the transverse mode at k_y=0 for different potential shifts at V_{DS}=0.3V in the 1QL thin film device with the transition region length of about 2.1 nm.

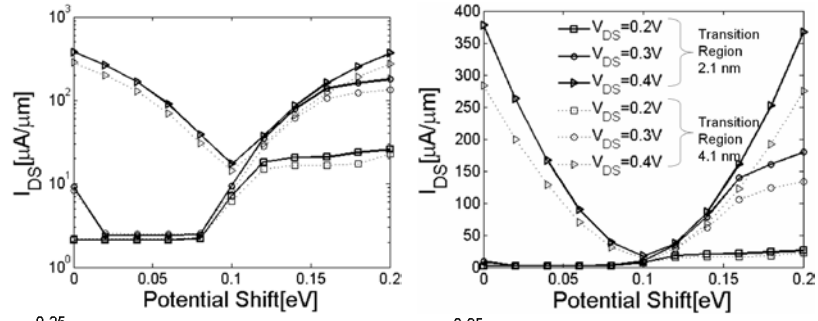

Fig. 5. I_{DS} vs channel potential plots for two different transition region lengths (about 2.1 and 4.1 nm) at different V_{DS} in the 2QL thin film device.

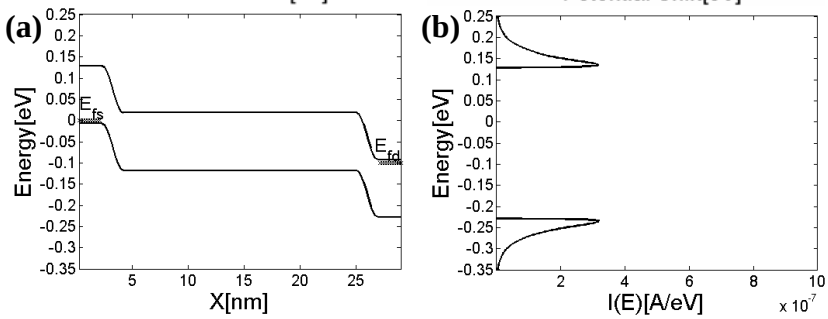

Fig. 6. (a) CB and VB edge profiles and (b) current distribution for the transverse mode at k_y=0 with the 0.05 eV channel potential shift at V_{DS}=0.1 V in the 2QL thin film device with the transition region length of about 2.1 nm

SymFET: A Proposed Symmetric Graphene Tunneling Field Effect Transistor

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Background: Graphene is being considered for alternative channel material for future CMOS technology, due to its high mobility and 2D carrier confinement [1]. The most distinguishing feature of graphene is the symmetric bandstructure, with the valence band a perfect mirror image of the conduction band. The same property carries over to 2D crystals such as Boron Nitride (BN) and less so to Molybdenum disulfide (MoS_2), which can behave as 2D insulators [2]. Attractive devices can be conceived of by stacking 2D crystals and building heterostructures without strain [3]. Experimental work has already demonstrated graphene/insulator/graphene (GIG) heterostructures [3-5]. The proposed BiSFET is based on an excitonic condensate that is a many-body electron-hole state formed in a GIG heterostructure; the power dissipation in computation using the functionality of BISFETs is predicted to be many orders lower than conventional CMOS switching [6]. Recently, we have calculated the tunneling current-voltage curves for finite area GIG heterostructures from a single-particle tunneling viewpoint, more like what happens in TFETs and RTDs. The model predicts a resonant current peak [7], and provides the framework to consider a single-particle tunneling transistor, which we call the "SymFET", since it exploits the intrinsic *symmetry* of the bandstructure of graphene. Here we present the predicted behavior of the SymFET and its characteristics.

Model: We extend the single particle tunneling model described in [7] by adding top and bottom gates that control the quasi-Fermi levels of the top and the bottom graphene layers of the GIG heterostructure. An analytical model is presented to calculate the channel potential and current. The device structure is shown in Figure 1 (a). The current that flows from one graphene layer to the other by tunneling through the insulator. For bias conditions when the two Dirac points are misaligned, only one k-ring in each Dirac cone satisfies the in-plane momentum conservation, and this nonresonant tunneling current is small. When the two Dirac points align, momentum conservation is obeyed for all energies between the left and right quasi-Fermi levels, thus a large resonant current peak is expected (Figure 1 (d)). The detailed expressions for *I-V* curves depending on both the gates and S/D biases are summarized in the left box (T = 0K). Eqs. (1) and (2) are for the nonresonant part of the current, and Eq. (3) is for the resonant part that is summed with Eqs. (1) or (2). The prefactor conductance is $G_1 = \frac{q^2 A}{2\hbar}\left(\frac{\hbar\kappa u_{12}^2 e^{-\kappa t}}{m d v_F}\right)^2$, κ is a decay constant for the tunneling current in the barrier, L is the coherence length of graphene (size of ordered areas in graphene film), and u_{11} and u_{12} are constants of order unity [7]. ΔE is the separation of quasi-Fermi level and Dirac point, $\Delta E = \Delta E_{doping} + qV_{ch}(V_G,V_D)$ and ΔE_{doping} is the chemical doping. The equations of channel potential $qV_{ch}(V_G,V_D)$ are solved analytically based on the charge neutrality equation, including the quantum capacitance of graphene (some more details are shown in the next page).

$$I = G_1\left(\frac{2\Delta E}{q} - V_{DS}\right), (0 < qV_{DS} < 2\Delta E), (1)$$

$$I = G_1\left(V_{DS} - \frac{2\Delta E}{q}\right), (qV_{DS} > 2\Delta E \text{ or } qV_{DS} < 0), (2)$$

$$I = \frac{1.6}{\sqrt{2\pi}} G_1 \frac{L\Delta E^2 (2u_{11}^4 + u_{12}^4)}{q\hbar v_F} \exp\left\{-\frac{L^2}{4\pi}\left|\frac{(qV_{DS} - 2\Delta E)}{\hbar v_F}\right|^2\right\}, (3)$$

Results and discussions: The expressions given in previous section, is for T = 0K. The room temperature results need to consider the Fermi distribution with integral over energy [7]. The corresponding device parameters are labeled in the figures. A graphene length L = 100 nm is assumed. When the tunnel barrier is thicker, the resonant peak current decreases as expected (Figure 2 (a)). Thinner t_{gate} offers better gate control and higher gate induced doping (and more resonant current). The corresponding resonance peaks increase and shift to higher bias (Figure 2 (b)). Figure 3 explores the entire bias phase space of the *I-V* characteristics. Though the on/off ratio of the SymFET is not a true performance metric, from equation (1) and (3) we find it is given by $I_{on}/I_{off} \approx L\Delta E/\hbar v_F$, (~100 for L ~ 100nm, ~1000 for L ~ 1 μm). It is independent of temperature and increases with size. The I_D-V_{DS} characteristics at fixed V_G are shown in Figure 4(a). In Figure 4(b), the I_D-V_G curve shows strong non-linear behavior. The transconductance can be large in the bias range where the resonant current peak exists. The I_D-V_{DS} curve (e.g. resonant width) is insensitive to the temperature (Figure 5), because of tunneling mechanism, except for Fermi function smearing. The slight difference at low V_{DS}, is due to the Fermi function varying with temperature. The increase of resonant peak current is because Fermi tail extends to high energy with larger density of states. The nonlinear symmetric I_D-V_{DS} behavior can also be used for purposes of frequency multiplication; if a dc voltage bias at the current peak V_{DSp} is superposed with an ac signal, the frequency of the output current will be doubled (Figure 6 schematic). The SymFET is expected to be intrinsically fast since it relies entirely on tunneling; high frequency digital operation and a host of analog applications such as frequency multiplication are thus possible by exploiting the symmetry of the bandstructure of 2D graphene.

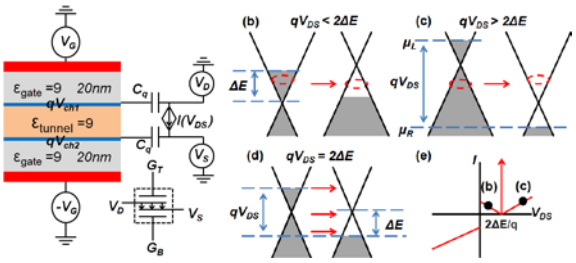

Figure 1: (a) Sketch of the Sym-FET (V_D = -V_S). C_q is the quantum capacitance. Insert is the device symbol. The band diagrams for GIG junction at voltages of (b) $qV_{DS} < 2\Delta E$, (c) $qV_{DS} > 2\Delta E$, and (d) $qV_{DS} = 2\Delta E$. When two Dirac points misalign with each other, only one k-ring meets the momentum conservation and current is small. When Dirac points align together, carriers can tunnel in all energy. The qualitative current-voltage *I-V* characteristic is shown in (e).

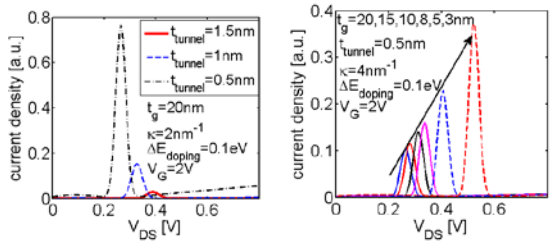

Figure 2: I_D -V_{DS} characteristic with scaling of (a) the tunneling insulator thickness and (b) the gate insulator thickness. The thickness of tunneling insulator strongly affects the tunneling current. Gate control is more effective with thinner t_{gate}. Thus electrostatic doing increase, ΔE increases and peak current increases.

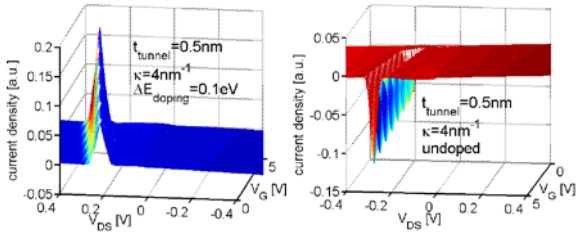

Figure 3: The contour plot of the complete bias space for (a) chemical doping ΔE = 0.1eV and (b) no chemical doping.

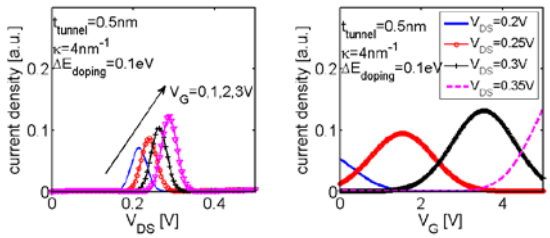

Figure 4: (a) I_D *vs.* V_{DS} curve with different V_G, large V_G induced higher doping effect and increases ΔE. V_{DSp} increases and peak current also increases. (b) I_D *vs.* V_G at different V_{DS}. Transconductance is large in the range where current resonance peak exists.

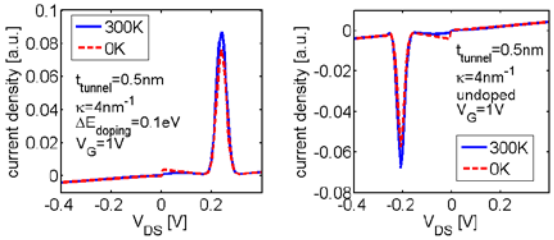

Figure 5: The *I-V* characteristics stay almost the same between T = 300K and T = 0K, since the tunneling current is insensitive to temperature. The difference at low V_{DS}, is due to the Fermi function varying with temperature. The increase of resonant peak current is because Fermi tail extends to high energy with larger density of states.

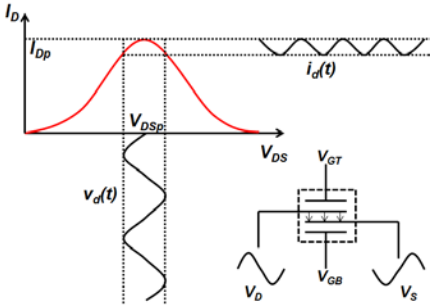

Figure 6: The red curve is the sketch of the symmetric resonance current peak, when V_{DSp} bias at resonance peak with an ac signal. The frequency of the ac signal will be double. The symmetric of conductance band and valence band in graphene offers such behavior.

$$V_{ch1}(V_G,V_D) = -V_{ch2}(V_G,V_D) = V_D + \frac{(2C_t + C_g)\pi(\hbar v_F / q)^2}{4q}$$
$$- \sqrt{\frac{(2C_t + C_g)\pi(\hbar v_F / q)^2}{2q} V_D - \frac{\pi(\hbar v_F / q)^2}{2q} C_g V_G + \frac{(2C_t + C_g)^2 \pi^2 (\hbar v_F / q)^4}{16q^2}}$$
$(V_D > 0)$
$$V_{ch1}(V_G,V_D) = -V_{ch2}(V_G,V_D) = V_D - \frac{(2C_t + C_g)\pi(\hbar v_F / q)^2}{4q}$$
$$+ \sqrt{-\frac{(2C_t + C_g)\pi(\hbar v_F / q)^2}{2q} V_D + \frac{\pi(\hbar v_F / q)^2}{2q} C_g V_G + \frac{(2C_t + C_g)^2 \pi^2 (\hbar v_F / q)^4}{16q^2}}$$
$(V_D < 0)$

Table 1. The equations of channel potential as a function of gates and S/D biases. Since the device is designed to be complete symmetric, V_{ch1} = -V_{ch2}.

(This work is supported by the Semiconductor Research Corporation Nanoelectronics Research Initiative and the National Institute of Standards and Technology through the Midwest Institute for Nanoelectronics Discovery (MIND).)

Hybrid straintronics and spintronics: An ultra energy-efficient paradigm for logic and memory

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Excessive energy dissipation during switching of logic and memory bits is the primary impediment to continued downscaling of electronic devices predicted by Moore's law. Nanomagnetic logic and memory switches are innately more energy-efficient than electronic switches because of *correlated* switching of spins that does not happen when charges are "switched" by moving them into and out of a transistor's channel. Furthermore, magnets do not "leak" unlike transistors. This results in much lower energy dissipation in a nanomagnetic switch compared to an electronic switch. However, this advantage is usually squandered in nanomagnetic logic (NML) paradigms because of very inefficient magnet switching schemes that result in mammoth dissipation in the switching circuit.

We have devised a new magnet switching scheme that we have termed *hybrid spintronics and straintronics* since it is predicated on coupling between magnetic and mechanical degrees of freedom. NML paradigms based on this approach turns out to be roughly four orders of magnitude more energy-efficient than modern day CMOS and possibly five orders more energy-efficient than other NML paradigms employing currents to switch magnets either by generating a magnetic field or spin transfer torque[1]. The central idea in our approach is to replace an ordinary magnet with a 2-phase multiferroic and rotate its magnetization through a large angle with a tiny voltage of ~ 10 mV at room temperature [1, 2]. A schematic of a multiferroic nanomagnet is shown in Fig. 1 and consists of a shape-anisotropic structure (an elliptical cylinder) made up of a piezoelectric layer elastically coupled with an overlying magnetostrictive layer. The two stable magnetization states are along the major axis of the ellipse and encode bits 0 and 1. A voltage applied across the structure generates strain in the piezoelectric that is transferred to the magnetostrictive layer and rotates its magnetization by ~ 90^0. Because of coupling between the in-plane and out-of-plane dynamics, if the stress is withdrawn quickly after the magnetization rotates by ~90^0, then it continues to rotate further and completes a ~180^0 rotation ("magnetization flip") . Extensive simulations of the switching dynamics in the presence of thermal noise based on the stochastic Landau-Lifshitz-Gilbert (LLG) equations show that the energy dissipated per switching event is less than 1 aJ at ~1 GHz clock rate [3]. This makes it one of the most energy-efficient paradigms extant.

This talk will describe Bennett clocking of logic chains [1], writing of bits in memory with straintronics with associated energy dissipation [2], design of universal logic gates that perform logic operations while dissipating ~ 2 aJ of energy at ~1 GHz sinusoidal clock rate [4], 4-state logic [5] and image processing based on the latter scheme that can reconstruct a 512×512 pixel grayscale image in ~ 2 ns [6].

1. J. Atulasimha and S. Bandyopadhyay, *Appl. Phys, Lett.* Vol. 97, 173105, 2010.
2. K. Roy, S. Bandyopadhyay and J. Atulasimha, *Appl. Phys. Lett.*, Vol. 99, 063108, 2011.
3. K. Roy, S. Bandyopadhyay, and J., Atulasimha, arXiv:1111.6129v1
4. M. S. Fashami, J.Atulasimha, S.Bandyopadhyay, *Nanotechnology*, Vol. 23 105201, 2012.
5. N. D'Souza, J. Atulasimha and S. Bandyopadhyay, *J. Phys. D: Appl. Phys*,, Vol. 44, 265001, 2011.
6. N. D'Souza, J. Atulasimha and S. Bandyopadhyay, arXiv:1109.6932v1.

[1] The "all-spin-logic" paradigm [S. Srinivasan, et al., IEEE Trans. Magn., Vol. 47, 4026 (2011)]], which is a variant of NML, uses spin polarized current for switching magnets, but is apparently equally energy-efficient as the scheme proposed here.

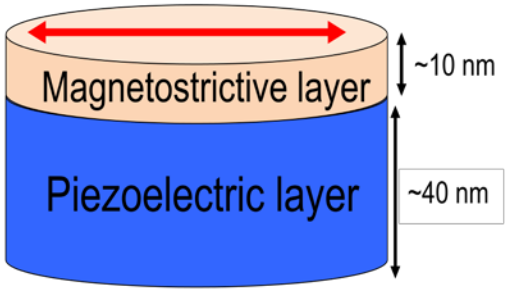

Fig. 1: A 2-phase multiferroic magnet

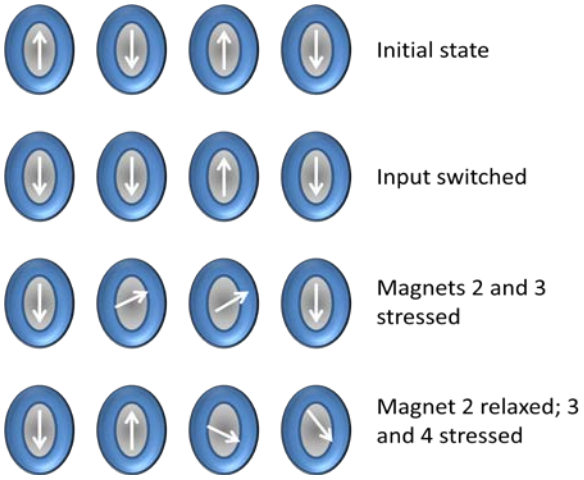

Fig. 2: Bennett clocking scheme for propagating a bit

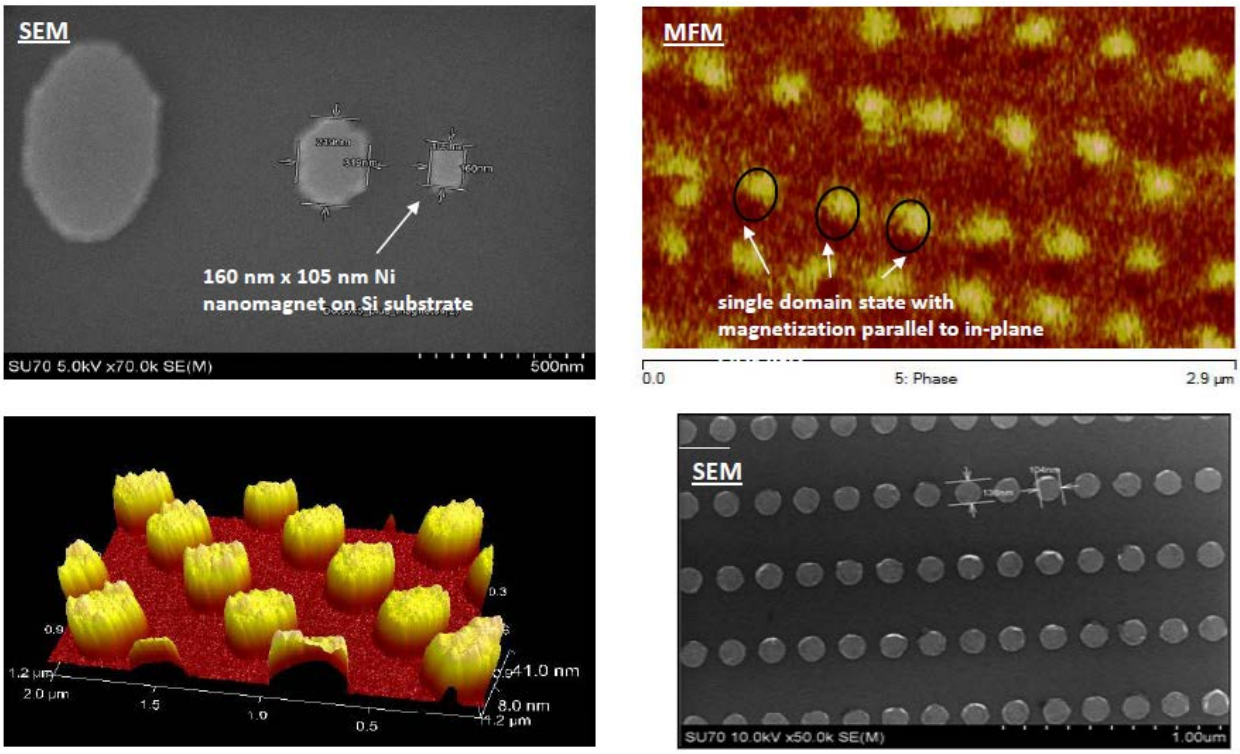

Fig. 3: Clockwise from top left: Scanning electron micrographs of nickel nanodots on Si substrate, magnetic force micrographs showing single domain states, scanning electron micrograph of arrays of nickel nanodots for logic chains, atomic force micrographs showing the absence of islanding in the nanomagnets.

Graphene and Topological Insulator Based Transistors: Beyond Computing Applications

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Silicon based field effect transistors (FET) have been the foundation of computing industries for decades. As we approach the end of the Moore's law scaling, there have been increasing interests and efforts to explore transistors based on many "emerging" (non-Si) materials that may replace or supplement Si in future electronics and computing devices. However, Si and Si-MOSFETs remain exceptionally competitive and hard to beat by most "emerging" contenders. On the other hand, many of the non-Si based "emerging transistors" have novel physical properties that may make them highly attractive for various non-computing applications. In this talk, I will discuss transistors based on graphene and topological insulators, two classes of materials that have attracted much recent attention in physics and nanoelectronics communities. While both materials feature many novel electronic properties related to the unique Dirac electronic bandstructure, the lack of band gap brings challenges in applying them as digital electronic switches in conventional computing applications. After a brief review of graphene and TI based transistors and their prospects for digital computing applications, I will focus on two examples of exploiting the unique physical properties of these transistors for non-computing applications, particularly sensing and energy conversion.

The simplest and most common graphene transistors use doped Si as a substrate and backgate. Recently we proposed that graphene on un-doped semiconductor substrates can be used as a radiation-activated field effect transistor to detect ionizing radiation [M. Foxe *et al*., IEEE Trans. Nanotech.(2012), doi:10.1109/TNANO.2012.2186312], based on the high sensitivity of graphene to charge and electric field perturbations (due to radiation) without collecting ionized charges as in conventional detectors. We have experimentally demonstrated that such graphene FETs fabricated on appropriate undoped semiconductor substrates (including SiC, GaAs, etc) can detect a broad range of radiation (X-rays, gamma-rays, and light), even at room temperature. I will discuss the potential performance advantages of such a graphene FET based radiation detector compared to conventional semiconductor charge collection based radiation detectors.

Topological insulator (TI) materials such as Bi_2Te_3 and Bi_2Se_3 have been used for decades as important thermoelectric materials. Recently, these materials have been shown to possess highly unusual, "topologically protected" metallic surface states with spin-polarized Dirac electrons. We have fabricated various back and top gated transistors based on TI thin films and nanowires. We demonstrate ambipolar field effect, and the ability to use the gate to tune the electronic transport from being bulk-dominated (metallic) to surface-dominated (topological insulator). We also demonstrate a gated-tunable thermoelectric device using TI FET. I will discuss the potential of these TIFETs to enable a new kind of high-performance thermoelectric devices harnessing the unique properties of the topological surface states.

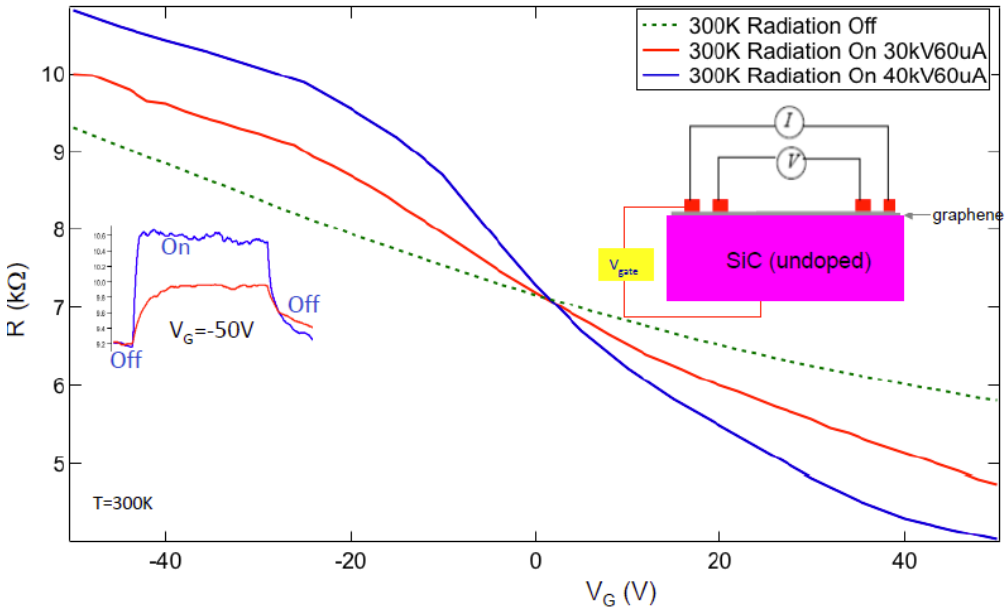

Figure 1. Graphene field effect transistor (GFET) as radiation detector. Field effect curves measured with and without X-ray irradiation (two different X-ray fluxes, red and blue) on a back gated epitaxial graphene device at room temperature. Left inset shows graphene resistance response to X-ray on/off. Light inset is a device schematic. Work in collaboration with A. Patil, O. Koybasi, I. Jovanovic, M. Bolen, P. Ye and M. Capano, and supported by DHS and DTRA.

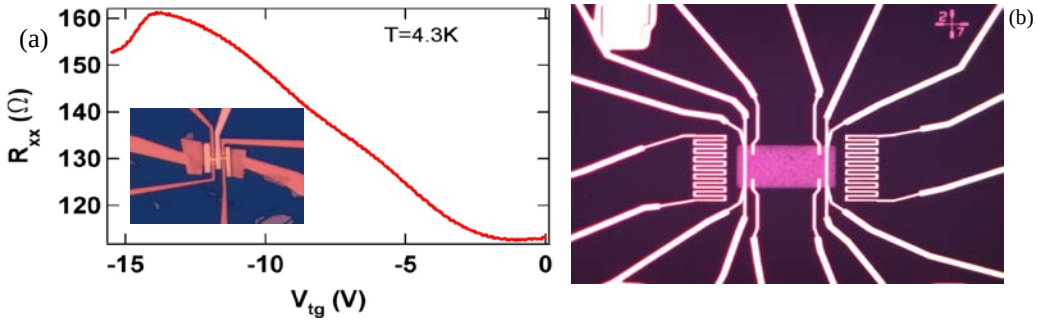

Figure 2. (a) Field effect measure in a top gated exfoliated Bi_2Se_3 TI thin film FET device. (b) A backgated field effect thermoelectric device fabricated on MBE Bi-Sb-Te TI thin film on $SrTiO_3$. The meander lines are microfabricated heaters and thermometers. Work in collaboration with H. Cao, J. Tian, I.Miotkowski, C.Chang, K.He, and Q. Xue, and supported by DARPA.

Poster Session

Monday PM, June 18th, 2012

III-1
Al_2O_3/InSb/Si Quantum Well MOSFETs Having an Ultra-Thin InSb Layer
K. Maezawa[1], T. Ito[1], A. Kadoda[1], K. Nakayama[1], Y. Yasui[1], M. Mori[1], E. Miyazaki[2] and T. Mizutani[2], [1]University of Toyama, Gofuku, Toyma, JAPAN and [2]Nagoya University, Furo-cho, Chikusa-ku, Nagoya, JAPAN

III-2 Student Paper
Ultra-Sensitive Magnetoelectric Sensor with High Saturation Field
L. Mei, Z. Fang, F. Li, S. Datta, and Q. M. Zhang, Department of Electrical Engineering, The Pennsylvania State University, University Park, Pennsylvania, USA

III-3 Student Paper
Study of SiO_x-based Complementary Resistive Switching Memristor
Y.-F. Chang[1], Y.-T. Chen[1], F. Xue[1], Y. Wang[1], F. Zhou[1], B. Fowler[2], and J. C. Lee[1], [1]Microelectronics Research Center, Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, Texas, USA and [2]PrivaTran, LLC, Austin, Texas, USA

III-4 Student Paper
Illumination Instability Analysis of ZnO Thin Film Transistors with HfO_2 Gate Dielectrics
J.J. Siddiqui[1], J.D. Phillips[1], K. Leedy[2], and B. Bayraktaroglu[2], [1]EECS Department, University of Michigan, Ann Arbor, Michigan, USA and [2]Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, Ohio, USA

III-5
1.4 kV Breakdown Voltage for MOCVD grown AlGaN/GaN HEMTs on Si substrate
S. . Selvaraj, A. Watanabe, A. Wakejima and T. Egawa, Research Center for Nano-Device and System, Nagoya Institute of Technology, Showa-ku, Nagoya, JAPAN

III-6 Student Paper
Dopant Straggle-free Heterojunction Intra-band Tunnel (HIBT) FETs with Low Drain-induced Barrier Lowering/Thinning (DIBL/T) and Reduced Variation in OFF Current
S. K. Gupta[1], J. P. Kulkarni[2], S. Datta[3] and K. Roy[1], [1]Purdue University, West Lafayette Indiana, USA, [2]Intel Corporation, Hillsboro, Oregon, USA and [3]Penn State University, University Park, Pennsylvania, USA

III-7 Student Paper
Exclusive Electrical Determination of High-Resistance Grain-Boundaries in poly-Graphene
R. Chen[1,2], S. R. Das[1], C. Jeong[1], D. B. Janes[1], and M. A. Alam[1], [1]Purdue University, West Lafayette, Indiana, USA and [2]Zhejiang University, Zhejiang, CHINA

III-8
Improved OFF-state Breakdown Voltage in AlGaN/GaN HEMTs grown on 150-mm Diameter Silicon-on-Insulator (SOI) Substrate
S. Arulkumaran[1], V. K. X. Lin[2], S. B. Dolmanan[2], G.I. Ng[3], S. Vicknesh[1], J. P. Y. Tan[2], S. L. Teo[2], M. K Kumar[2] and S. Tripathy[2], [1]Temasek Laboratories@NTU, Nanyang Technological University, SINGAPORE, [2]Institute of Materials Research and Engineering, A*STAR, SINGAPORE, and [3]NOVITAS, Nanoelectronics Centre of Excellence, School of EEE, Nanyang Technological University, SINGAPORE

III-9 Student Paper
Improved Dual-Carrier High Gain Impact Ionization Engineered Avalanche Photodiode
J. Huang[1], K. Banerjee[1], S. Ghosh[1], and M. M. Hayat[2], [1]Dept. of ECE, Univ. of Illinois at Chicago, Chicago, Ilinois, USA and [2]Center for High Technology Materials, Univ. of New Mexico, Albuquerque, New Mexico, USA

III-10 Student Paper
Enhanced Tunneling Current in 1d-1d$_{Edge}$ Overlapped TFET's
S. Agarwal and E. Yablonovitch, University of California, Berkeley, California, USA

III-11 Student Paper
Metal Contacts to Mo_2: a Two-Dimensional Semiconductor
A. T. Neal, H. Liu, J. J. Gu, and P. D. Ye, School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana, USA

III-12 Student Paper
Balancing stress & dipolar interactions for fast, low power, reliable switching in multiferroic logic
K. Munira, S. Nadri, M. Forgues, and A. W. Ghosh, Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, Virginia, USA

III-13 Student Paper
Double Slot High-k Waveguide Grating Couplers for Silicon Photonics
M. M. Naiini, C. Henkel, G. B. Malm and M. Östling, KTH Royal Institute of Technology, School of Information and Communication Technology, Integrated Devices and Circuits, Kista, SWEDEN

III-14 Student Paper
Self-aligned metal S/D GaSb p-MOSFETs using Ni-GaSb alloys
C. B. Zota, S. H. Kim, Y. Asakura, M. Takenaka and S. Takagi, School of Engineering, The University of Tokyo, Bunkyo-ku, Tokyo, JAPAN

III-15 Student Paper
Bilayer Graphene Vertical Tunneling Field Effect Transistor
D. Reddy, L. F. Register, and S. K. Banerjee, University of Texas, Austin, Texas, USA

III-16 Student Paper
440 V AlSiN-Passivated AlGaN/GaN High Electron Mobility Transistor with 40 GHz Bandwidth
E. Harvard and J. R. Shealy, Cornell University, School of Electrical and Computer Engineering, Ithaca, New York, USA

III-17
Analysis of terahertz zero bias detectors by using a triple-barrier resonant tunneling diode integrated with a self-complementary bow-tie antenna
M. Suhara[1], S. Takahagi[1], K. Asakawa[1], T. Okazaki[1], M. Nakamura[1], S. Yamashita[1], Y. Itagaki[1], M. Saito[1], A. Tchegho[2], G. Keller[2], A.r Poloczek[2], W. Prost[2], F-J. Tegude[2], [1]Electrical and Electronic Engineering, Graduate School of Science and Engineering, Tokyo Metropolitan University, Hachioji, Tokyo, JAPAN and [2]Center for Semiconductor Technology and Optoelectronics, University of Duisburg-Essen, Duisburg, GERMANY

III-18
An InAs Nanowire Spin Transistor with Subthreshold Slope of 20mV/dec
K. Yoh[1], Z. Cui[1], K. Konishi[1], M. Ohno[2], K. Blekker[3], W. Prost[3], F.-J. Tegude[3], J.-C. Harmand[4], [1]Research Center for Integrated Quantum Electronics , Hokkaido University, Sapporo, JAPAN, [2]Graduate School of Engineering, Hokkaido University, Sapporo, JAPAN, [3]Semiconductor and Information Engineering, University of Duisburg-Essen, Duisburg, GERMANY, and [4]CNRS-Laboratory of Photonic and Nanostructures , Marcoussis, FRANCE

III-19 Student Paper
Understanding dual-gate polymer field-effect transistors
T.-J. Ha[1], P. Sonar[2] and A. Dodabalapur[1], [1]Microelectronics Research Center, The University of Texas at Austin, Austin, Texas, USA and [2]Institute of Materials Research and Engineering, Singapore, SINGAPORE

III-20 Student Paper
Fundamental Limitations of Conventional-FET Biosensors: Quantum-Mechanical-Tunneling to the Rescue
D. Sarkar and K. Banerjee, Department of Electrical and Computer Engineering, University of California, Santa Barbara, California, USA

III-21 Student Paper
Can Quasi-Saturation in the Output Characteristics of Short-Channel Graphene Field-Effect Transistors be Engineered?
K. Ganapathi[1], M. Lundstrom[2] and S. Salahuddin[1], [1],Department of Electrical Engineering and Computer Sciences, UC Berkeley, Berkeley, California, USA and [2],School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana, USA

III-22 Student Paper
Phonon Limited Transport in Graphene Pseudospintronic Devices
Z. J. Estrada, B. Dellabetta, U. Ravaioli, and M. J. Gilbert, University of Illinois at Urbana-Champaign, Urbana, Illinois, USA

III-23
Resistive Switching in Aluminum Nitride
M. J. Marinella, J. E. Stevens, E. M. Longoria, and P. G. Kotula, Sandia National Laboratories, Albuquerque, New Mexico, USA

III-24 Student Paper
Limits of Detection for Silicon Nanowire BioFETs
N. K. Rajan, X. Duan, A. Vacic, D. A. Routenberg, M. A. Reed, Dept. of Applied Physics, Dept. of Electrical Engineering, New Haven, Connecticut, USA

III-25
Hole-blocking TiO_2/Silicon Heterojunction for Silicon Photovoltaics
S. Avasthi[1], W. McClain[2], J. Schwartz[2], and J. C. Sturm[1], Princeton Institute for the Science and Technology of Materials, Princeton University, Princeton New Jersey, USA and [1]Department of Electrical Engineering and [2]Department of Chemistry

III-26 Student Paper
Recess Integration of Platelet Laser Diodes with Waveguides on Silicon
S. Famenini and C. G. Fonstad, Massachusetts Institute of Technology, Cambridge, Massachusetts, USA

III-27 Student Paper
NLSTT-MRAM: Robust Spin Transfer Torque MRAM using Non-Local Spin Injection for Write
M. Sharad[1], G. Panagopoulos[1], C. Augustine[2] and K. Roy[1], [1]School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana, USA and [2]Circuit Research Lab, Intel labs, Intel Corporation, Hillsboro, Oregon, USA

III-28 Student Paper
All Spin Logic device as a compact artificial neuron
A. Sarkar[1], B. Behin-Aein[2], S. Srinivasan[1], and S. Datta[1], [1]School of Electrical and Computer Engineering, Purdue University, W. Lafayette, Indiana, USA and [2]Technology Research Group, GLOBALFOUNDRIES USA, Sunnyvale, Calidorna, USA

III-29 Student Paper
Experimental Demonstration of "Cold" Low Contact Resistivity Ohmic Contacts on Moderately Doped n-Ge with in-situ Atomic Hydrogen Clean
A. Agrawal[1], J. Park[2], D. Mohata[1], K. Ahmed[2] and S. Datta[1], [1]Department of Electrical Engineering, The Pennsylvania State University, University Park, Pennsylvania, USA and [2]Applied Materials, Inc., Santa Clara, California, USA

III-30 Student Paper
Mobility and Scattering Mechanisms in Buried InGaSb Quantum Well Channels Integrated with in-situ MBE Grown Gate Oxide
S. Madisetti, P. Nagaiah, T. Chidambaram, V. Tokranov, M. Yakimov, and S. Oktyabrsky, College of Nanoscale Science and Engineering, University at Albany- SUNY, Albany, New York, USA

III-31 Student Paper
Dielectric Thickness Dependence of Quantum Capacitance in Graphene Varactors with Local Metal Back Gates
M. A. Ebrish and S. J. Koester, University of Minnesota-Twin Cities, Minneapolis, Minnesota, USA

III-32
Negative dierential resistance in short-channel graphene FETs: semianalytical model and simulations
R. Grassi[1], T. Low[2], A. Gnudi[1] and G. Baccarani[1], [1]ARCES, University of Bologna, Bologna, ITALY and [2]IBM T.J. Watson Research Center, Yorktown Heights, New York, USA

III-33 Student Paper
Drain-Induced-Barrier Lowering and Subthreshold Swing Fluctuations in 16-nm-Gate Bulk FinFET Devices Induced by Random Discrete Dopants
H.-W. Su, Y. Li, Y.-Y. Chen, C.-Y. Chen, and H.-T. Chang, Parallel and Scientific Computing Laboratory, Department of Electrical Engineering, National Chiao Tung University, Hsinchu, TAIWAN

III-34 Student Paper
THz Detector Based on Proximity Effect of Topological Insulator
X. Li, Y. G. Semenov, and K. W. Kim, Dept. of Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina, USA

III-35 Student Paper
Transverse-Field Bandgap Modulation on Graphene Nanoribbon Transistors by Double-Self-Aligned Spacers
L.-T. Tung, M. V. Mateus and E. C. Kan, School of Electrical and Computer Engineering, Cornell University, Ithaca, New York, USA

III-36 Student Paper
Epitaxial Si Punch-Through based Selector for Bipolar RRAM
P. Bafna[1], P. Karkare[1], S. Srinivasan[1], S. Chopra[2], S. Lashkare[1], Y. Kim[2], S. Srinivasan[2], S. Kuppurao[2], S. Lodha[1], and U. Ganguly[1], [1]Department of Electrical Engineering, Indian Institute of Technology, Bombay, Mumbai, INDIA and [2]Epi-Division, Front End Products, Applied Materials Inc., Santa Clara, California, USA

III-37 Student Paper
A Figure of Merit for Oscillator-Based Thin-Film Circuits on Plastic for High-Performance Signaling, Energy Harvesting and Driving of Actuation Circuits
W. Rieutort-Louis, L. Huang, Y. Hu, J. Sanz-Robinson, S. Wagner, J. C. Sturm, and N. Verma, Princeton University, Department of Electrical Engineering, Princeton, New Jersey, USA

III-38 Student Paper
Short-Channel Enhancement-mode Planar GaAs Nanowire HEMTs through a Bottom-up method
X. Miao, C. Zhang and X. Li, Department of Electrical and Computer Engineering, Micro and Nanotechnology Laboratory University of Illinois at Urbana-Champaign, Urbana, Illinois, USA

III-39 Student Paper
Electric Field Driven Domain Wall Transfer in Hybrid Structures
X. Duan[1], V. Stephanovich[2], Y. G. Semenov[1],H. Fangohr[3], M. Franchin[3], and K. Wook Kim[1], [1]Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina, USA, [2]nstitute of Physics, Opole University, Oleska, POLAND and [3]Engineering and the Environment, University of Southampton, Southampton, UNITED KINGDOM

III-40 Student Paper
Comparison of Graphene Nanoribbons With Cu and Al Interconnects
N. Wang[1], C. D. English[2], and E. Pop[1], [1]Dept. of Electrical and Computer Engineering and [2]Dept. of Physics, University of Illinois at Urbana-Champaign, Urbana Ilinois, USA

III-41 Student Paper
Electrical Control of Nuclear-Spin-Induced Hall Voltage in an Inverted InAs Heterostructure
T. Ishikura, Z. Cui and K. Yoh, Research Center of Integrated Quantum Electronics, Hokkaido University, Sapporo, JAPAN

III-42 Student Paper
Epitaxialy defined (ED) FinFET: to reduce V_T variability and enable multiple V_T
S. Mittal[1], S. Gupta[2], A. Nainani[2], M.C. Abraham[2], K. Schuegraf[2], S. Lodha[1], U. Ganguly[1], [1]CEN, Department of EE, Indian Institute of Technology Bombay, INDIA and [2]Applied Materials Inc, Santa Clara, California, USA

III-43 Student Paper
Power Reduction in Nanomagnetic Logic Clocking through High Permeability Dielectrics
P. Li[1], G. Csaba[1], V. K. Sankar[1], X. S. Hu[2], M. Niemier[2], W. Porod[1], and G. H. Bernstein[1], [1]Department of Electrical Engineering and [2]Department of Computer Science and Engineering, University of Notre Dame, Notre Dame, Indiana, USA

III-44 Student Paper
New Tunnel-FET Architecture with Enhanced I_{ON} and Improved Miller Effect for Energy Efficient Switching
A. Biswas, C. Alper, L. De Michielis, and A. M. Ionescu, Nanoelectronics Devices Laboratory (NANOLAB), Ecole Polytechnique Fédérale de Lausanne, EPFL, SWITZERLAND

III-45 Student Paper
Switching dynamics in ferroelectric-charge hybrid nonvolatile memory
K. Auluck, S. Rajwade and E. C. Kan, School of Electrical and Computer Engineering, Cornell University, Ithaca, New York, USA

III-46 Student Paper
Frequency Dependence of Amorphous Silicon Schottky Diodes for Large-Area Rectification Applications
J. Sanz-Robinson, W. Rieutort-Louis, N. Verma, S. Wagner, and J. C. Sturm, Dept. of Electrical Engineering and the Princeton Institute for the Science and Technology of Materials, Princeton University, Princeton, New Jersey, USA

III-47
Reliability Improvement Achieved by N_2O Radical Treatment for AlGaN/GaN Heterojunction Field-Effect Transistors
C.-Y. Hu and T. Hashizume, Research Center for Integrated Quantum Electronics (RCIQE),Hokkaido University, Sapporo, JAPAN

III-48 Student Paper
Exploring Variability and Reliability of Multi-Level STT-MRAM Cells
G. Panagopoulos[1], C. Augustine[2], X. Fong[1] and K. Roy[1], [1]School of ECE, Purdue University, West Lafayette, Indiana, USA and [2]Circuit Research Lab, Intel labs, Hillsboro, Oregon, USA

III-49 Student Paper
Comparative Study of LEDs conformally overgrown on multi-facet GaN NWs vs. conventional c-plane LEDs
A..M. Hosalli[1], P. Frajtag[2], D. M. Van Den Broeck[1], T. Paskova[1,2], N..A. El-Masry[2], and S..M. Bedair[1,], [1]Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina, USA and [2]Department of Materials Science and Engineering, North Carolina State University, Raleigh, North Carolina, USA

III-50 Student Paper
Inkjet-printed SWCNT films for stretchable electrode and strain sensor applications
T. Kim, J. Byun, H. Song and Y. Hong, Department of Electrical Engineering and Computer Science, Seoul National University, Gwanak-gu, Seoul, KOREA

III-51 Student Paper
Comparison of Instantaneous Crystallization and Metastable Models in Phase Change Memory Cells
A. Faraclas, N. Williams, G. Bakan, A. Gokirmak, and H. Silva, Electrical and Computer Engineering, University of Connecticut, Storrs, Connecticut, USA

III-52

A Surface-Potential Based Compact Model for GaN HEMTs Incorporating Polarization Charges

R. Jana and D. Jena, Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA

Al_2O_3/InSb/Si Quantum Well MOSFETs Having an Ultra-Thin InSb Layer

Koichi Maezawa[1], Taihei Ito[1], Azusa Kadoda[1], Koji Nakayama[1], Yuichiro Yasui[1], Masayuki Mori[1], Eiji Miyazaki[2] and Takashi Mizutani[2]

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InSb is one of the most promising candidates for the channel layers of the post scaling LSIs, because it features highest electron mobility of 78,000 $cm^2/(Vs)$ and highest saturation velocity of $5x10^7$ cm/s among III-V compound semiconductors. High performance HEMTs based on InSb/InAlSb material system have been already demonstrated [1]. However, growth of high quality InSb on Si is difficult due to the large lattice mismatch of 19.3%. We have recently demonstrated that good InSb epitaxial films can be grown on Si (111) substrates using novel growth technique [2]. This technique is based on the fact that the InSb layer grown on a Si (111) substrate is rotated by 30 degrees with respect to the substrate under a certain initial condition, which reduces the lattice mismatch to only 3.3 %, as shown in Fig. 1. Very high mobility of 40,000 $cm^2/(Vs)$ with low carrier concentration of $1.8x10^{16}$ cm^{-3} has been obtained using this growth technique for 1-μm-thick films [3]. Moreover, this drastic reduction of the lattice mismatch produces a new possibility, a pseudomorphic InSb/Si quantum well (QW) MOSFETs based on an ultra thin InSb layer grown directly on Si. When the thickness of the InSb channel layer reduces to the critical thickness, such thin channels should have good quality. This has significant advantages, such as elimination of the time-consuming thick buffer layer growth, good electron confinement by the InSb/Si heterojunction. Furthermore it can receive benefits of SOI if one uses SOI substrates. In this paper, we report the fabrication and the properties of Al_2O_3/InSb/Si QW MOSFETs having an ultra thin InSb channel layer.

The details of the growth procedure were reported previously [3], and we describe its essence, here. A key to rotate the InSb epitaxial layer is the InSb initial bi-layer prepared by adsorption of 1 monolayer Sb onto In-induced surface reconstruction. Special care is taken here to the phase of the surface reconstruction. The InSb film having only 15 nm thickness was grown on this bi-layer. We observed good *C-V* characteristics for the MOS diodes having such thin InSb layers [4], which are similar to those of much thicker (1 μm) samples, though this thickness is still larger than the expected critical thickness. The p-type Si substrates having specific resistance of 10-20 Ωcm were used. The epitaxial layer was n-type, though no impurity was intentionally doped.

We fabricated Al_2O_3/InSb MOSFETs on epitaxial films grown using above technique. The cross-sectional view of the fabricated MOSFETs is shown in Fig. 2. First, the InSb layer is etched for isolation by citric acid based etchant, then the same resist pattern was used to lift off the sputtered SiOs layer, which insulates metal pads from the Si substrate. An Al_2O_3 gate insulator layer was deposited by using atomic layer deposition (ALD) at 250 C after ohmic metal formation. Thickness of the Al_2O_3 was 10 nm. Ohmic contacts were based on Sn/Au/Ni/Ti/Au metals deposited by electron beam evaporation. The devices were completed by Ti/Au gate metal formation. Figure 3 shows the microphotograph of the fabricated device.

Figure 4 shows the capacitance-voltage (*C-V*) curve of the MOS diode fabricated simultaneously on the same wafer. The *C-V* curve was measured at room temperature with signal frequencies of 100 kHz. This *C-V* curve shows low-frequency behavior even at 100 kHz. This type of *C-V* behavior is characteristic to narrow bandgap semiconductors having high generation-recombination rate. This curve is similar to those observed for thicker InSb diodes [4], and indicates occurrence of the accumulation and inversion.

Figures 5 and 6 show examples of the I_D-V_D characteristics and the transfer characteristics of the fabricated MOSFETs, respectively. The gate length and width were 2 and 40 μm, respectively. Good I_D-V_D characteristics with an transconductance of 67 mS/mm were obtained as shown in the figure. This demonstrates that the ultra thin InSb channel layer grown directly on Si can be used for MOSFET channels. Though further studies are needed, we think the InSb/Si pseudomorphic quantum well MOSFETs can be a promising candidate for future VLSIs.

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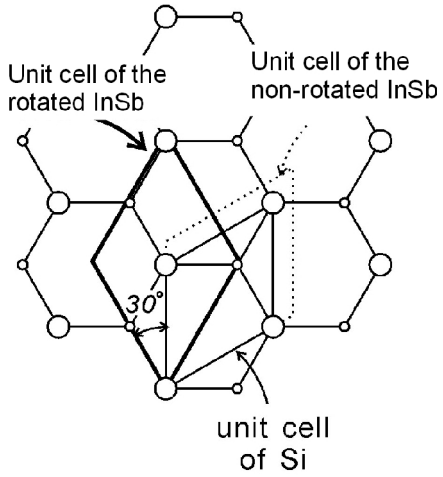

Fig. 1 Schematic view of the atom position of the Si(111) surface and the unit cells of Si and InSb. The 30-degree rotation of the InSb unit cell reduces the lattice mismatch drastically.

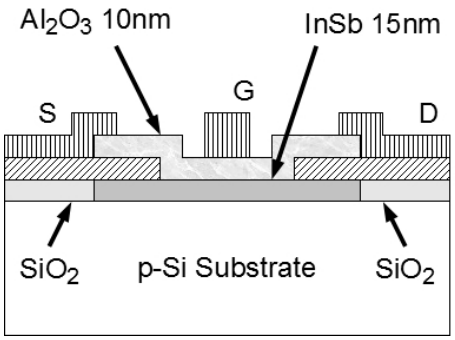

Fig. 2 Schematic cross-sectional view of the fabricated MOSFETs.

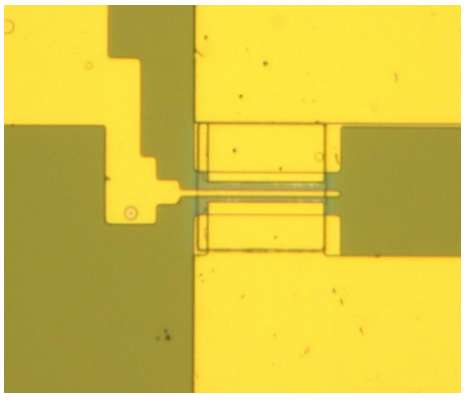

Fig. 3 Microphotograph of the fabricated MOSFET.

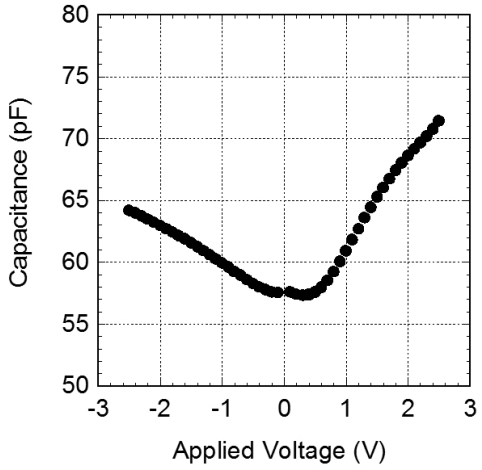

Fig. 4 The *C-V* curve of the MOS diode fabricated simultaneously with the MOSFETs. It was measured at RT with a signal frequency of 100 kHz. The capacitor was circular with a 100-μm diameter.

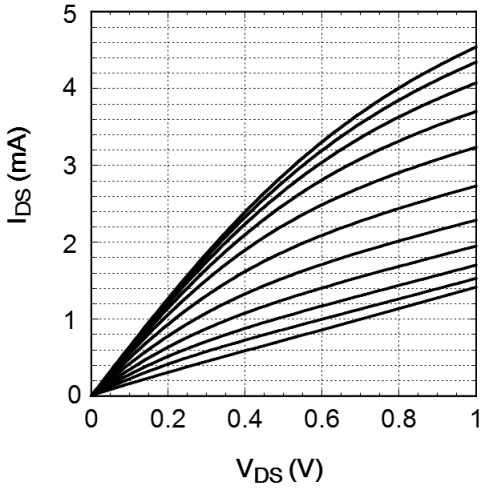

Fig. 5 I_D-V_D characteristics of the fabricated MOSFET. The gate voltage is varied from -1 V to 1V with a 0.2-V step. The gate length and width are 2 and 40 μm, respectively.

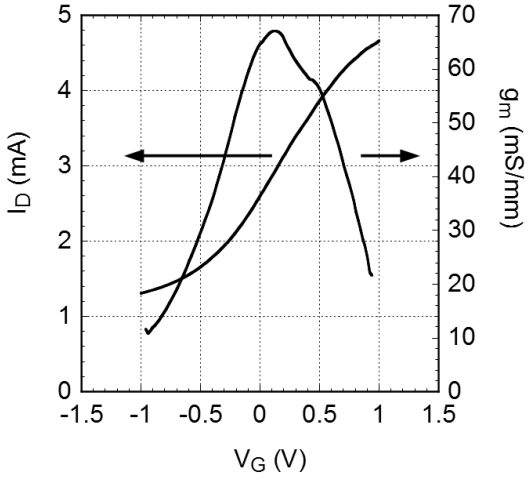

Fig. 6 Transfer characteristics of the fabricated MOSFET. The gate length and width are 2 and 40 μm, respectively.

Ultra-Sensitive Magnetoelectric Sensor with High Saturation Field

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Magnetoelectric effect is a material phenomenon featuring the interchange between magnetic and electric energies or signals. Ultra sensitive magnetic sensor operating at room temperature can be realized by the magnetoelectric coupling, this sensor has the potential to be used for bio signal detection like biomagnetic liver susceptometry (BLS) because of its high sensitivity and high saturation field.

The principle of the ME sensor is that a magnetic field induces a strain in the ferromagnetic substance ($NiFe_2O_4$, Metglas, Terfenol-D, TbFe2, etc) by magnetostriction; and the strain is then coupled to the piezoelectric substance ($Pb(Zr, Ti)O_3$, PMNPT, PVDF, etc), resulting in an electric output signal, as illustrated in Figure 1. The BLS technique entails measurement of magnetic field variation in the region of liver in response to an external magnetizing field, which is typically >0.1 Tesla and the feedback signal from liver is very weak (~ 10-6 of the applied field). For these reasons, ultra sensitive magnetoelectric sensor with high saturation field should be studied. Because of the nonlinearity of ferromagnetic substance's magnetization, the saturation field of different ME structure will differ a lot, Figure 2 is the B-H loop of our TbFe2 ferromagnetic material, the saturation field is above 0.5 Tesla which is 10 times larger than current used Terfenol-D ferromagnetic phase and suitable for BLS measurement. Figure 3 is the magnetoelectric coefficient of TbFe2/PZT structure. Table 1 is the properties of different magnetostrictive materials.

High sensitivity is also required for BLS measurement; Signal-to-noise ratio (SNR) is one key parameter for ultrasensitive magnetic sensors. In general, charge sensitive readout is preferred in the piezoelectric sensors, especially when integrated with advanced microelectronics. The charge amplifier is based on a charge transfer from the sensor to a fixed capacitor, C_f, and then measuring the voltage across it. For the ME sensor systems, various sources such as the piezoelectric layer and the readout circuit can contribute to the noises. Our studies have shown that at low frequencies the main noise source is due to the dielectric loss (~$C_p \tan\delta$) [2].The SNR could be calculated as

$$\mathrm{SNR} = \frac{V_{output}}{V_{n,\delta}} = \frac{d_p}{s_p^E\left(1+\frac{s_m^H t_p}{s_p^E t_m}\right)\sqrt{\frac{4kT\tan\delta}{\omega}}}\sqrt{\frac{t_p A_p}{\varepsilon_p}}\frac{\Delta S}{\Delta H_a}$$

Which shows the dependence of field sensitivity of the ME sensor on the material parameters such as the piezo-coefficient d_p, the magnetostrictive coefficient $\Delta S_m/\Delta H_a$, and the elastic compliance $s^E{}_p$.of piezolayer. Figure 4 is the noise level of our TbFe2/PZT sensor; the sensor noise is at nano Tesla range (lower than 10-9Tesla/ rtHz) at the frequency of 1Hz and even lower at higher frequency. Since the feedback signal is ~ 10-6 of the applied field (0.1 Tesla or higher), the noise is lower than 1/100 of the feedback signal which means a SNR higher than 100.

The magnetic sensors based on TbFe2/PZT ME laminates developed here have several inherent advantages, such as high saturation field, high sensitivity, low noise level, compact size, simple structure, and as passive sensors that can be operated without external power supply. Compared with current BLS measurement techniques, our sensor is ultra portable with prominent sensitivity. Accurate measurements of low level bio magnetic signal can be used for noninvasive medical imaging and diagnosis. Their performance can be compared with the most sensitive magnetic-field sensor –SQUID sensors. However, such detectors need expensive and cumbersome cryogenics to operate [3], which severely limit its broad usage and proliferation for biomedical imaging and diagnosis. The recent advancement in TbFe2/PZT ME sensors which could reach Pico-Tesla sensitivity and Tesla range saturation field, can lead to chip-scale magnetic sensors at room temperature for biomedical imaging and diagnoses.

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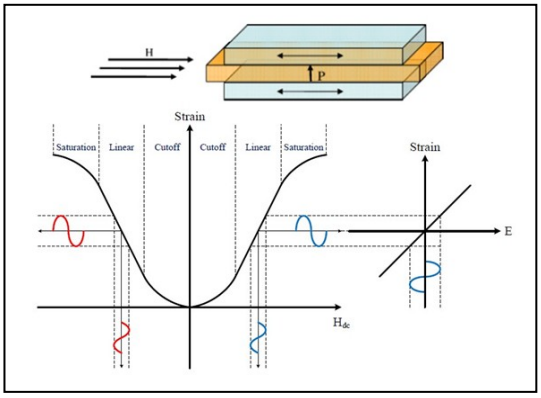

Figure 1: Schematic representation of the ME effect in the composites utilizing the product property

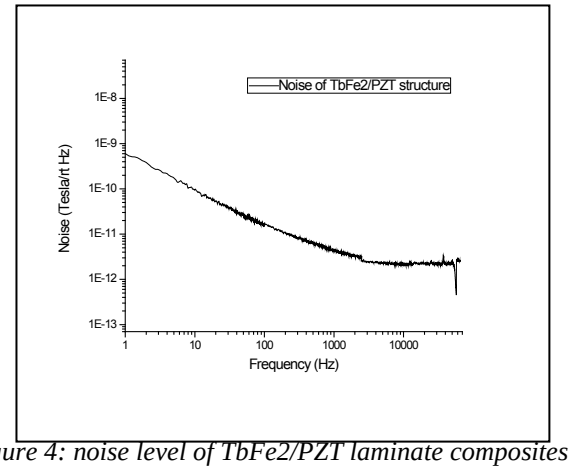

Figure 4: noise level of TbFe2/PZT laminate composites

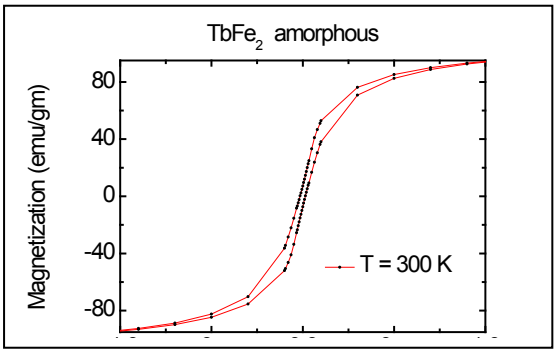

Figure 2: Magnetization of un-annealed TbFe2 ferromagnetic material at 300K

	NiFe2O4	Terfenol-D	Fe-Ga	Metglass 2605SA1	TbFe2
λ (ppm)	27	1400	200	40	1300-1400
μ	20	6-10	20	45000(as cast)	6-10
ρ(g/cm3)	5.37	7.8	7.7	7.18	7-8
R(Ωm)	10^6	$5.8*10^{-7}$	$6*10^{-7}$	$1.3*10^{-6}$	$5.8*10^{-7}$
Saturation field (10-4 Tesla)	120	300-500		10	5000

Table 1：Properties of Magnetostrictive Materials

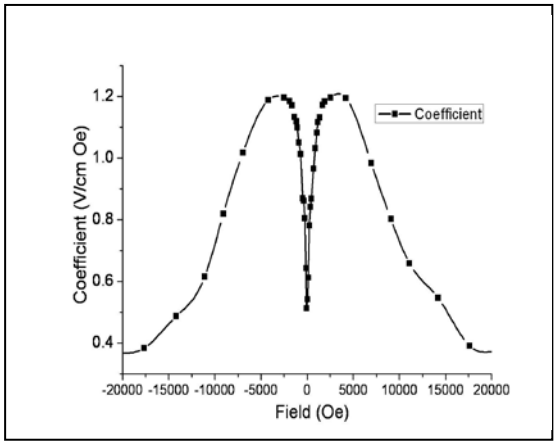

Figure 3: αME as a function of dc bias magnetic field for TbFe2/PZT laminate composites

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Study of SiO_x-based Complementary Resistive Switching Memristor

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The electrical characteristics of SiO_x-based complementary resistive switching (CRS) memristor have been investigated. Post-deposition annealing (PDA: 500°C 5min in O_2) of $TaN/SiO_2/n^{++}$ Si-substrate CRS memristor has been found to reduce operational variation in device characteristics, as well as improve the electrical stability during repeated switching. In this work, we have also studied the effects of sweeping polarity, operating temperature, electrode material and dimension scaling. Our experimental results not only provide additional insights into optimization of the SiO_x-based CRS memory but also help in constructing a physical picture for the switching mechanism.

The schematic cross section and process flow of a SiO_x-based CRS memristor are shown in Fig. 1. The electroforming process was performed by ramping applied bias from 0V to about 15V. A typical CRS operation with repeated cycling (30 times) for devices undergone a PDA anneal is shown in Fig. 2. The electrical stability of memory window (i.e. low resistance state/ high resistance state (LRS/HRS) current ratio @ 0.2V) has been found to improve significantly for devices with PDA anneal (see Fig. 3). Also, the CRS memory window was maintained at least one order of magnitude and without degradation during cycling for each polarity sweeping. Note that the HRS current and the reset voltage values are larger in the negative reset operation than in the positive operation, but they are found to be independent with the set process polarities (Fig. 3). However, the reset current values were found to exhibit an opposite trend (Fig. 4). According to previous studies [1], the Si nano-filaments would be formed at the device edge after an electroforming process. The current-induced Joule heating energy [2] and asymmetric thermal conductivity between top TaN electrode and bottom n^{++} Si-substrate [3] indicate that the resistive switching occurs at the cathode rather than the anode side.

Comparing to the TaN electrode CRS memristors, the memory window of the poly-Si top electrode devices exhibit less stable CRS behavior (see Fig. 5). The temperature dependence for the TaN electrode devices suggests semiconductor-type current transport for both HRS and LRS (Fig. 5). Higher temperature would accumulate resistive switching reaction in the CRS behaviors [2]. By scaling the device area, the reset current has been reduced to the sub-100uA regime (Fig. 6). The results indicate that SiO_x-based CRS memristors hold good promise for the future nonvolatile memory applications.

In conclusion, CRS behaviors have been demonstrated with $TaN/SiO_2/n^{++}$ Si-substrate memristor structure. Post-deposition anneal (PDA) treatment has been used to improve electrical characteristics and device stability. Moreover, by detailed analysis of the switching characteristics, it has been found that resistive switching occurs at the cathode side. This could be due to asymmetric thermal dissipation with two different materials. Electrode and temperature effect indicate that TaN is a suitable electrode for the SiO_x-based CRS memristor and thermal switching reaction may be responsible for CRS operation. Our results suggest that SiO_x-based CRS memristors hold good promise for future resistive switching memory.

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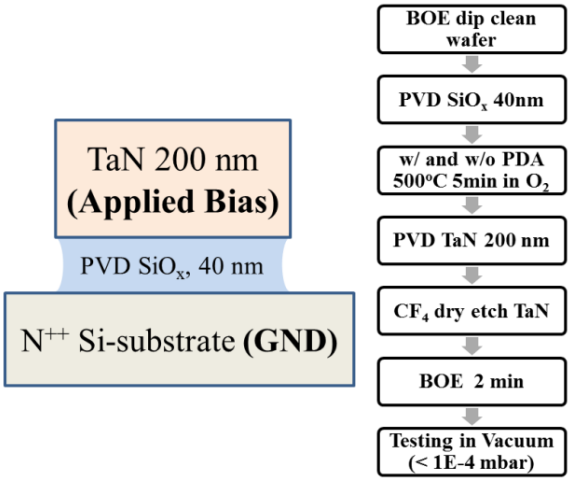

Fig.1 Schematic cross-section and process flow of $TaN/SiO_2/n^{++}$ Si-substrate structure.

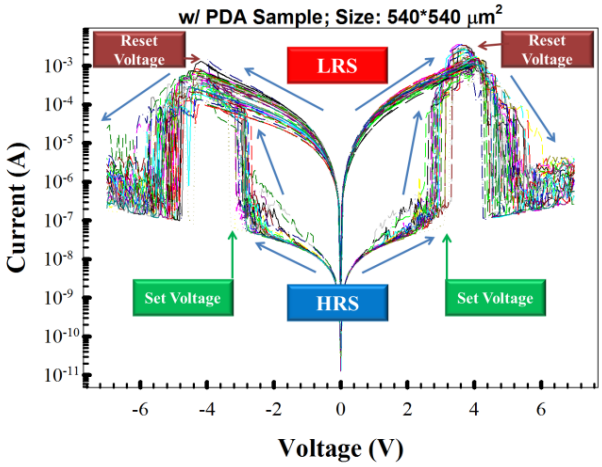

Fig.2 CRS behaviors of TaN devices w/ PDA. The arrows indicate voltage sweeping directions.

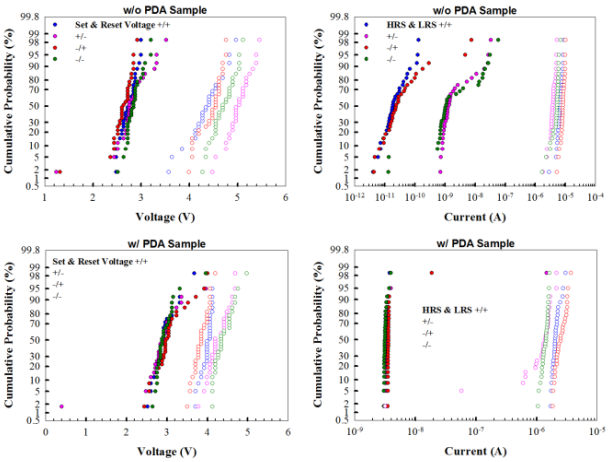

Fig. 3 Distribution of polarity-dependence V_{set}/V_{reset} and HRS/LRS for TaN devices w/o and w/ PDA.

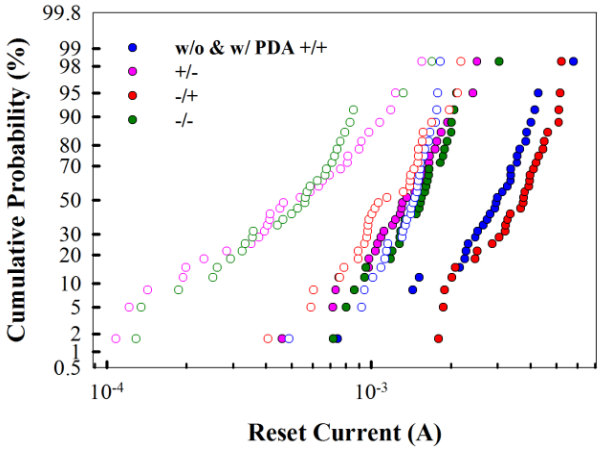

Fig. 4 Polarity-dependence I_{reset} for TaN devices w/o and w/ PDA.

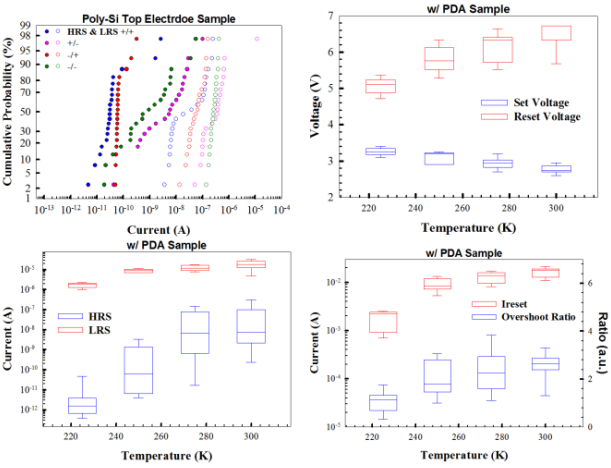

Fig. 5 Poly-Si top electrode devices and temperature effect of TaN w/ PDA devices.

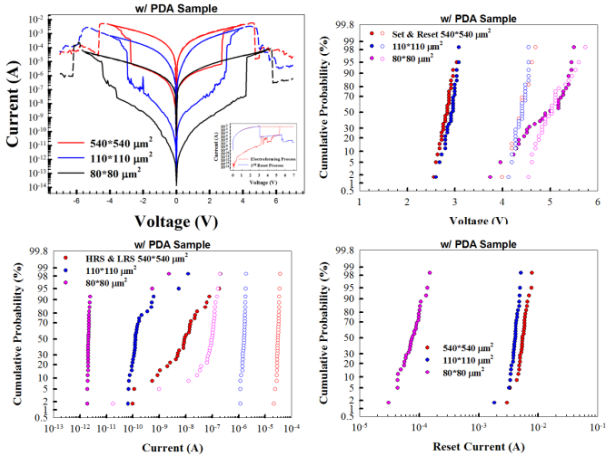

Fig. 6 Scaling effect and its corresponding distribution of electrical characteristics for TaN w/ PDA devices.

Illumination Instability Analysis of ZnO Thin Film Transistors with HfO_2 Gate Dielectrics

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ZnO thin film electronics have received much attention due to the relatively high electron mobility of ZnO thin films in comparison to amorphous silicon (a-Si) and organic thin films. There is significant interest in using ZnO thin film transistors (TFTs), or similar oxides such as InGaZnO and zinc tin oxide, to replace a-Si TFTs in large area display technologies such as active matrix liquid crystal display (AMLCD) devices and active matrix organic light-emitting diode (AMOLED) displays where transparency in the visible range and high carrier mobilities are significant advantages. In addition, the integration of high dielectric constant (high-k) dielectrics in ZnO TFTs has demonstrated performance advantages including reduced operating voltage, increased I_{on}/I_{off} ratios, and larger transconductance. HfO_2 has emerged as a high-k dielectric of choice for both silicon microelectronics and thin film electronics due to the high dielectric constant ($\varepsilon_r \sim 25\varepsilon_0$), low leakage current, and low synthesis temperature.

It is important to investigate device stability to gain understanding about the material system and improve transistor performance. Next generation Active Matrix Liquid Crystal high resolution displays with 4000x2000 pixels, a high frame rate (>240 Hz), and sized larger than 70 inches require a thin-film semiconductor with mobility above 3 cm^2/V s and a-Si cannot achieve this value [1]. ZnO based thin-films can be used for this application as the switching transistor and driving transistor. In both cases threshold voltage stability is an important issue as driving transistor threshold voltage instability of only 0.1V could result in 20% change in luminance [2]. It is clear illumination stability is a critical issue as ZnO is a likely candidate for many future transparent and display applications where TFTs will be directly exposed to light in the visible spectrum. Prior work on ZnO-based semiconductor TFT bias-illumination instability has indicated that illumination typically causes or enhances negative threshold voltage shifts. Three mechanisms have been reported as governing these instabilities: photo generated interface/dielectric hole trapping, photo desorption of oxygen related molecules, and creation of photo excited donor states. In addition, reports have shown a dielectric dependence on light-induced instabilities of ZnO-based amorphous semiconductors [1-3]. The light-induced instabilities of nanocrystalline ZnO with HfO_2 gate dielectrics have not been investigated to date and are reported in this work.

Thin-films of ZnO and HfO_2 were deposited by pulsed laser deposition and atomic layer deposition, respectively, and device structures were fabricated using standard photolithography and etching techniques. TFT I-V parametric testing was carried out using a Keithley 4200 SCS with a temperature-controlled probe station. Individual TFTs from the same sample were diced apart and used for each photon energy experimental point. Each device's transfer curve was measured in a dark environment to serve as the control case and then illuminated with light of various wavelengths. Devices were illuminated for $8x10^3$ seconds with source, drain, and gate biases set to 0 volts. A transfer curve was measured at logarithmic time steps to capture the change in device parameters over the course of illumination. V_{TH} and μ were extracted from a linear fit of $\sqrt{I_{DS}}$ vs V_{GS} in the TFT saturation region. Initial device performance indicates typical values of V_{TH} = 1.5 V, μ = 24 cm^2/Vs, S = 140 mV/decade, and $I_{on}/I_{off} = 1x10^{10}$.

Illumination influenced results show clear trends of increased I_{OFF}, negatively shifted V_{TH} ($-\Delta V_{TH}$), and increased S with time. In addition, $+\Delta I_{OFF}$ and $-\Delta V_{TH}$ increase in magnitude with illumination photon energy. Analysis of extracted grain boundary trapped charge (N_{GB}) shows a strong correlation between decreased N_{GB} and $-\Delta V_{TH}$. Using a model developed for conduction by thermionic emission over grain boundaries in polycrystalline thin film transistors, a fit in trends between experimental transfer curves changing with illumination and modeled transfer curves changing with decreased N_{GB} indicate grain barrier charge plays a large role in the illumination instabilities in ZnO/HfO_2 thin film transistors. ΔI_{OFF} trends with time and photon energy can be explained by a modified thermionic emission model, where a photo-generated term is considered as an additional source of carriers.

Illumination studies will also be conducted on devices with SiO_2 gate dielectrics to elucidate the role of the dielectric and devices with backside passivation layers will also be investigated to study the role of ZnO surface or photo desorption induced states on illumination instabilities.

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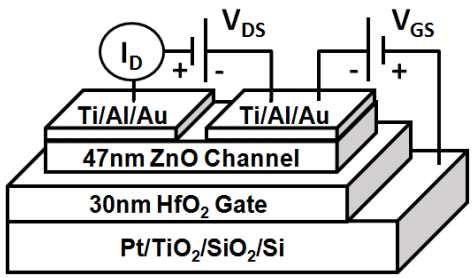

Figure 1: Schematic of HfO_2/ZnO TFT and biasing scheme during illumination (V_{GS} = V_{DS} = 0 V).

Color	Peak Wavelength (nm)	Radiation Energy (eV)	FWHM (nm)	Intensity (mW/cm^2)	Flux ($m^{-2}s^{-1}$)
Red	631	1.93	32	2.56	$8.1x10^{19}$
Green	525	2.36	65	2.43	$6.4x10^{19}$
Blue	452	2.74	61	2.75	$6.3x10^{19}$
UV	300 - 450	4.1 - 2.7	Not Gaussian	2.55	$4.7x10^{19}$ (for 375 nm)

Figure 2: Table indicating illumination sources' wavelength, energy density, and flux.

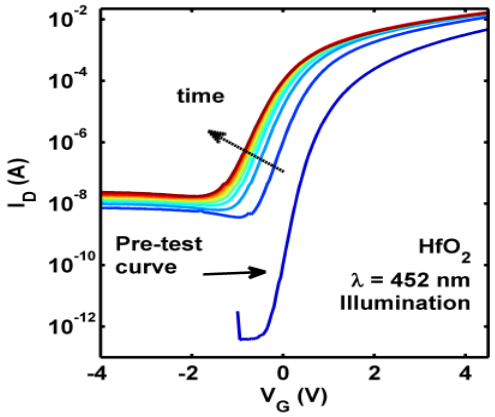

Figure 3: Series of transfer (I_D-V_{GS}) characteristics under λ = 452 nm illumination.

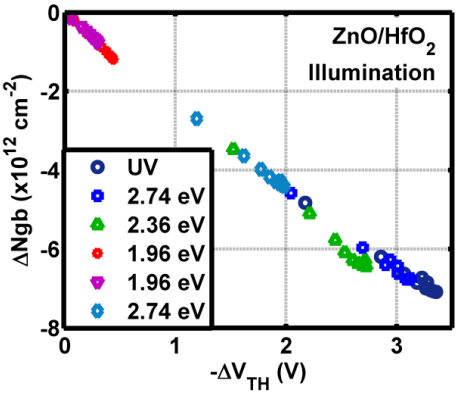

Figure 4: Plot of ΔN_{GB} vs $-\Delta V_{TH}$ indicating strong correlation over all illumination wavelengths.

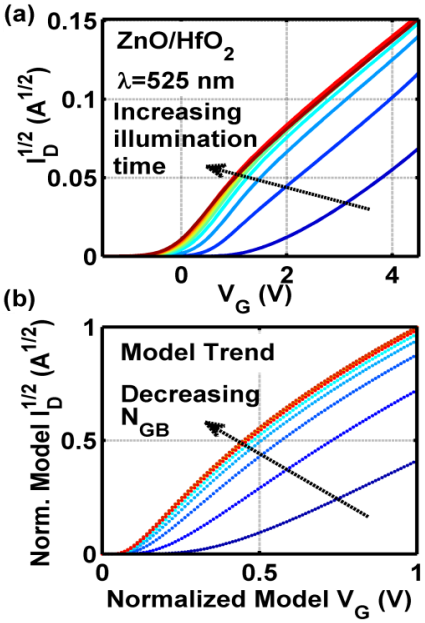

Figure 5: (a) Measured temporal dependence of I_D-V_G under illumination and (b) model of I_D-V_G with decreasing values of N_{GB}. Model trends agree with experimental trends.

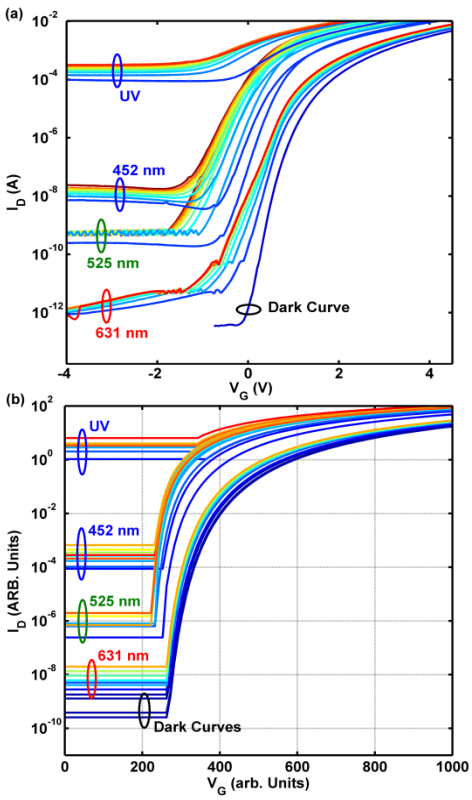

Figure 6: (a) Experimental I_D-V_G curves. (b) Modeled curves for thermionic emission above grain barriers modified by adding photo-generated carrier term, which dominates at off-state voltages.

1.4 kV Breakdown Voltage for MOCVD grown AlGaN/GaN HEMTs on Si substrate

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The growth of GaN transistors on Si substrate has received tremendous attention due to large size availability of Si substrates at low cost. However, it is imperative to demonstrate a high breakdown AlGaN/GaN HEMTs on Si grown by MOCVD as high power device applications are the primary significant contribution expected of a GaN based devices. In the past, we have demonstrated high breakdown on AlGaN/GaN HEMTs grown on Si by thickening the buffer layers [1-2]. All our previous reports were based on the 3-terminal OFF breakdown voltage (*3TBV*) measured on devices with short gate-drain (L_{gd} = 3 or 4 μm) spacing which limited the breakdown voltage due to Schottky gate leakage current [3]. Therefore, in the current investigation, we prepared HEMTs with various L_{gd} and studied its dependence on *3TBV*. We observed a *3TBV* of 1.4 kV for an AlGaN/GaN HEMT grown on Si having L_{gd} of 20 μm.

The MOCVD grown HEMT epi-layers used for this study as shown in Fig. 1 had a buffer thickness (T_{Buf}) varying from 1.25 μm to 5.0 μm and GaN thickness (T_{GaN}) varying from 0.5 to 2.0 μm. The purpose behind growing thick epi-layers is to minimize the threading dislocations which offer a high resistive i-GaN suitable for driving the device to higher breakdown voltage during *3TBV* measurement. The cross-sectional transmission electron microscopic image in Fig. 2 shows very high density of dislocations at the Si and buffer interface. But these dislocations are minimized as buffer thickness increased and one could see the i-GaN grown on 2.5 μm thick buffer has low dislocations (1.5×10^8 cm^{-2}) as understood from Fig. 2. Also from Fig. 3, it is evident that screw and edge dislocation densities (calculated from full width at half maximum (FWHM) peaks of x-ray diffraction) decrease gradually for GaN grown on thick buffers.

In order to investigate the resistive nature of i-GaN and buffer we measured the vertical breakdown voltage by etching the top 50 nm including 25 nm i-AlGaN [3]. Top electrode contact on i-GaN and a back Ohmic contact on p-Si were made for vertical *I-V* measurement. A plot of vertical breakdown voltage with T_{GaN} and T_{Buf} in the current study is shown in Fig. 4. From the normalized thickness of T_{GaN} and T_{Buf} it is understood that increasing T_{Buf} contributed more towards increasing the vertical breakdown voltage (Fig. 4(b)).

HEMTs with various L_{gd} (4 to 20 μm) were fabricated from these wafers for I_d-V_d and breakdown voltage measurements. From the I_d-V_d characteristics measured at V_g = +1.5 V, the drain resistance (R_d) calculated (Fig. 5) shows an increase in R_d with L_{gd}. However, we found R_d is lowered as the total thickness of epi-layer increased which is attributed to improved crystal quality and better confinement of electrons at the 2DEG channel lowering its channel resistance. For *3TBV* measurement, the samples were immersed in Fluorinert and substrate grounded. The summary of *3TBV* for devices with T_{GaN} = 1.0 μm shown in Fig. 6 reveals a distinct increase in the breakdown voltage with T_{Buf}. For L_{gd} less than 6 μm, very small increase in the breakdown voltage was observed with regard to increase in T_{Buf} because of the Schottky gate leakage driven breakdown. However, for L_{gd} exceeding 6 μm there was a drastic increase in the breakdown voltage for every increase in T_{Buf}. And therefore, the contribution of T_{Buf} to *3TBV* is clearly evident in the devices having L_{gd} > 6 μm. For every thickness of buffer, it appears that breakdown saturates for L_{gd} around 15 μm. A highest breakdown of 1402 V was observed for T_{GaN} of 2.0 μm grown on T_{Buf} of 5.0 μm as shown in Fig. 7. Further, we did not observe any two-step breakdown (sudden surge in the leakage current without undergoing a final breakdown) [3] for devices grown on thick buffer. In Fig. 8, the *specific-on resistance* (R_{on} x A) of our devices are compared with the state-of-the art results by other groups [4-5]. A figure of merit ($FOM = BV^2/R_{d\text{-}on}$) of 2.6×10^8 V$^2\Omega^{-1}$cm^2 was calculated for this device.

In order to demonstrate a high three-terminal off breakdown voltage for AlGaN/GaN devices grown on Si, we have suppressed the leakage currents both in the lateral and vertical direction by growing high resistive GaN using thick buffer. A very high breakdown voltage of 1.4 kV was observed for devices fabricated on these devices with large L_{gd}.

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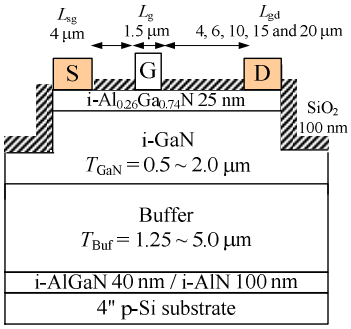

Fig.1. SiO_2 passivated HEMTs with varying buffer (T_{Buf}) and GaN (T_{GaN}) thicknesses were fabricated with different L_{gd} (4 to 20 µm).

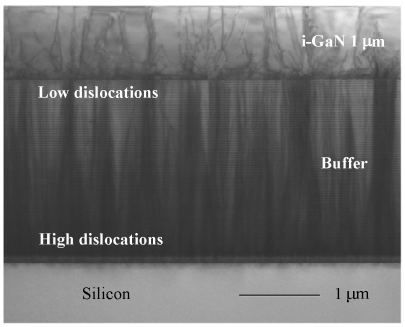

Fig. 2. TEM image shows a high density of dislocations at the GaN/Si interface. These dislocations are reduced when the thickness of epi-layer is increased.

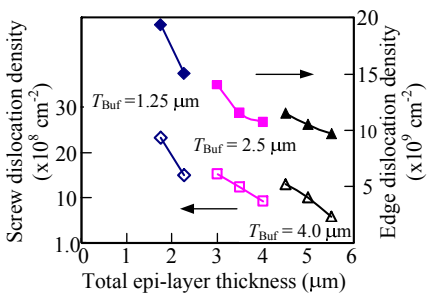

Fig. 3. Screw and edge dislocation densities as calculated from the XRD-FWHM values.

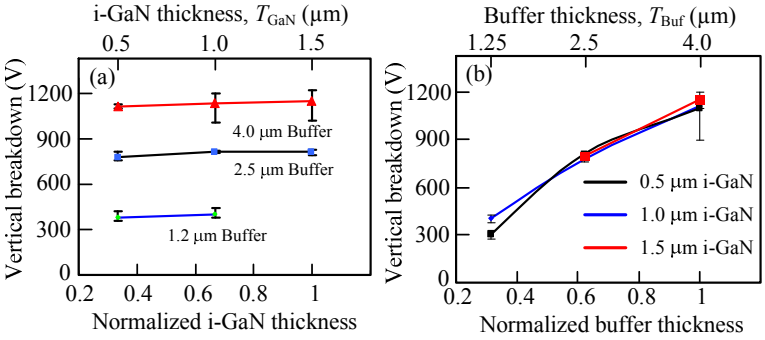

Fig. 4. A large improvement in vertical breakdown was observed for increasing buffer thickness compared to increasing GaN thickness.

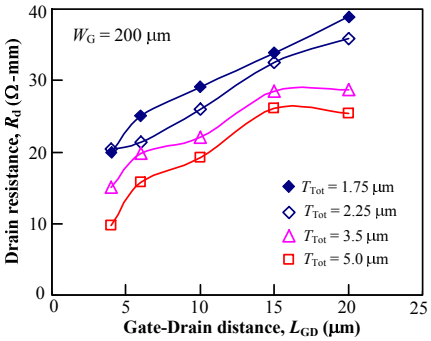

Fig. 5. Drain resistance *vs* L_{gd} for HEMTs shows a considerable decrease in R_d as the total thickness of the epi-layer is increased.

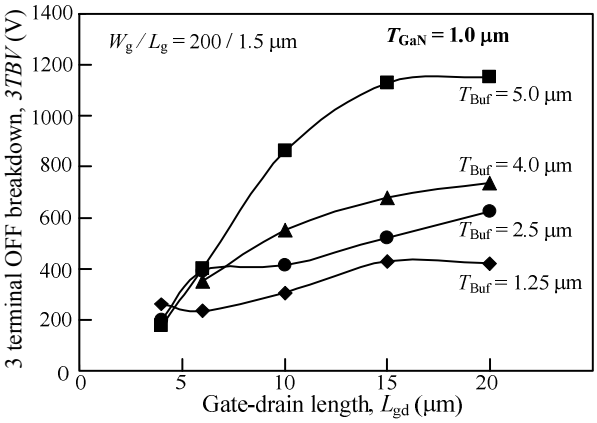

Fig. 6. Summary of *3TBV* measured for HEMTs having 1.0 µm T_{GaN} grown on different T_{Buf} with different L_{gd}.

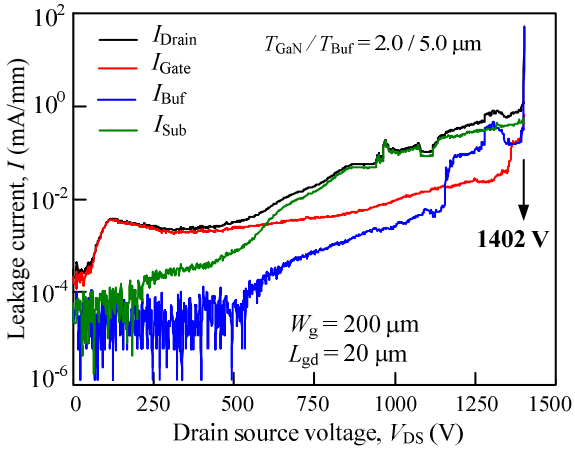

Fig. 7. A highest *3TBV* of 1402 V for L_{gd} of 20 µm was observed for our AlGaN/GaN HEMT having 5 µm buffer thickness.

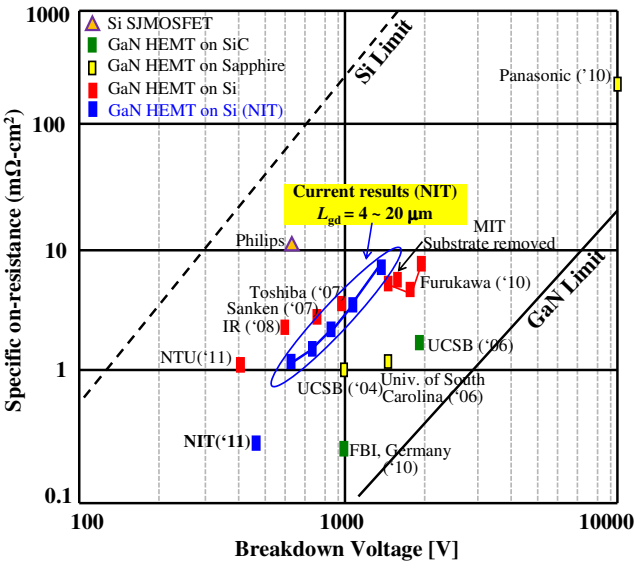

Fig. 8. Specific on-resistance *vs* three-terminal off-breakdown voltage of our devices compared with other groups. Specific on-resistance was calculated using R_{on} x A.

Dopant Straggle-free Heterojunction Intra-band Tunnel (HIBT) FETs with Low Drain-induced Barrier Lowering/Thinning (DIBL/T) and Reduced Variation in OFF Current

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We propose heterojunction intra-band tunnel (HIBT) FETs with reduced sensitivity of OFF current (I_{OFF}) to parameter variations (PV) and lower drain-induced barrier lowering/thinning (DIBL/T) compared to Si double gate (DG) MOSFETs. We evaluate the impact of low I_{OFF} variations in HIBT FETs on SRAM leakage and stability and show their potential for low power applications.

Device Structure: In an HIBT-FET, different semiconductor materials are used for source/drain (S/D) and channel so that a heterojunction is formed between S/D and channel regions (Fig. 1). Two requirements for S/D and channel materials are: (a) matched lattice constants and (b) a positive conduction band offset (CBO) from S/D to channel for an n-type device (Fig. 2). One of the material-pairs which meet the requirements for n-type HIBT FETs is Si-GaP (Si S/D and GaP channel – Fig. 1). In order to fabricate Si-GaP HIBT FETs, vertical growth of Si source, GaP channel and Si drain is required, similar to the technique followed in [1].

Heterovalent materials in S/D and channel (i.e. group IV S/D and III-V channel materials) make the Si-GaP HIBT FETs dopant straggle-free. The Si S/D regions are doped with phosphorus (P) atoms. However, when P atoms diffuse into the channel, they do *not* act as dopants for the GaP channel leading to abrupt S/D junctions (Fig. 2(a)). As a result, HIBT FETs exhibit tolerance to variations due to dopant straggle. (Note, cross-doping of GaP with Si is neglected, as suggested in [2]). Other important attributes of HIBT FETs are: (a) symmetric device structure which leads to equal bi-directional drain current and (b) absence of ambi-polar conduction [3] due to large bandgap of Si S/D. We now discuss the device characteristics of HIBT FETs and compare them with Si DG MOSFETs. The analysis is based on ballistic non-equilibrium Green's function (NEGF) models, solved self-consistently with Poisson's equation [4].

Device Characteristics: Conduction band offset (CBO) in HIBT FETs results in higher OFF state energy barrier compared to Si homojunction DG MOSFETs. Lower gate workfunction (Φ_G) is used for HIBT FETs to achieve similar OFF state energy barrier (Fig. 2(a)) as Si DG MOSFETs. As a result, HIBT FETs and Si DG MOSFETs exhibit equal sub-threshold current (I_{SUB}) at supply voltage (V_{DD}) = 0.7V (Fig. 3(a)). Note, the transport mechanism in the OFF state is thermal injection of carriers over the energy barrier. In contrast, carrier transport in the ON state occurs by intra-band tunneling (Fig. 2(b)), resulting in degradation in ON current (I_{ON}) (Fig. 3). However, HIBT FETs show a large improvement in DIBL/T and output conductance (g_{DS}), compared to Si DG MOSFETs (Fig. 3). This can be attributed to CBO at the S/D-channel interfaces which limits the impact of drain electric field on the carrier injection at the source.

Comparison of the gate currents (I_G) of the two devices (Fig. 3(a)) shows that HIBT FETs have comparable OFF state gate current (I_{GOFF}) but higher ON state gate current (I_{GON}). This is because in the ON state, direct tunneling current (I_{DT}) is the dominant component of I_G. Higher I_{DT} in HIBT FETs is the result of (a) lower tunneling barrier at the GaP-gate dielectric interface compared to the Si-gate dielectric interface and (b) lower Φ_G. In the OFF state, edge tunneling current (I_{ET}) is the dominant component of I_G. Abrupt S/D junctions in HIBT FETs lead to reduced carrier concentration in the vicinity of S/D and tend to lower I_{ET}. On the other hand, lower gate tunneling barriers in HIBT FETs tend to increase I_{ET}. The overall effect is that the two devices have comparable I_{ET}. Note, I_{SUB} is significantly larger than I_{GON} and I_{GOFF} (Fig. 3(a)). This is because high-*k* gate dielectric (HfO_2 - Fig. 1) limits I_G, which has the following consequences: (a) the OFF current (I_{OFF}=I_{SUB}+I_{GOFF}) is almost equal to I_{SUB} and (b) although HIBT FETs have higher I_{GON} than Si MOSFETs, the total leakage (I_{OFF}+I_{GON} – sum of leakage in the OFF and ON states) is not significantly large (nominal values in Fig. 5).

Fig. 5 summarizes the comparison of HIBT FETs and Si DG MOSFETs. Since HIBT FETs are more suitable for low voltage (low frequency) applications because of low I_{ON}, we perform the analysis at V_{DD}=0.4V and 0.7V. HIBT FETs show improved DIBL/T and g_{DS} but also reduced I_{ON}-I_{OFF} ratio, marginally higher sub-threshold swing (SS), lower transconductance (g_m) and higher ON resistance (R_{ON}). However, a significant advantage of HIBT FETs is lower sensitivity of I_{OFF} to parameter variations (PV), which we discuss next.

Parameter Variations (PV): Figs. 4(a-b) show that the sensitivity (S) of I_{OFF} with respect to body thickness (T_{BODY}), oxide thickness (T_{OX}), spacer length (L_{SP}) and gate length (L_G) is significantly lower for HIBT FETs compared to Si DG MOSFETs and is attributed to CBO at the S/D-channel interfaces which reduces the impact of PV. Due to abrupt S/D junctions in HIBT FETs, S with respect to dopant straggle depth (σ_{DOP}) is zero. S due to device width (W) is similar while S due to Φ_G is mildly higher for HIBT FETs. Analysis for I_{ON} (Fig. 4(c-d)) shows reduced S for HIBT FETs with respect to T_{BODY} and L_G due to CBO, zero S with respect to σ_{DOP}, similar S for Φ_G and W and increased S for T_{OX} and L_{SP}. S for I_{ON} of HIBT FETs is large with respect to T_{OX} and L_{SP} because the tunneling barrier width is significantly affected by the change in T_{OX} and L_{SP}, resulting in large variation in intra-band tunneling current. An analysis of the joint effect of variations in all the parameters on the device characteristics (Fig. 4) shows significant reduction in I_{OFF} variations for HIBT FETs compared to Si DG MOSFETs, with lower I_{ON} variations at V_{DD}=0.4V and mildly higher I_{ON} variations at V_{DD}=0.7V. Fig. 5 summarizes the comparison of device metrics of HIBT FETs and Si DG MOSFETs for nominal case and considering worst case variations in all parameters. Significant reduction in I_{OFF} and I_{GON}+I_{OFF} (total leakage) is observed for HIBT FETs, considering worst case PV. The trends for other device metrics under PV are similar to those in the nominal case. Due to large reduction in variation in leakage and I_{ON}-I_{OFF} ratio, HIBT FETs show suitability for low power SRAMs, in which V_{DD} scaling is limited by cell stability requirements in the presence of variations rather than the performance constraints. We now present the leakage and stability analysis of HIBT FET based 6T SRAMs.

HIBT FET based 6T SRAMs: We analyze a hybrid 6T SRAM (Fig. 6 (b)) with HIBT FETs as pull-down (PD) and access (AX) transistors and Si p-MOSFETs as pull-up (PU) transistors. We compare HIBT FET SRAM with Si DG MOSFET SRAMs (Fig. 6(a)) considering worst case PV at V_{DD}=0.4V. Low I_{OFF} variations in HIBT FETs leads to a large reduction in cell leakage of HIBT FET SRAM under PV (Fig. 6 (c)) compared to Si DG MOSFET SRAM. Higher hold and read static noise margins (SNM) are observed in HIBT FET SRAMs at low V_{DD} under PV. This is due to lower variation in I_{ON}-I_{OFF} ratio in HIBT FETs. HIBT FET SRAMs also show higher write margin (WM) at low V_{DD}. This is because higher g_m in Si p-MOSFETs compared to HIBT FETs leads to sharper decrease in the strength of PU compared to AX as V_{DD} is lowered, leading to increase in WM.

Conclusion: The proposed HIBT FETs exhibit low I_{OFF} variations due to the conduction band offset (CBO) and absence of dopant straggle. As a result, HIBT FET based SRAMs exhibit a large reduction in SRAM cell leakage and higher cell stability at low V_{DD} under parameter variations, compared to Si DG MOSFET based SRAMs. This makes HIBT FETs suitable for low-voltage low-power SRAMs.

Acknowledgements: This work was supported in part by Intel and NSF.

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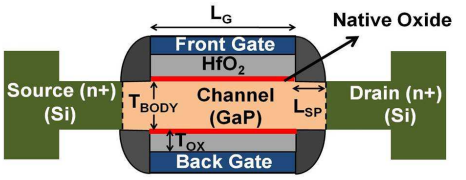

Channel Material	HIBT Si DG	GaP Si
Source/Drain Material		Si
Lattice Constant	GaP Si	5.45 A 5.43 A
Gate Dielectric	HIBT Si DG	HfO_2+Ga_2O_3/$GaPO_4$ HfO_2+SiO_2
Physical Gate Length (L_G)		10.8nm
Body Thickness (T_{BODY})		4.5nm
Physical Oxide Thickness (T_{OX})		2.4nm
Spacer Thickness (L_{SP})		2.4nm
Gate Workfunction (Φ_G)	HIBT Si DG	4.08eV 4.4 eV
Body Doping		Intrinsic
Source/Drain Doping		$10^{20}cm^{-3}$
Phosphorous Straggle (σ_{DOP})		1.5nm/decade

Fig. 1 Device structure of Heterojunction Intra-band Tunnel (HIBT) FET showing different semiconductors in source/drain and channel. Device parameters for HIBT and homojunction Si DG MOSFETs are shown in the table.

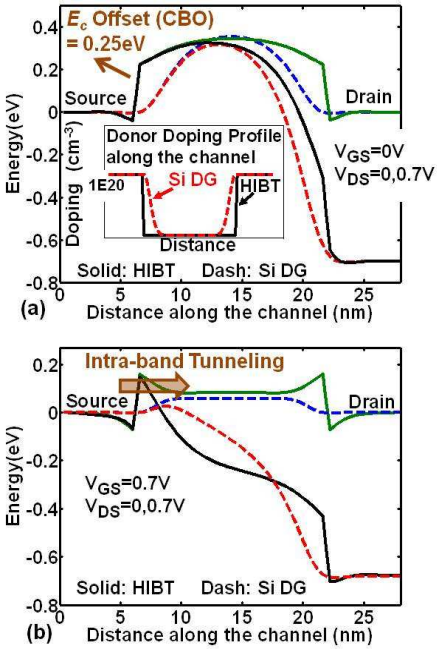

Fig. 2 Conduction band of HIBT and Si DG MOSFETs showing conduction band offset (CBO) and intra-band tunneling barrier in HIBT FETs. Inset : Abrupt S/D junction in HIBT FETs due to the dopant straggle-free nature of Si-GaP HIBT FETs.

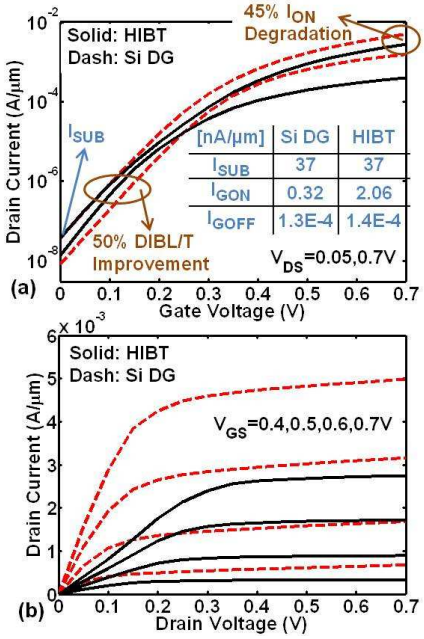

Fig. 3 (a) I_D-V_{GS} and (b) I_D-V_{DS} characteristics of HIBT and Si DG MOSFETs. Fig. 2(a) also shows that sub-threshold current (I_{SUB}) is much larger than the gate currents in ON (I_{GON} -V_{GS}=0.7V, V_{DS}=0V) and OFF (I_{GOFF}-V_{GS}=0V, V_{DS}=0.7V) states.

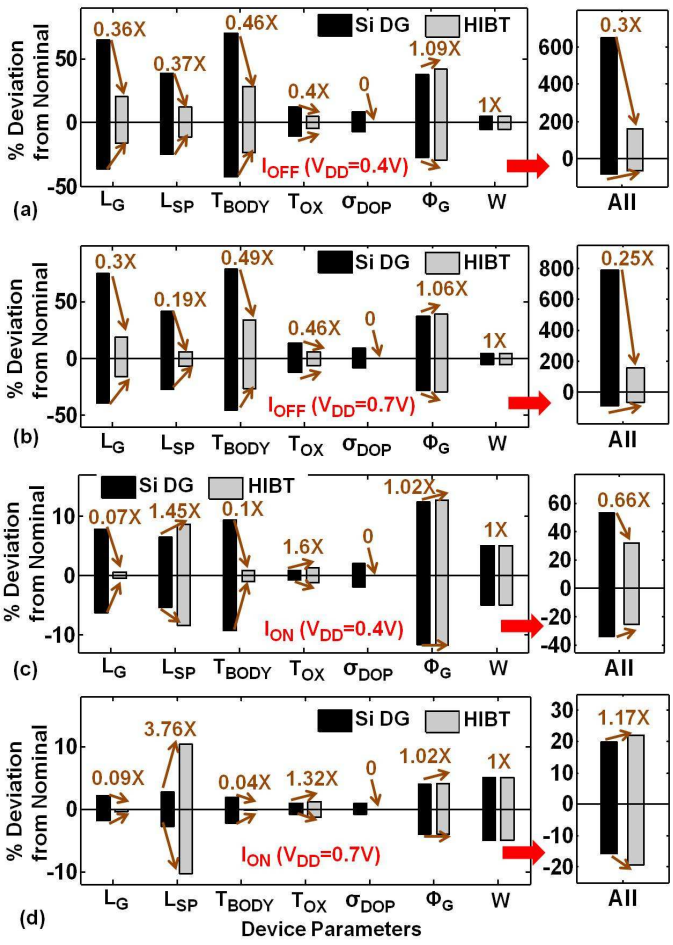

Fig. 4 Variation of I_{OFF} and I_{ON} with respect to device parameters for HIBT and Si DG MOSFETs at V_{DD} = 0.4V and V_{DD} =0.7V. Range of variation in Φ_G = ±10mV. Range of variation in other device parameters ~ ±5-10% of the nominal value. Numbers on the bars are the ratio of the variation range of HIBT FETs with respect to Si DG MOSFETs. 'All' refers to variations in all device parameters.

Metric	V_{DD}=0.4V		V_{DD}=0.7V	
	Nominal	Worst Case	Nominal	Worst Case
I_{ON}	0.56X	0.63X	0.55X	0.53X
I_{OFF}	1.28X	0.45X	1X	0.29X
I_{GON}	4.6X	4.4X	6.5X	6.6X
I_{OFF} + I_{GON}	1.28X	0.45X	1.05X	0.29X
SS	1.04X	1.04X	1.07X	1.03X
DIBL/T	0.5X	0.41X	0.5X	0.4X
g_m	0.56X	0.58X	0.57X	0.51X
g_{DS}	0.18X	0.16X	0.26X	0.27X
R_{ON}	2.6X	2.5X	2.9X	3.2X

Fig.5. Ratio of device metrics of HIBT FET to Si DG MOSFETs ($Metric_{HIBT}/Metric_{SiDG}$) for nominal case and considering worst-case process variations in all device parameters. Range of variation in Φ_G = ±10mV. Range of variation in other device parameters ~ ±5-10% of the nominal value.

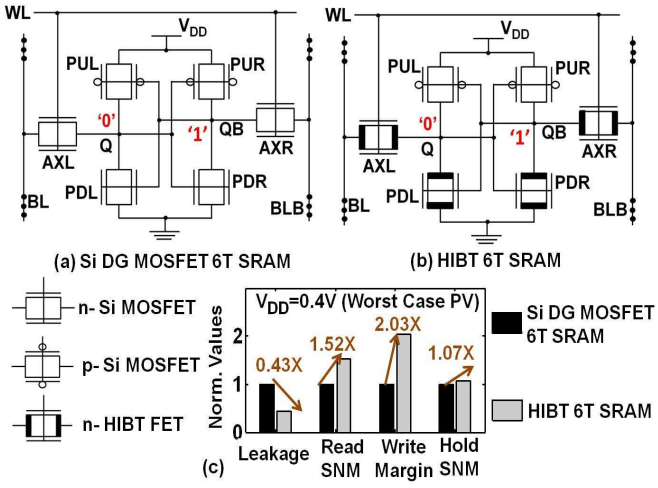

Fig. 6 Schematic of (a) Si DG MOSFET SRAM (b) HIBT FET SRAM with HIBT access and pull-down transistors and Si PMOS pull-up transistors and (c) comparison of leakage, read static noise margin (SNM), write margin (WM) and hold SNM of low voltage HIBT FET based and Si DG MOSFET based 6T SRAMs, considering worst case process variations in all n- and p- transistors.

Exclusive Electrical Determination of High-Resistance Grain-Boundaries in poly-Graphene

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Background. Single layer graphene (SLG), with high optical transparency and electrical conductivity, may potentially be used as flexible transparent electrode in photovoltaics, photo detectors, and flat panel displays. While its optical transmittance exceeds 95% (significantly better than most traditional materials), its sheet resistance (ρ_{poly-G}) must be reduced below 10-20Ω/□ for viable replacement of present Transparent Conducting Oxides (TCOs) like Indium doped Tin Oxide (ITO). However, large scale CVD SLG is typically polycrystalline, consisting of many grains, with neighboring grains separated by high- and low-resistance grain boundaries (HGB and LGB), see Fig. 1 and 7. The HGBs severely limit the (percolating) electronic transport, so that $\rho_{poly-G} > 1000\Omega/\square$. It is therefore important to determine the electronic nature and *fraction* of HGB to improve transport in polycrystalline SLG.

Approach. While the macroscopic features of grains and GB have been mapped by variety of techniques [1], they cannot distinguish between LGB and HGB. Microscopic measurement of inter-GB electronic transport offers insight regarding *individual* HGB [2], but cannot estimate fraction of HGB in a large scale SLG that contains thousands of GBs [3]. In this work, we combine systematic electrical measurement of R_{poly-G} (L, T) and sophisticated theoretical model [3] to determine the HGB in SLG films. L and T represent the channel length of our two terminal devices and the temperature respectively. Optical transmission of the SLG sample is also presented.

Sample Preparation. The SEM image in Fig. 1 suggests the typical grain size of the SLG sample (from ACS Co., MA) is ~1μm. The CVD SLG grown on copper foil was transferred onto 1cm x1cm quartz substrate (0.5mm thickness), as shown in Fig.2. Circular TLM photo mask with 4 different channel spacings (L) were used to pattern the structure and a metal trilayer (Ti/Pd/Au of 1nm/30nm/20nm) was e-beam evaporated for the electrodes fabrication. Fig. 3 shows the top view of devices with an optical microscope.

*Results/Discussion.*The resistance of each device was measured at T=300K, 333K, 367K and 400K, and plotted in Fig.5. The ρ_{poly-G} was calculated from the median value of R_{poly-G} (L, T) , corrected for the shape factor [4]: $C = R_1 / s * \ln[(R_1 + s)/R_1]$, where s is the spacing of channel between inner and outer rings, R_1 is the radius of inner circle. The sheet resistance is obtained from: $R_s = \Delta R / \Delta s * [2\pi R_1]$. As shown in Fig. 6, at room temperature, the sheet resistance is 1225Ω/□, much smaller compared with what has been reported [5].

The temperature-dependence of R_{poly-G} (L, T) allows us to determine the fraction of HGB, as follows: As shown in Fig. 7, when T increases, the R_{GB}/R_{grain} ratio decreases (R_{grain} is the sheet resistance of grain), thus larger fraction of the current can pass through the HGB (the overall current is reduced due to the increased R_{grain}) We analyze the T-dependence of sheet resistance by a well-calibrated voronoi percolation model, where each grain is represented by only one node, with four resistors connected to the neighbor, see Fig. 8. A high-resistance GB are characterized by $R_{GB}^{(hi)} < R_{grain}$ and a low-resistance GB by $R_{GB}^{(lo)} \equiv R_{grain}$, and $R_{GB}^{(hi)} \sim 60 R_{GB}^{(lo)}$ at room temperature. For temperature dependence, it is assumed that GB resistance is insensitive to temperature (T) [6], and following recent experiments on a single crystalline graphene, grain resistance is proportional to T^5 [7]. Fig. 8 shows the sheet resistance (R_S) of poly-graphene samples normalized by R_S at 300K vs. temperature with respect to the percentage of high resistance GBs (P_{GB}). It can be seen that a computed results with P_{GB} between 40% and 50% offers a good match with measured data (percolation threshold ~ 66%), explaining why the film is so resistive (> 1000Ω/□). Our results confirm that a the measurement of R_{poly-G} (L, T), when interpreted by percolation model, provides a robust methodology to determine the percentage of high-resistance grain-boundaries in arbitrary poly-graphene samples.

+ These authors have equal contribution

* Corresponding author

[1] K. Kim et al., *ACS Nano*, vol. 5, p. 2142-2146 (2011); [2] Q. Yu et al., *Nat. Mater.*, vol. 10, p. 443-449 (2011); [3] C. Jeong et al., *Nano Lett.*, vol. 11, p. 5020-5025 (2011); [4] J.H. Klootwijkk et al., *Proc. IEEE*, vol. 17, p. 247-252 (2004); [5] Y. Zhu et al., *Adv. Mater.*, vol. 22, p. 3906-3924 (2010); [6] Private communication, Prof. Yong Chen's group in Purdue University; [7] S.V. Morozov et al., *Phys. Rev. Lett.*, vol. 100, p. 016602-1-4 (2008)

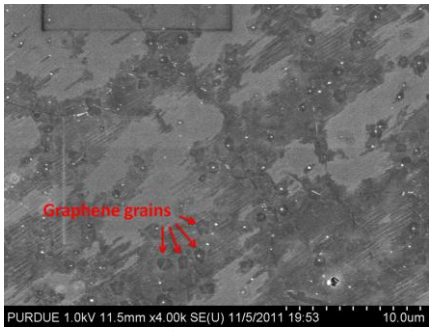

Fig.1 SEM image of SLG, showing grain size of approx.. 1μm

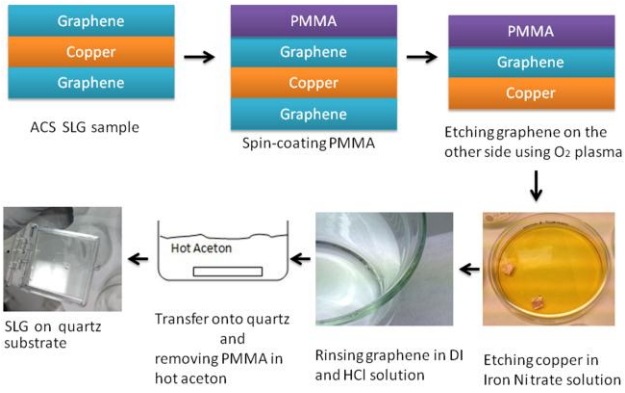

Fig.2 Overview of transfer procedure

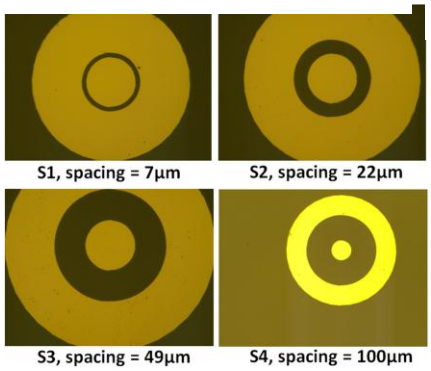

Fig.3 Top view of 4 types of circular TLM electrodes. The golden part is electrode & darker regions are SLG on quartz.

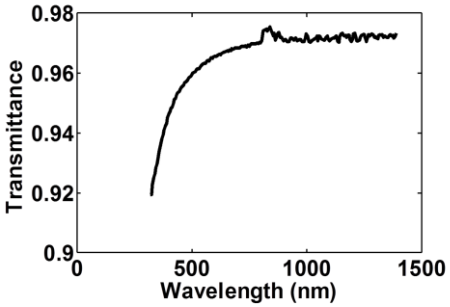

Fig.4 Optical transmittance spectrum of SLG in VIS-NIR range.

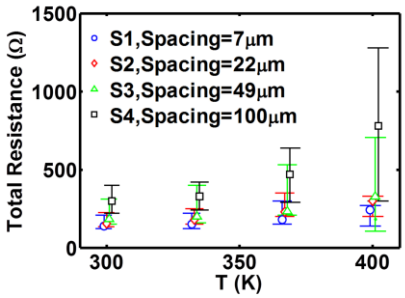

Fig.5 Measured temperature-dependence of resistance for circular electrode structures with 4 different spacings

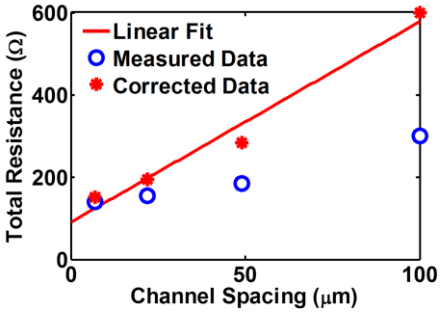

Fig.6 Resistance plotted versus channel spacing before (circle) and after (star) applying correction factors for circular structures. A sheet resistance of 1225Ω/□ is obtained from linear fit.

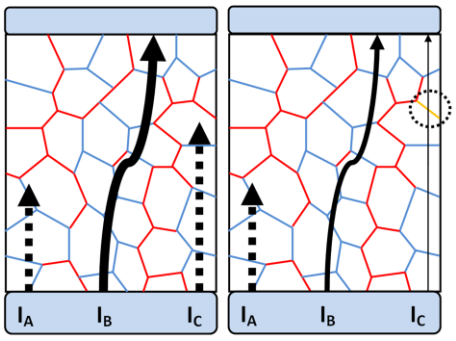

Fig. 7 The schematic figures to interpret the resistance of poly-graphene as a percolation problem defined by high and low resistance grain boundaries (GB), shown by red and blue line. High and low resistance GBs are shown by red and blue line, respectively. In the left picture, I_A and I_C are blocked, But I_B is stronger due to small R_{grain}. But when temperature increase, the R_{GB}/R_{grain} ratio decrease, there are more currents can pass through the GB barrier. Therefore in the right picture, I_B becomes less strong but there is a weak I_C passing through.

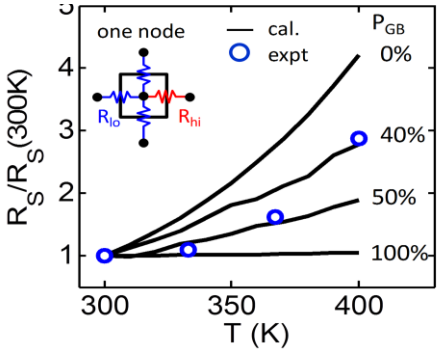

Fig.8 Measured sheet resistance (Rs) of poly-graphene samples versus temperature (normailized by R_S at 300K). Calculated curves are shown for various percentages of high resistance GBs (P_{GB}). It can be seen that a computed result with P_{GB} between 40% and 50% is in a good agreement with measured data

Improved OFF-state Breakdown Voltage in AlGaN/GaN HEMTs grown on 150-mm Diameter Silicon-on-Insulator (SOI) Substrate

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The AlGaN/GaN-based high-electron-mobility transistors (HEMTs) are suitable for discrete components in many high power and high frequency power electronics applications useful for communications, satellites, power amplifiers, inverters/converters for electric and/or hybrid vehicles. Presently, these devices are commonly grown on sapphire, silicon carbide, and recently on 100- to 200-mm diameter silicon substrates. For a large scale deployment of low cost GaN-based power electronic devices, silicon substrate offers tremendous opportunities due to mature back-end Si process technologies. However, GaN epilayers on large area Si substrates results in severe wafer bowing and cracking due to high thermal mismatch between nitride layer and the substrate. As an alternative to Si substrate, silicon-on-insulator (SOI) substrate has been used for the demonstration of GaN-based light emitting diodes (LEDs)[1]. To the best of our knowledge, the demonstration of AlGaN/GaN transistors on a thin SOI substrate is rather limited. In this study, we report on the growth and characteristics of AlGaN/GaN heterostructures (HSs) on 150-mm diameter Si(111) and SOI(111) substrates. In addition, fabrication of HEMTs and device characteristics will be discussed on the SOI platfrom.

The $Al_xGa_{1-x}N$/GaN HSs are grown on 150-mm SOI substrates by MOCVD. The 650 μm–thick SOI (111) substrates were prepared by the separation using implantation of oxygen (SIMOX) process. The burried SiO_2 and the top Si thicknesses are around 75-80 nm and 30-35 nm, respectively. The schematic layer structures of the nitride layers are shown in Fig. 1. For a comparitive study, similar AlGaN/GaN HSs were grown on 150-mm diameter and 650 μm-thick bulk Si (111) substrates. The cross-sectional scanning transmission electron microscopy (Fig. 2), high-resolution x-ray diffraction (Fig. 3), wafer bowing, and Hall measurements were performed to characterize the structural and electrical properties. A much lower wafer bowing of 25-40 μm range and an average sheet resistance (R_{sh}) of 350-360 Ω/sq., mobility (μ_H) of 1900-2000 cm^2/Vs and a maximum sheet carrier density (n_s) of 0.9×10^{13} cm^{-2} were obtained for several HEMT layers grown on thin SOI (111) as compared to the wafer bowing of 80 μm and an average R_{sh} of 430 Ω/sq, μ_H of 1600 cm^2/Vs and a maxmum n_s of 0.9×10^{13} cm^{-2} for the epilayer grown on bulk Si (111). The Al-content of 26% in $Al_xGa_{1-x}N$ is estimated by photoluminescence (PL) measurements (See Fig. 4).

The HEMTs with the gate-length (L_g) of 2 μm were fabricated on the AlGaN/GaN HSs grown on both Si and SOI substrates. The device fabrication details are similar to previously reported work [2]. The devices on both Si and SOI substrates exhibited good pinch-off characterstics (See Fig. 5) with maximum drain current density (I_{Dmax}) of 480 mA/mm & 510 mA/mm and maximum extrinsic transconductance (g_{mmax}) of 130 mS/mm & 120 mS/mm, respectively. With reference to the HEMTs on bulk Si, about 40% and 17% improvement is observed in 3-terminal off-state breakdown voltage (BV_{gd}) for the HEMTs on SOI with the gate drain spacing (L_{gd}) of 2 μm and 10 μm, respectively. This improvement is due to the reduction of substrate leakage current (I_{sub}) in the SOI substrate (See Fig. 8). The BV_{gd} as a function of L_{gd} will be discussed in the conference. Due to the improved structural, electrical properties and device breakdown voltage of HEMTs on SOI with the significant reduction of wafer bowing, our study shows that the GaN-on-SOI offers an alternate platform for high-power switching device applications.

[1] S. Tripathy et al., *Appl. Phys. Lett.* vol 91, p 231109 (2007).

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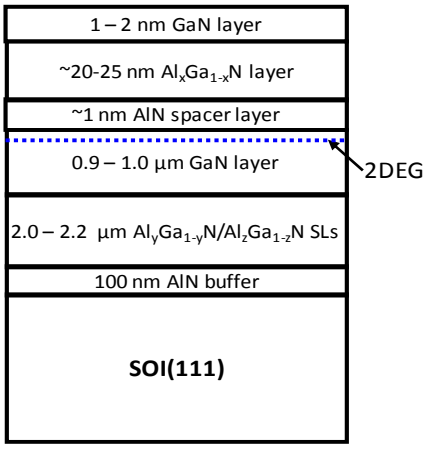

Fig. 1: AlGaN/GaN HEMT structures grown on 35 nm SOI (111).

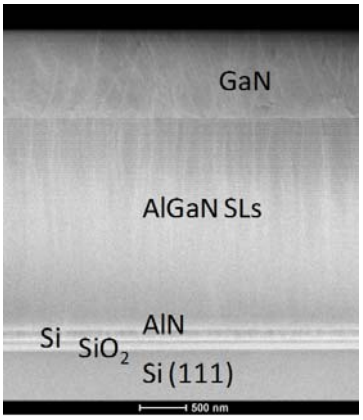

Fig. 2: Cross-sectional STEM image of HEMT structure on thin SOI (111).

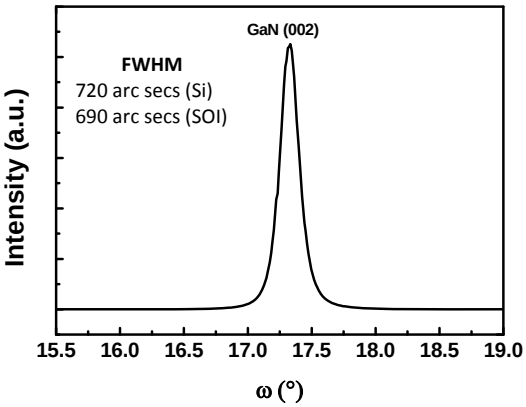

Fig. 3: HRXRD spectra of (0002) omega scan of the GaN/SOI (111).

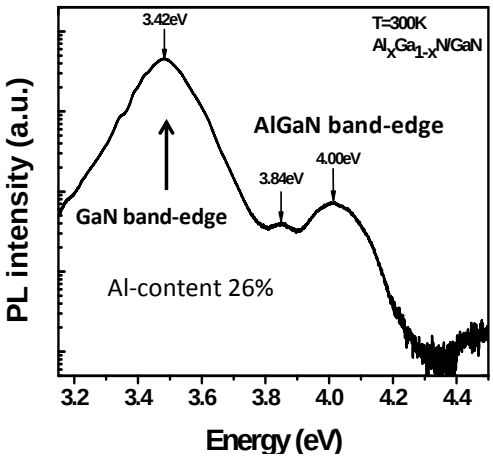

Fig. 4: Typical PL spectrum from AlGaN/GaN HSs on 150-mm SOI.

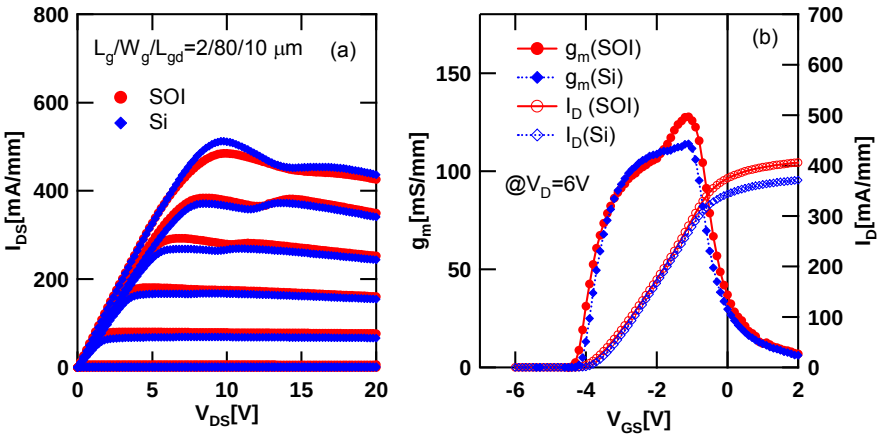

Fig. 5 (a) I_{DS}-V_{DS} and (b) transfer characteristics of AlGaN/GaN HEMTs on 150-mm diameter bulk Si(111) and SOI (111) substrate.

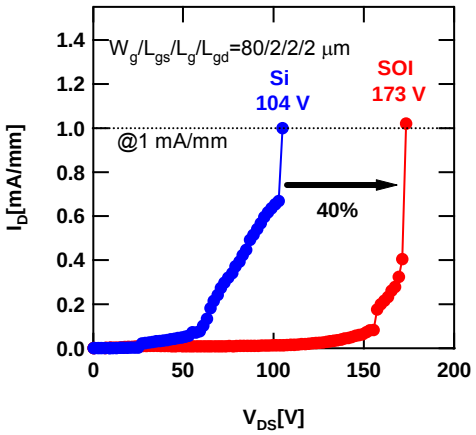

Fig. 6: OFF-state Breakdown voltage of AlGaN/GaN HEMTs on 150-mm diameter Si and SOI substrates. V_g=-6V. Breakdown strength is 0.87 MV/cm

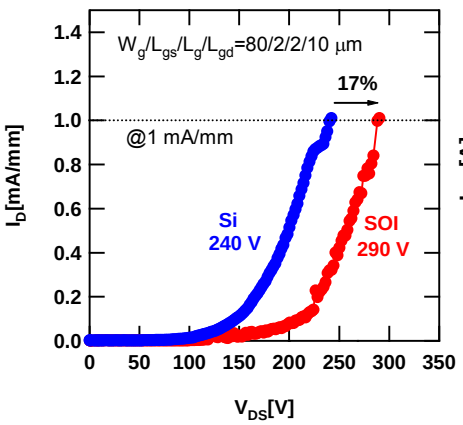

Fig. 7: OFF-state Breakdown voltage of AlGaN/GaN HEMTs on 150-mm diameter Si and SOI substrates. V_g=-6V

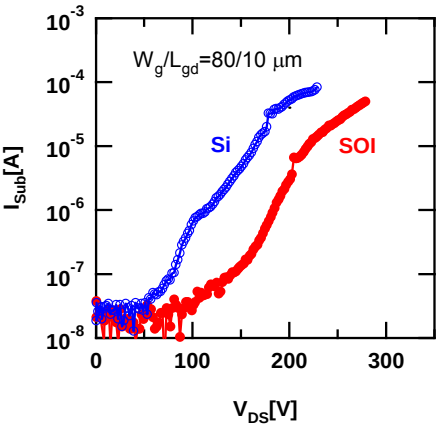

Fig. 8: Substrate leakage current of AlGaN/GaN HEMTs on 150-mm diameter Si and SOI substrates. V_g=-6V.

Improved Dual-Carrier High Gain Impact Ionization Engineered Avalanche Photodiode

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Avalanche photodiodes (APDs), which have light detection and amplification combined in a single stage, are crucial for infrared detection. They operate at a relatively high reverse bias to enable avalanche multiplication from impact ionization of electrons and holes. However, avalanche multiplication process can contribute to excess noise, which results from the non-uniformity of ionization of individual carriers. Based on McIntyre's Theory [1], one important key to minimize excess noise is to make impact ionization coefficient ratio, k, zero or infinity, which is pure electron or hole multiplication. Based on previous work [2], multiple novel dual carrier multiplication structures are simulated for the study of gain and excess noise factor. Such structures can achieve much higher gain compared to conventional APDs while minimizing excess noise factor through localization of impact ionization in thin multiplication layers.

Four structures are demonstrated in figure 1. Regions marked with "0", "1", "2" and "3" represent absorber, 10nm hole multiplication, 800nm electron multiplication and 10nm electron multiplication layers, respectively. Structure (a) has a single electron multiplication layer. But for others, we extend from a single thin hole impact ionization region placed next to a thick electron multiplication region, to multiple alternate thin hole and electron multiplication layers. 24Å InAs/ 24Å GaSb strained layer superlattice is used for pure electron multiplication region ("2", "3") and it is specifically lattice engineered using 14 band k.p model to have pure electron impact ionization (k=0). For hole multiplication region, GaxIn1-xSb has been used with x=0.02. Dead space multiplication theory [3] is used for gain and excess noise simulation. Since the doping levels of the multiplication regions are generally kept low, a uniform electric field is present in the direction from "2" to "0".

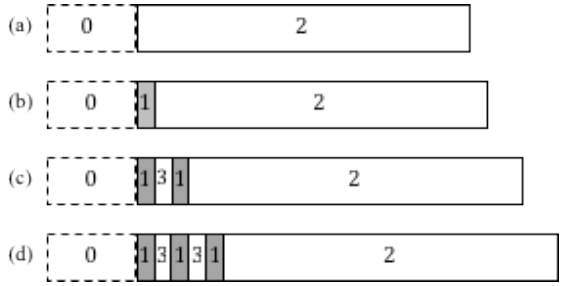
It is clear in figure 2 that with just adding five10nm multiplication layers in structure (d) compared to (a), a gain of 165.2 instead of 1.25 is achieved at a reverse bias around 2V which can be explained using dual carrier feedback. For instance, in structure (b), holes that are generated from impact ionization in wide electron multiplication region ("2") will drift into hole multiplication region ("1") under existing electric field and impact ionize if hole energy is higher than threshold. Then, secondary electron-hole pair is generated and its electron will enter electron multiplication region ("2") to impact ionize again. Also, for (c) and (d), with more and more thin layers alternatively added, not only impact ionization possibility increases, but also more and more feedback paths are created, thus much higher gain can be achieved. But with thin layers adding up, excess noise factor increases too. In figure 3, simulation is carried out to find out excess noise factor. From the figure, excess noise factor is getting higher from (a) to (d) at a certain gain. This is caused by homogeneity loss and uncertainty of where hole and electron will impact-ionize.

In figure 4, equivalent impact ionization ratios are simulated to study excess noise further. Simulation is done under an electric field of 20kv/cm with a dead space of 107nm and 170nm for hole and electron multiplication. Width of thin region is changed while keeping total width the same. Since thin regions are greatly thinner than dead space, carriers with enough energy can only impact ionize once. There is not enough space for a secondary carrier to build up energy higher than threshold energy. Thus, we can see equivalent impact ionization ratio (Kequ) is getting smaller when width of thin region is decreased. Also, that can explain figure 5 where excess noise factor is simulated while only changing impact ionization ratio of thin hole multiplication region. As long as we can keep hole impact ionization rate in thin hole multiplication region the same, gain and excess noise factor will not be affected whatever electron impact ionization rate is inside hole multiplication region.

Therefore, improved novel structure simulations of dual carrier multiplication are proposed. Such low-bias high -gain operation enables single photon counting and integration of it to Silicon ROIC. Dark current can be reduced due to lower electric field. Materials that are used for electron or hole multiplication are already proven useful for MWIR APDs. This structure is specially designed for MWIR, but not restricted for that.

[1] R. J. McIntyre," Multiplication noise in uniform avalanche diodes," IEEE Trans. Electron Devices, vol. ED-13, p.p. 164-168 (1966)
[2] S. Ghosh, K. Banerjee, Q. Duan, C. H. Grein, E. A. Plis, S. Krishna, M. M. Hayat, "Dual-carrier multiplication high-gain MWIR strained layer superlattice impact ionization engineered avalanche photodiodes", Proc. of SPIE Vol. 7660, 76601W-5 (2010)
[3] M. A. Saleh, M. M. Hayat, B. E. A. Saleh, M. Carl Teich, "Effect of dead space on gain and noise of double-carrier-multiplication avalanche photodiodes", IEEE Trans. On Elec. Devices, 39 (3) 546-552 (1992)

Fig. 1: (a), (b), (c), (d) are four structures with different multiplication regions. (a) is single carrier(electron) multiplication, (b), (c), (d) are dual carrier multiplication structures.
"0": absorber
"1": 10nm hole multiplication layer
"2": 800nm electron multiplication layer
"3": 10nm electron multiplication layer



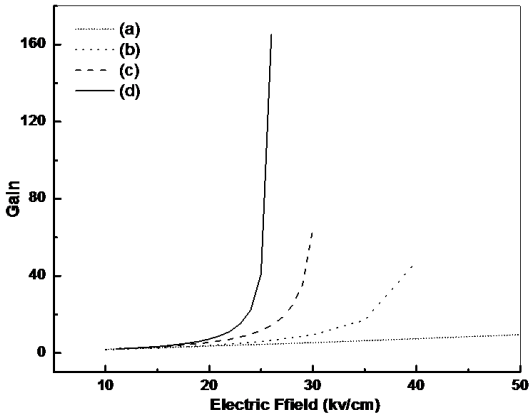


Fig. 2: Gain versus electric field for structures (a), (b), (c), (d), uniform electric field across structure are assumed.

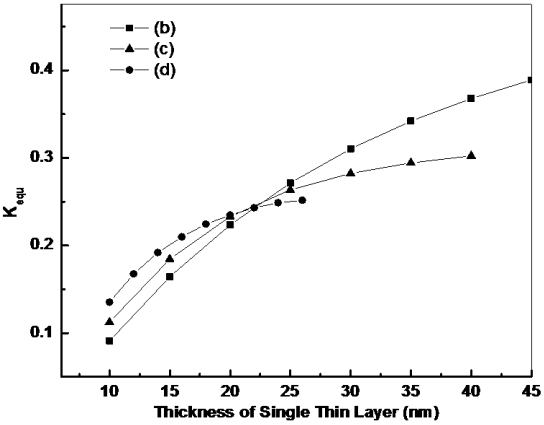


Fig. 4: For dual carriers structures (b), (c), (d), equivalent impact ionization ratio of overall structure with variation of width of single thin layer thickness

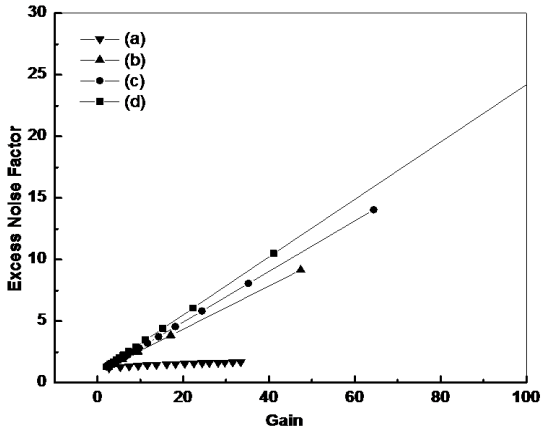


Fig. 3: Excess noise factors characteristics of structures (a), (b), (c), (d).

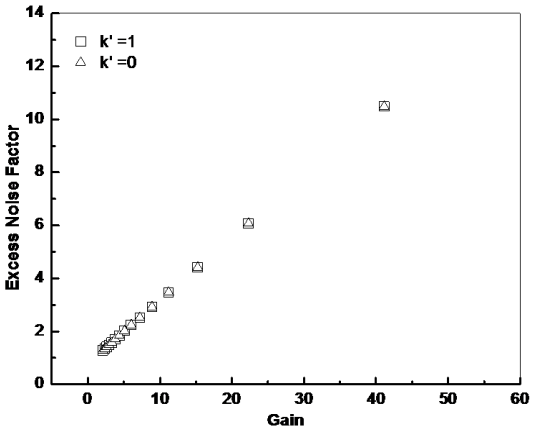


Fig. 5: Variation of excess noise factor with impact ionization ratio (k') in thin hole multiplication region ("1") for structure (d). Hole impact ionization rate is kept constant all the time.

Enhanced Tunneling Current in 1d-1d$_{Edge}$ Overlapped TFET's

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In order to reduce the power consumption of modern electronics, the operating voltage needs to be significantly reduced. Tunneling field effect transistors (TFET's) have the potential to do this. As shown in Fig 1, current can flow as soon as the conduction band and valence band overlap. However, the shape of the turn on is dependent on the density of states (DOS) of each band. The DOS can be controlled by changing the dimensionality of the device [1, 2].

One of the byproducts of pn-junction dimensionality analysis [1, 2] is that quantum confinement in the tunneling direction on either side of a tunnel junction greatly increases the tunneling current! This arises analytically, but here we derive added insights into the benefit of quantum confined tunneling through numerical simulation. This broadly validates the great increase in tunneling current, but reveals some new oscillatory features in the I-V curve that were previously unnoticed.

We compute the small bias conductance using 2d ballistic transport simulations within the nonequilibrium green's function (NEGF) formalism. We model the bandstructure using an 8×8 k.p Hamiltonian [3] and ignore the effects of strain. We take the electronic potential to be dropped entirely across the tunnel barrier and plot the conductance as a function of the overlap potential, V_{OL}, as shown in Fig 1.

First we consider the tunneling between GaSb/InAs quantum wires (1d:1d$_{edge}$) pn junctions as shown in Fig 2a. We choose the GaSb/InAs system because it has become accepted as the preferred material platform since it doesn't require heavy doping and has a favorable Type III, broken gap, band alignment. Gate electrodes can be added to the nanowires to control the overlap voltage V_{OL}. Assuming a continuum density of states model, the current should diverge upwards and then fall off as $1/\sqrt{V_{OL}}$ as shown by the dotted line in Fig 3 [2]. Conservation of energy and transverse momentum only allows current to flow at a single energy as shown in Fig 4a. This causes the shape of the conductivity curve to represent the 1d density of states (DOS) at the tunneling energy as shown in Fig 4b. However, in small devices, the 1d DOS does not form a continuum, but rather a series of individual levels as shown in Fig 4c. This is because the transmission probability is maximized when matching wave vectors fit in the 40 nm overlap on each side of the junction. This is illustrated in Fig 5. As seen in Fig 3, this causes the actual shape of the conductivity to be dominated by an oscillatory behavior, but only the first peak is relevant in a switching device. Except for the conductivity oscillations, the analytical continuum approximation and the more exact numerical 1d:1d$_{edge}$ curves in Fig 3 are similar.

Now we introduce the 2d:2d$_{edge}$ pn junction which simply eliminates the quantum confinement in the tunneling direction Fig. 2b. Once again gates can be added on top of the quantum wells to control the overlap potential V_{OL}. We see in Fig. 3 that without quantum confinement in the tunneling direction (2d:2d$_{edge}$ junction) the magnitude of the conductivity is 10 times lower than the 1d:1d$_{edge}$! Counter-intuitively, shrinking the device and truncating the quantum wells increases the conductivity. This is because the quantum confinement increases the rate of tunneling attempts on both sides of the junction and improves the wavefunction overlap between each side of the junction.

By using quantum confinement along the tunneling direction, the conductivity of TFET's is significantly increased. This will help overcome the limited current drive capability of TFET's.

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[2] S. Agarwal E. Yablonovitch, submitted to *Physics Review B*, arXiv:1109.0096 [cond-mat.mes-hall]

[3] B. A. Foreman, *Physical Review B*, vol 59, pp. 12748-12751, Nov 1997

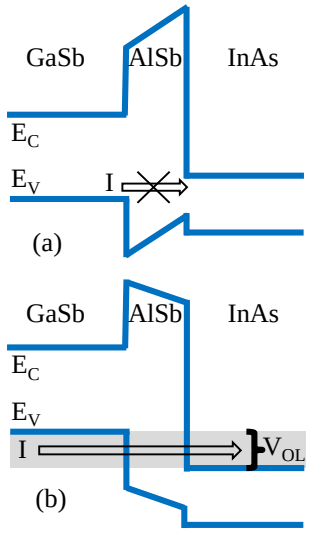

Fig 1: (a) No current can flow when the bands do not overlap. (b) Once the bands overlap, current can flow.

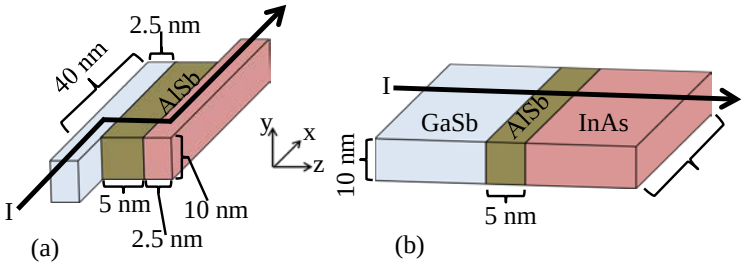

Fig 2: (a) We model tunneling between two coupled nanowires ($1d\text{-}1d_{edge}$) and (b) between two quantum wells ($2d\text{-}2d_{edge}$) with the same AlSb barrier. Except for the added confinement along z, the nanowires are identical to the quantum wells.

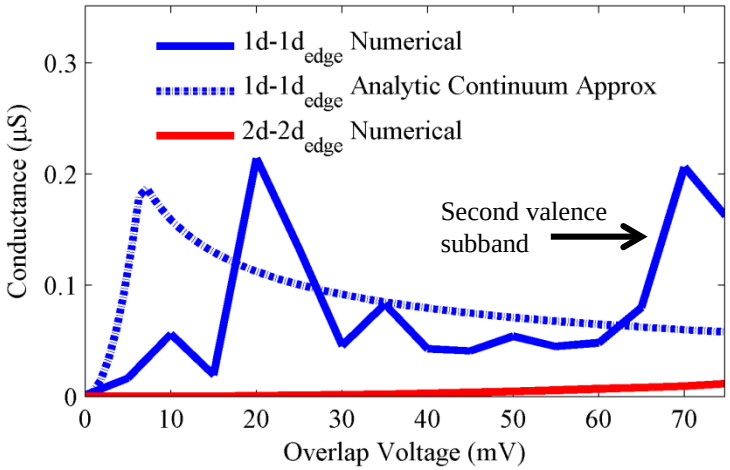

Fig 3: The $1d\text{-}1d_{edge}$ conductance in is plotted as a function of V_{OL}. We see that it is 10 times larger than the $2d\text{-}2d_{edge}$ conductance and that numerical calculation oscillates as a function of V_{OL}.

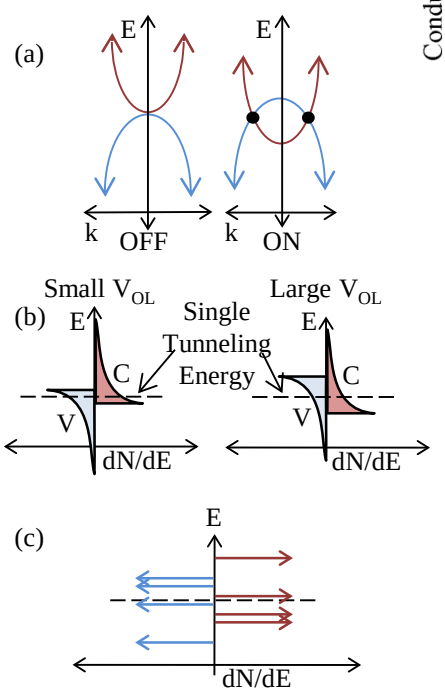

Fig 4: (a) There is only a single tunneling energy because of the conservation of energy and momentum. (b) The 1d density of states at the tunneling energy is different at different overlap voltages. (c) In small devices the 1d DOS is actually a series of individual states.

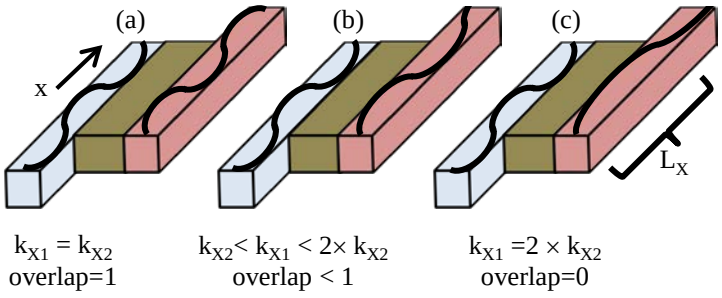

Fig 5: (a) When the transverse momentum, k_X, is the same in both nanowires, the transverse overlap integral is 1 and the conductivity is high (b) When k_X is slightly different on each side the transverse overlap integral starts to fall (c) When the k vectors differ by a multiple of π/L_X the overlap integral drops all the way to zero

Metal Contacts to MoS_2: a Two-Dimensional Semiconductor

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With increasing demands for electrostatic control as scaling continues in today's transistors, low dimensional structures continue to gain attention as a pathway for future device scaling because they offer excellent electrostatic control while remaining compatible with straightforward lithography techniques. In particular, MoS_2 has attracted interest for transistor applications because its large band gap allows for field effect devices with low off-current, unlike graphene [1]. One key bottleneck, however, is the realization of ohmic contacts on MoS_2 to improve FET device on-state performance. With this in mind, we evaluate Ni and Pd contacts on MoS_2 as potential alternatives to the already realized Au-MoS_2 and Ti-MoS_2 contacts [1]. Back-gated transfer length method (TLM) structures with Au, Ni, and Pd contact metals were fabricated on exfoliated MoS_2 flakes, with 300nm SiO_2 on degenerately doped Si as the substrate. The data indicate that Ni, like Au, makes an ohmic contact to the n-doped MoS_2 while the Pd metal contact shows Schottky behavior.

Figure 1 shows the alignment of the metal work-functions to the MoS_2 bands for the high work function metals on which we focus in this work. Figure 2 shows representative I_d-V_{ds} characteristics at V_{bg}=50V for the three contact metals on MoS_2. The MoS_2 flake thicknesses are 5nm for Ni and 6nm for Au, measured by AFM, and ~13nm for Pd, estimated by optical contrast. One finds that the Ni and Au contacts are ohmic while the Pd contact shows Schottky behavior. Figure 3 shows the contact resistance (R_c) as a function of back-gate voltage (V_{bg}), extracted using the TLM. R_c for Ni and Au are found to be comparable, with a minimum R_c of about 4.5Ω.mm at V_{bg}=50V. The gate-dependent R_c reflects the gate modulation of the potential barrier at the metal-MoS_2 interface. Considering charge-transfer at the metal-MoS_2 interface alone for these high work function metals, the different contact nature of Pd from Ni and Au is somewhat unexpected. Indeed, recent *ab inito* calculations suggest that the modification of the electronic states at the interface by the metal is the key to understanding the contact to MoS_2, going beyond the simple charge-transfer considerations of a metal-semiconductor junction [2]. To investigate the Ni contact further, R_c was measured at low temperature via TLM, as shown in Figure 4, for a ~6nm thick flake, as estimated by optical contrast. The R_c varies weakly with temperature, increasing by less than a factor of two from 238K to 78K for any V_{bg}. Enabled by the low temperature Ni ohmic contact, the sheet resistance and mobility of MoS_2 could be extracted as shown in Figure 5. The mobility, extracted from fits to the sheet resistance as a function of V_{bg}, is determined to be 48 cm^2/Vs at 289K, increasing to 237 cm^2/Vs at 78K due to decreased phonon scattering. The mobility of MoS_2 could be significantly improved to several hundred cm^2/Vs if its surface is passivated by atomic-layer-deposited dielectrics. [1, 3] The temperature dependence of the mobility is power law, $\mu \sim T^{-\gamma}$, where γ=1.36 for T=130K and above.

In conclusion, studies of Ni, Au, and Pd metal contacts on MoS_2 reveal that Ni, like Au, is ohmic while Pd shows Schottky contact behavior. Contact resistance for Ni and Au are comparable, with a minimum R_c for both metals of about 4.5Ω.mm at V_{bg}=50V.

References

[1] B. Radisavljevic et al, *Nature Nanotechnology*, **6**, 147 (2011).
[2] I. Popov et al, *Physcial Review Letters*, **108** (2012).
[3] H. Liu and P.D. Ye, *IEEE Electron Device Letters* (in press).

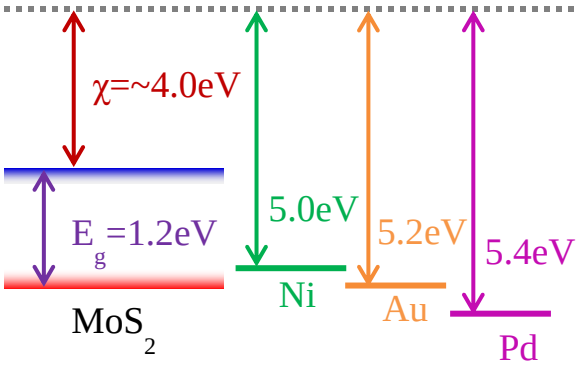

Figure 1: Band diagram showing the work function alignment of the contact metals to MoS_2

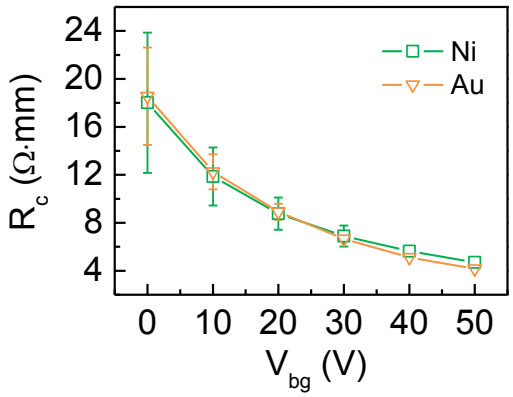

Figure 3: R_c extracted from TLM as a function of gate voltage for Ni and Au contact metals at V_{ds}=50mV. Error bars are determined from the liner fit used to extract R_c. Error bars are omitted for those smaller than the size of the symbol.

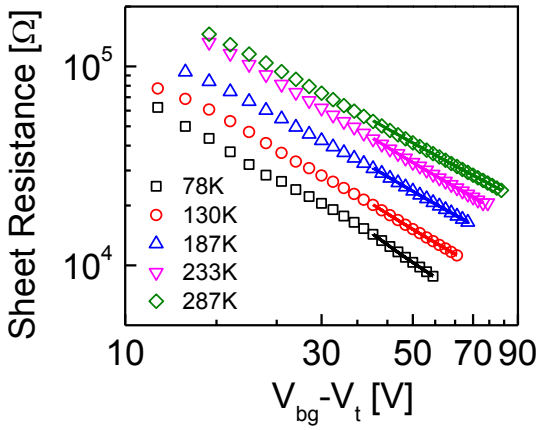

Figure 5: Symbols: Experimental sheet resistance of MoS_2 extracted at V_{ds}=50mV as a function of V_{bg}-V_t for different temperatures for an Ni TLM device. V_t is taken as the V_{bg} where I_d is 10nA. Solid lines: $R_{sheet}=1/C_{ox}(V_{bg}-V_t)\mu$ fits to the data used to extract mobility.

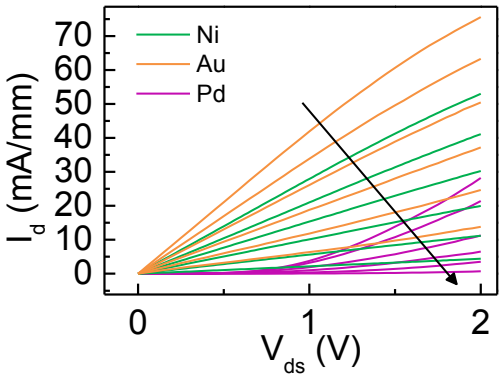

Figure 2: I_d-V_{ds} output characteristics for the three contact metals at V_{bg}=0V to 50V with 10V step. Arrow indicates decreasing V_{bg}. The channel length for all three devices is 500nm.

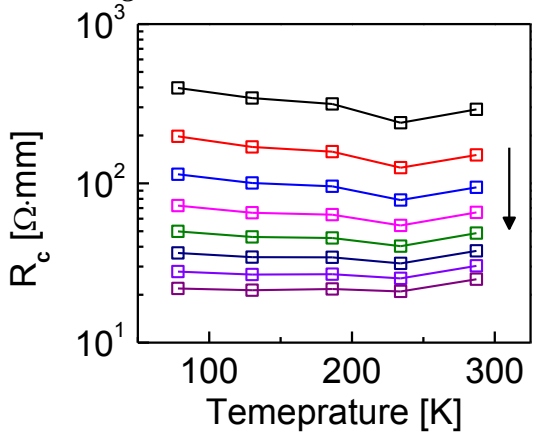

Figure 4: R_c extracted at V_{ds}=50mV as a function of temperature for V_{bg}-V_t from 14V to 56V with 6V step. The sample is different from the one measured in Figure 3. V_t is taken as the V_{bg} where I_d is 10nA. The arrow indicates increasing gate voltage.

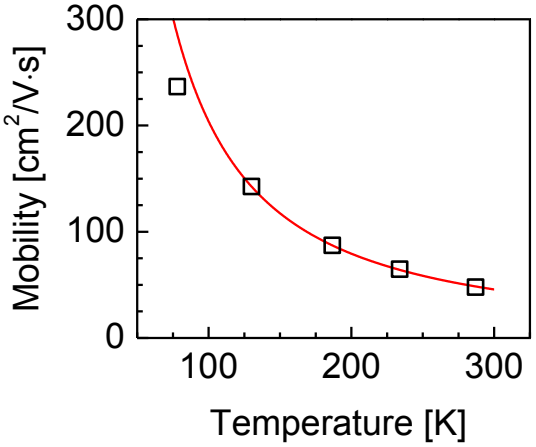

Figure 6: Mobility as a function of temperature extracted from the sheet resistance with power law fit $\mu \sim T^{\gamma}$, where γ=1.36, T=130K and above.

Balancing stress & dipolar interactions for fast, low power, reliable switching in multiferroic logic

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Nanomagnetic logic, though inherently energy efficient, has been historically limited by the energy overhead of the local write operations The ability to rotate magnetizations with strain rather than an applied field opens up the possibility of highly pipelined and fast, Bennett-clocked, low power logic with energy efficient writes. In multi-ferroic logic, information is passed along an array of nearest neighbor dipole coupled nanomagnets (NM). The NMs consist of magnetostrictive elements (e.g. Terfenol-D) storing the bits, piezoelectric elements (e.g. PZT) for stressing, and hard magnetic layers for the read and write references (Fig. 1a) [1]. The bistable configuration along the easy axis of the Terfenol-D layer encodes logic bits "0" and "1" ($\Theta = \pi/2$ or $3\pi/2$).

In this work, we will focus on efficient transmission to NM2 of information just written onto NM1 with torque from a current spin polarized by the hard layer (Fig. 1b, period A). In order to propagate the logic bit unidirectionally from NM1 to NM2 and switch the magnetization of the latter, a small local voltage (~10 mV) applied to the piezoelectric element stresses the magnetization of NM2 to switch to its hard axis (Fig. 1b, period B). Upon releasing the stress, the magnetization of the NM2 relaxes to the easy axis, with its final orientation determined by the dipolar coupling with the NM1 (NM3 still stressed and kept out of operation), thus achieving a fast and low power Bennett clocked computation (Fig. 1b, period C). In this work, we will assess the interplay between stress and dipolar coupling by varying the stressing profiles (Fig. 1c). Specifically we will explore the trade-off between energy dissipated, switching speed and reliability, through a thermodynamic study of the complex 3D spin dynamics of the NMs, captured within a stochastic Landau-Lifshitz-Gilbert formalism.

Achieving lower error rate with adiabatic stressing: The write error rate (WER) during switching depends on the interplay between stress applied and dipolar coupling between NMs. As dipole coupling is proportional to $1/d^3$, a smaller separation d between the NMs leads to lower error rates (Fig 2). While a high stress is needed to switch the magnetization from hard to easy axis during period B, it hinders the dipole from dictating the switching direction in period C, resulting in high error rates (Stressing profiles 1, 5 in Fig 2, 3 and 4). However, if the stress is tapered off at the end of period B, the dipole coupling can better dictate the direction of the magnetization switching, resulting in fewer errors (Stressing profiles 2, 3 and 6 in Fig 2, 3 and 4). At an applied stress of 10MPa, profile 3 has the lowest error rate, as the stress is tapered off over a period of 1ns, giving the dipolar coupling from NM1 enough time to switch NM2 in the right direction. Profile 5 has the highest error as the stress is suddenly switched from positive to negative, leading to a high dynamic error probability.

Faster switching with negative stress amplitude: In order to switch faster, a negative stress can be applied at period C for 1ns as shown in stress profiles 5 and 6, to switch the magnetization quickly from the hard to the easy axis. The magnetization switches 0.5ns faster than the other profiles (Table. 1).

Low power write: In stress profiles 1, 2, 3, and 4, the energy consumed while applying a voltage across the PZT is given by CV^2 where C is the capacitance of the PZT and V is the applied voltage. That consumed in profile 5 is given by $3CV^2$. In profile 6, a low-energy adiabatic stressing profile is used, where the energy consumption is 2 orders of magnitude lower than the other profiles. Energy consumed is given by $\pi V^2 C^2 R\omega$ where R is the resistance of the PZT and ω is the frequency of the sine wave [2].

In conclusion, the adiabatic stress profile, 6, is best suited for transmission of information through arrays of NMs in multi-ferroic logic because of its low energy, high speed and lower error rate. Such optimization information transfer at the 2 NMs level is critical to ensure efficient computation in interconnect and logic gate configurations.

This works has been supported by the NSF-NEB grant.

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[2]Mohammad S. Fashami *et al*, *Nanotechnology*, vol. 23 p. 105201 (2012)

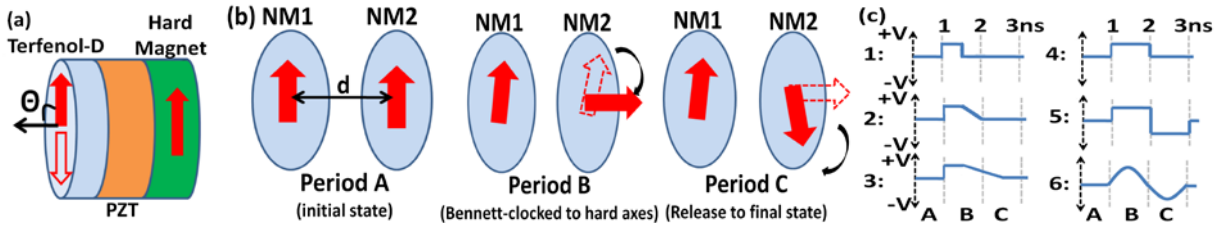

Fig. 1: (a) Multi-ferroic NM (Terfenol-D/PZT/Hard magnet). The bistable configuration along the easy axis of the Terfenol-D layer encodes bits "0" and "1" ($\Theta = \pi/2$ or $3\pi/2$). (b) 3-step information transmission process in 2 NMs. (c) Stress profiles varying from abrupt to tapered at the end of Period B.

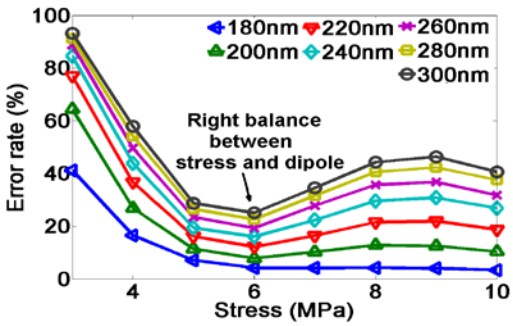

Fig. 2: Success rate for various separations and stress amplitudes for stress profile 1. Higher stresses undermine the dipole's role in switching accurately.

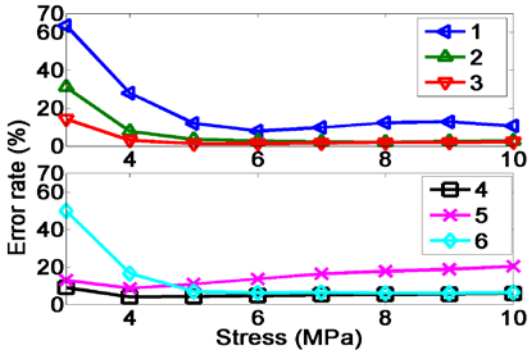

Fig. 3: Success rate for various stress amplitudes and profiles. Tapered profiles (2, 3 and 6) have lower error rates that abrupt (1, 4 and 6).

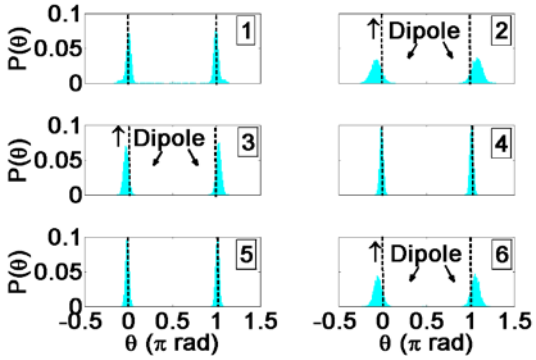

Fig. 4: Dipolar effect at the end of Period B (2ns) in NM2. The tapered stress in profiles 2, 3, and 6 enables the dipole to help switch accurately.

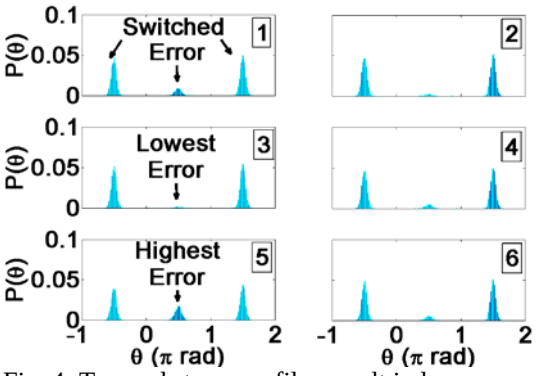

Fig. 4: Tapered stress profiles result in lower error rates. Profile 3 has the lowest numbers of error while 5 has the highest.

		4 MPa		10 MPa	
Stress Profile	**Mean delay (ns)**	**Error rate (%)**	**Energy (K_BT)**	**Error rate (%)**	**Energy (K_BT)**
1	**1.17**	**27.9**	**348**	**10.6**	**1038**
2	**1.5**	**7.7**	**348**	**2.7**	**1038**
3	**1.9**	**3**	**348**	**2.1**	**1038**
4	**1.7**	**4**	**348**	**5.9**	**1038**
5	**1.24**	**8.6**	**1044**	**20.4**	**3114**
6	**1.27**	**16.6**	**0.48**	**6.4**	**2.6**

Table. 1: Energy-delay-WER comparison for all six stressing profiles at 4 and 10MPa at 200nm separation. Profile 6 has the most optimal error rates with a small delay and acceptable write energy cost.

Double Slot High-k Waveguide Grating Couplers for Silicon Photonics

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Novel on-chip double slot high-k waveguide grating couplers have been successfully fabricated, and characterized. Silicon cannot yet be directly used for light generation and modulation in photonic devices because of its weak nonlinear optical effects. Slot waveguide is a solution to this problem, this structure consists of silicon and low refractive index material layers as the active material[1, 2]. Previously, grating couplers were demonstrated for horizontal single slot SiO_2 waveguides [3, 4]. Double slot waveguide is of great interest since the confinement of the optical power in the active material is significantly larger. Atomic layer deposited (ALD) high-k aluminum oxide (Al_2O_3) was used as the slot layer because of a superior layer quality and thickness uniformity. The ultimate goal of this work is the demonstration of the highly reproducible on-chip photonic devices.

The 3D schematics and the cross section of the device are illustrated in Fig.1 and 2, respectively. The device is fabricated on an amorphous-silicon-on-insulator wafer. The a-Si layers were deposited by LPCVD using disilane gas. In order to prevent the formation of microcrystal islands, the deposition temperature was 480 ˚C. The Al_2O_3 layers were deposited with ALD using trimethylaluminum (TMA) and DI water precursors at 250 ˚C. The gratings were monolithically manufactured with the waveguides while the patterned structures were fully etched to the buried oxide layer. The silicon layers were dry-etched using $HBr/Cl_2/He/O_2$ chemistry and the etching was stopped by an endpoint detection when the Al_2O_3 or SiO_2 layers had been reached. The Al_2O_3 layers were dry etched using a $BCl_3/Cl_2/N_2$ chemistry. The grating structure can be filled with SiO_2 cladding layers. Gratings with and without SiO_2 cladding were prepared. The gratings were filled with a 500 nm SiO_2 film deposited by PECVD. In Fig. 3 an SEM cross section image of the fabricated slot waveguide is shown.

In this work the measurements were conducted without the traditional index matching fluid [5], because of its incompatibility with electrical probing and slow alignment procedure. Optical fibers were 17˚ tilted and the fibers were aligned with a top viewing microscope. The attenuation in the waveguides was found by the transmission measurements in the waveguides with the different lengths. Fig. 4 (a) shows the original measured signal excluding the waveguide attenuation. The fluctuations observed in this spectrum can be filtered to two components. Fig. 4 (b) shows a fluctuation with the frequency of 0.66 (1/nm) that is obtained by a low pass filter. The resonance cavity size that corresponds to this fluctuation is 330μm long, whereas the measured waveguide was 1400μm long. In order to characterize the efficiency of the couplers a square shaped band reject filter with the center frequency of 0.66 (1/nm) and bandwidth of 0.1 (1/nm) is applied to the spectrum (the result is illustrated in Fig. 4 (c)).

The efficiency spectrum for the samples with and without the SiO_2 cladding is shown in Fig. 5 and 6, respectively. The samples without the cladding layer have an insertion loss of 6.6dB per coupler (a total transmission of -13.2 dB shown in the figure). The insertion loss for an SiO_2 cladded coupler was 6.5dB (-13 dB total transmission). The efficiency of the couplers has a 2.5 dB bandwidth of 48 nm in case of SiO_2 cladding and 60 nm for the air. Fig. 7 is a summary of the peak wavelengths measured for several grating periods in the case of air and SiO_2 cladding. For further investigations the coupler efficiency versus the top SiO_2 thickness is simulated. The simulation results show that the efficiency can be modulated with the top oxide thickness by the amplitude of 1.2 dB.

In conclusion, fully etched grating couplers are manufactured for double slot high-k waveguides. These couplers have a maximum efficiency of 22 %. This higher achieved efficiency despite the lack of a matching fluid compared to the case of single slots (18.5 % [4]) is due to the higher confinement of the optical power in the slot region for the double slot structures. Doubling the slot number reduces the effective refractive index from 2.7[3] to 2.2.

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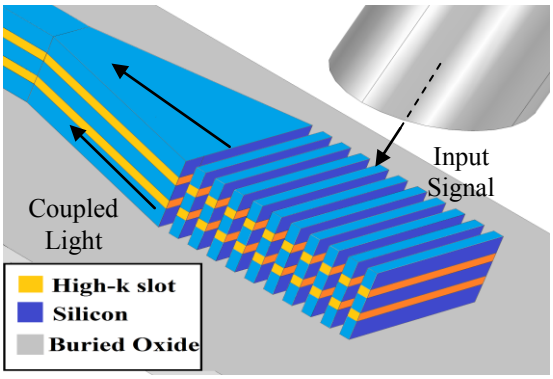

Figure 1. Showing the 3D schematic of the grating couplers (not to scale).

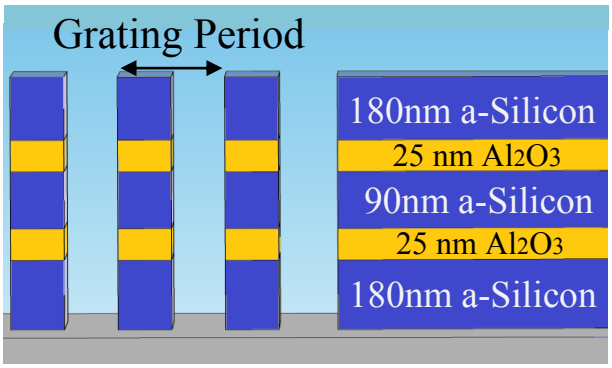

Figure 2. The side view schematics of the grating coupler including the details of materials stack and the thicknesses (not to scale).

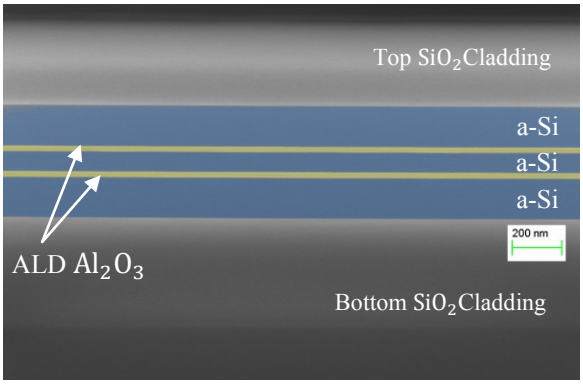

Figure 3.Partly colorized cross-section SEM image of the deposited layers for the double slot structures. Same color index as fig 1.

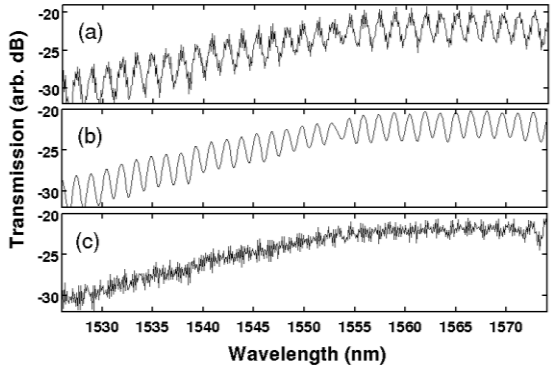

Figure 4. Demonstrating two Fourier filters. (a) shows the original transmission signal, (b) low pass filtered, (c) band reject filtered.

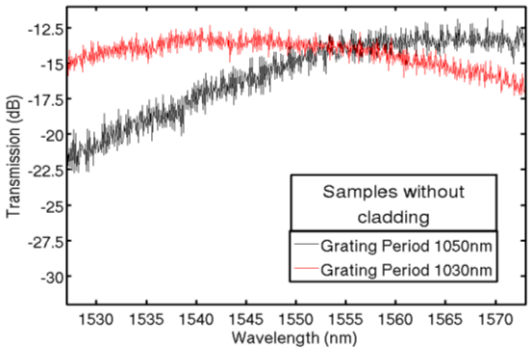

Figure 5. The transmission spectrum excluding the waveguide attenuation for samples with air cladding.

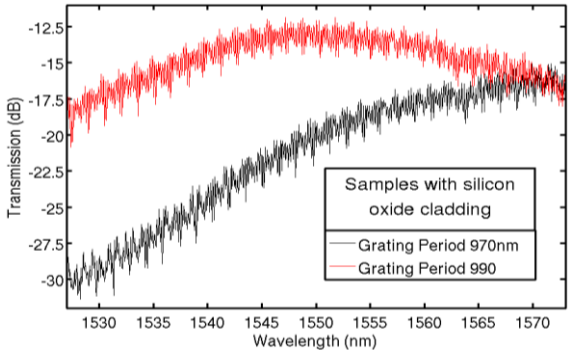

Figure 6. The transmission spectrum excluding the waveguide attenuation for samples with SiO_2 cladding.

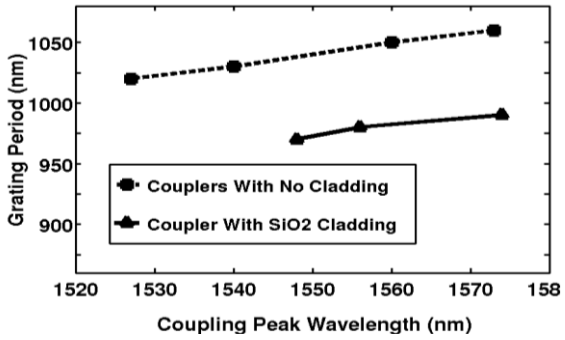

Figure 7. The Coupling peak values for different grating periods. Waveguides with top the SiO_2 cladding require smaller periods for an appropriate coupling.

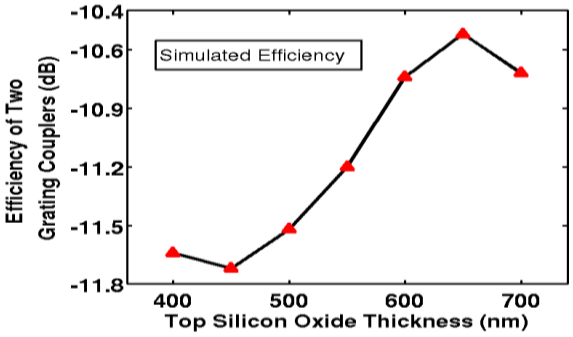

Figure 8.The effect of top cladding silicon oxide layer thickness. The simulations show a 1.2 dB modulation amplitude.

Self-aligned metal S/D GaSb p-MOSFETs using Ni-GaSb alloys

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GaSb has stirred a significant interest over the recent years, due to its high bulk electron/hole mobility and optoelectronic properties [1]. Particularly, the high hole mobility makes GaSb one of the III-V materials promising for p-MOSFETs and fully-integrated CMOS applications. However, the device technologies for GaSb MOSFETs have not been fully developed yet. In this work, we address a novel formation technology of source and drain (S/D) for GaSb p-MOSFETs. One of the problems of the S/D formation in GaSb (and generally III-V) is the low dopant solubility and the necessity of high temperature annealing for dopant activation. However, thermal stability of the GaSb/oxide interfaces is low and, therefore, a S/D formation process with low thermal budget is strongly required [2]. Also, for deeply-scaled MOSFET fabrication, self-aligned S/D formation is mandatory. For these reasons, we introduce a salicide-like self-aligned metal S/D process by using Ni into GaSb. In this study, we present the results of the characterization of Ni-GaSb alloys formed by direct reaction between Ni and GaSb, which are suitable for S/D in GaSb p-MOSFETs. Finally, we demonstrate, for the first time, a GaSb p-MOSFET with self-aligned Ni-GaSb alloy S/D, which allows us to fabricate MOSFETs at temperature as low as 250°C.

In order to find a suitable S/D metal (alloying with GaSb, having etching sensitivity relative GaSb, and having low contact resistance) and to evaluate Schottky barrier height (SBH) against GaSb, metal/GaSb diodes were fabricated using Al, Au, Ni and Ti with a Au capping layer, on both n-GaSb and p-GaSb substrates (both 1.5×10^{17}). The metals were deposited by EB (Ti, Au), thermal evaporation (Al) and sputtering (Ni). After Au deposition as the back contact, RTA (Rapid Thermal Annealing) was performed at 250°C-450°C for 1 minute. It was observed from the color change of the sample surfaces that Ni reacts with GaSb into alloys after RTA. Subsequent XRD analyses of a blanket Ni sputter on GaSb with increasing RTA temperature was performed to confirm the existence of the Ni-GaSb alloys, and the alloy formation temperature. The Ni thickness was 60 nm. Fig. 1 shows that 300°C or higher RTA provides a peak around 39°, which is attributable to a Ni-GaSb alloy crystalline phase. The peak intensity remains constant at RTA higher than 400°C, implying that most of the Ni film is alloyed at this temperature. Also, although no clear peak is visible at 250°C, we have confirmed the Ni-GaSb alloy formation at this temperature, judging from the successful MOSFET fabrication with 250°C RTA. Thus, no clear XRD peak at 250°C is ascribed to thin thickness of the Ni-GaSb alloy and/or an amorphous phase. We have also found that Ni can be selectively etched by HCl without etching the formed Ni-GaSb alloys, allowing us to employ the salicide-like self-aligned S/D formation process.

As shown in Figs. 2 and 3, the metal/p-GaSb diodes exhibited Ohmic behaviors, while the metal/n-GaSb samples exhibited Schottky behaviors, meaning that SBH for electrons is much higher than that for holes. The I-V characteristics for the Ni-GaSb alloys are almost the same as those for the other unalloyed metals. Figs. 4 and 5 show SBH for electrons and holes evaluated from the zero-bias I-V method, exhibiting the Fermi level pinned near the valence band. These results mean that SBH for holes is fairly low for all the metals [3] including the Ni-GaSb alloys, which is advantageous for S/D in p-MOSFETs.

In order to study the resistivity of the Ni-GaSb alloy, the sheet resistance (R_{sheet}) was determined by using a circular transmission line method (CTLM) pattern. After HCl pretreatment, Ni was sputtered on n-GaSb and RTA was performed at 250°C-500°C. Subsequently, the samples were dipped in HCl solution for 1 minute to remove remaining Ni. Finally, Al was evaporated. Fig. 6 shows R_{sheet} as a function of RTA temperature. R_{sheet} for Ni-GaSb is shown to be as low as ~12Ω, close to that of the as-deposited Ni film. On the other hand, R_{sheet} increases after 350°C RTA, suggesting changes in the Ni-GaSb structures.

A GaSb p-MOSFET using the Ni-GaSb alloy as S/D was successfully fabricated, for the first time, as shown in Fig. 7, a top-view SEM image. The process flow is shown in Fig. 8. An n-GaSb substrate was pretreated with HCl (36%) to remove the native oxide. A 10 nm Al_2O_3 gate oxide was deposited at 150°C and Ta was used as the gate metal. A 30 nm Ni film was sputtered, followed by RTA at 250°C for 5 minutes. Figs. 9 and 10 show the I_D-V_D and I_D-V_G characteristics of the GaSb p-MOSFETs with gate length of 1 and 0.7 μm, respectively. The I_D-V_D characteristics show the clear transistor behavior even without S/D p-n junctions, due to the good junction characteristics of the Ni-GaSb/GaSb contacts. The on-current is not too high, which may be caused by the low mobility of 3 cm^2/Vs due to the un-optimized poor MOS interface in the present devices. Fig. 11 shows the total resistance between the source and the drain. As a result, the S/D resistance is estimated to be 300 kΩμm, which is still high probably due to insufficiently high SBH for holes and/or un-optimized gate formation under-lapped with S/D.

In summary, we have characterized the Ni-GaSb alloys, formed by the direct reaction between Ni and GaSb, suitable for S/D in GaSb p-MOSFETs in the self-aligned metal S/D process. A metal S/D GaSb p-MOSFET using this alloy has been demonstrated, for the first time, by employing the low-temperature self-aligned process.

[Acknowledgment] This work was supported by NEDO.

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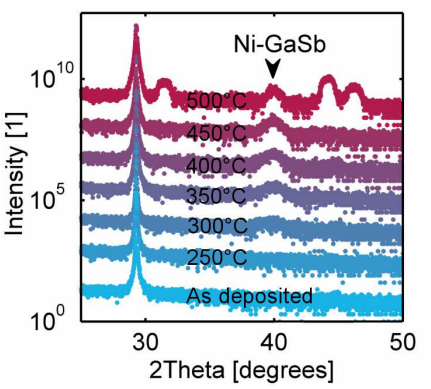

Fig. 1. XRD of Ni on GaSb for different RTA temperatures at 1 minute.

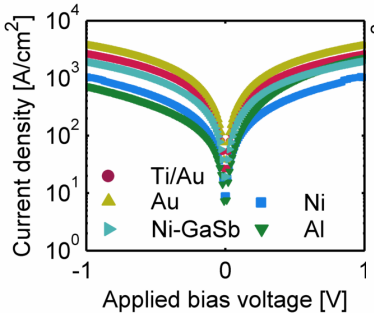

Fig. 2. I-V characteristics of metal/p-GaSb diodes, showing Ohmic behaviour.

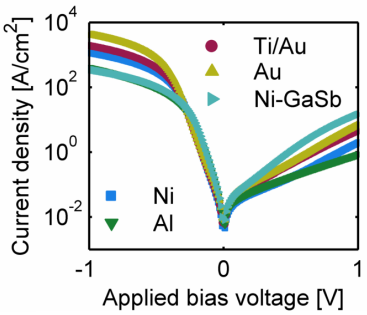

Fig. 3. I-V characteristics of metal/n-GaSb diodes, showing large Schottky barrier height (SBH).

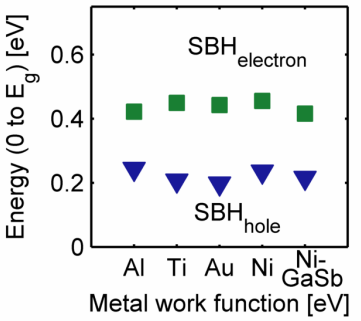

Fig. 4. SBH for different metals and the Ni-GaSb alloy, by the zero-voltage I-V method.

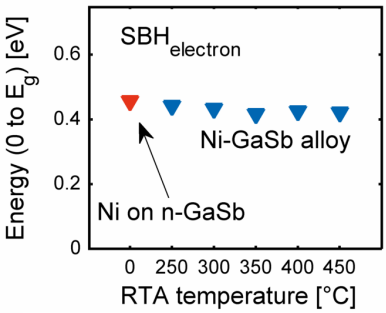

Fig. 5. SBH to GaSb as a function of RTA temperature.

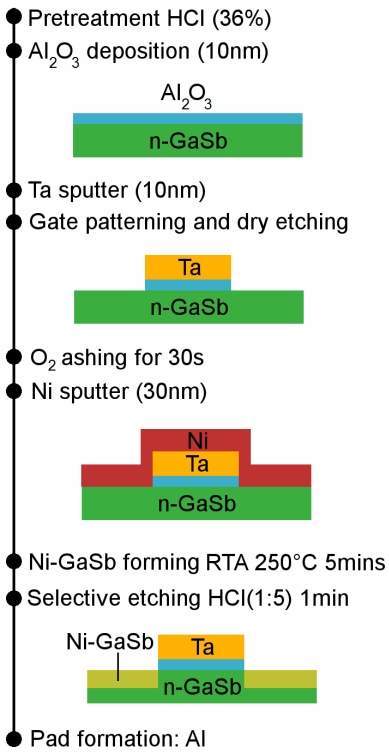

Fig. 8. Process flow for a Ni-GaSb S/D GaSb pMOSFET

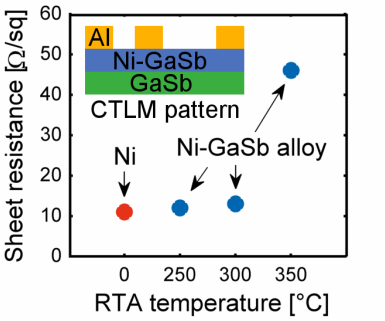

Fig. 6. Sheet resistance as a function of RTA temperature.

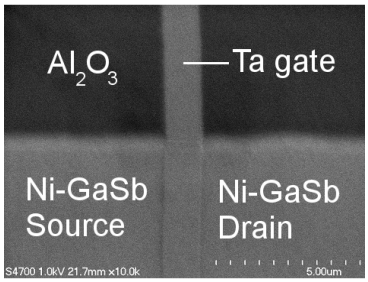

Fig. 7. SEM image of a Ni-GaSb S/D GaSb pMOSFET.

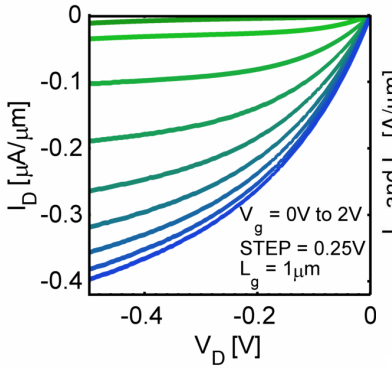

Fig. 9. I_D -V_D characteristics of a Ni-GaSb S/D GaSb pMOSFET.

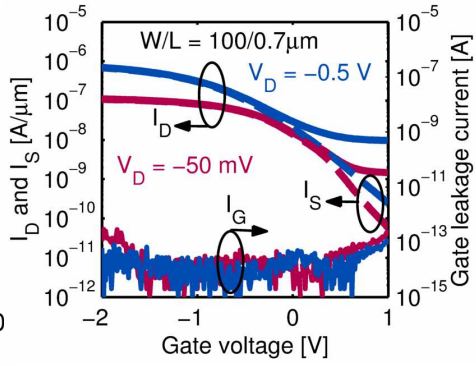

Fig. 10. I_D, I_S, and gate leakage at V_D = -0.5 V and -50 mV.

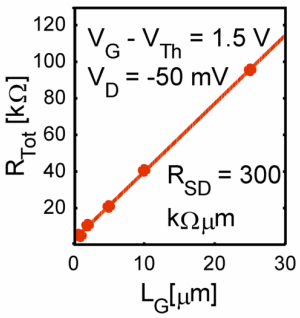

Fig. 11. Total resistance as function of gate length.

Bilayer Graphene Vertical Tunneling Field Effect Transistor

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Electronic devices have been explored in the past based on resonant single-electron CB (conduction band) to CB tunneling between parallel quasi-two dimensional (2D) quantum wells within III-V heterostructures and their accompanying negative differential resistance (NDR) [1]. Such devices are attractive for high speed electronics, and digital logic circuits also have been demonstrated using a combination of conventional and such NDR FETs [2]. For two graphene layers separated by a tunnel barrier, we recently proposed the ultra-low-voltage Bilayer pseudoSpin FET (BiSFET) which would employ enhanced *non*resonant VB (valence band) to CB tunneling, with a nevertheless very sharp NDR characteristic based on a predicted room-temperature many-body superfluid state [3]. However, NDR due to resonant single-particle CB-to-CB or VB-to-VB tunneling may also be achievable in such a structure. Furthermore, the atomically near-perfect 2D nature of the component graphene layers and the conduction/valence band symmetry may offer advantages over III-Vs. Here, we model the *I-V* characteristics due to single-particle tunneling in such a structure, Fig. 1, using a perturbative tunneling Hamiltonian approach [4,5], and deviations from this simple theory using atomistic tight-binding nonequilibrium Green's function (NEGF) simulation.

For the perturbative analysis, the ***k***-space Hamiltonian of the coupled system is given by Eq. (2) (see next page) where the first line represents the *intra*layer contribution. The summation over crystal momentum ***k*** is around the Dirac points. The summation over *s* is for the CB (*c*) and VB (*v*). The CB and VB energies ε are given by, respectively, $\varepsilon_{1/2,c/v,k} = \pm\hbar v\mathbf{k} - q\varphi_{1/2}$, where 1/2 indicates the layer, and $\varphi_{1/2}$ is the layer potential. The second line in Eq. (2) represents real-space AB *inter*layer coupling of strength *t*. The corresponding ***k***-space interlayer coupling is $t_k = te^{(-i\theta_{1k}-i\theta_{2k})/2}$, where θ_{1k} and θ_{2k} are the directions of the ***k*** in Layers 1 and 2 with respect to corresponding Dirac points. Assuming perfectly aligned layers, $t_k = te^{-i\theta_k}$. The tunneling current between the graphene layers for an applied bias $\mu_1 - \mu_2 = qV$ is given by Eq. (3) allowing for valley and spin degeneracy. $\mu_{1/2}$ is the Fermi level in layers 1 and 2, $f(E)$ is the Fermi distribution function and $T(E)$ is the transmission between the layers given by Eq. (4), where $A_{1/2}$ are the spectral density of state functions for layers 1 and 2. These spectral functions are assumed to be of the Lorentzian form of Eq. (5), where the Γ represents transition broadening due to, e.g., scattering. Fig. 2(a) shows the interlayer tunneling current as a function of interlayer bias for three different gate voltages. The dependence of interlayer potential on interlayer voltage bias, obtained by solving Eq. (1), is shown in Fig. 2(b). The graphene layers are in resonance and the interlayer current peaks in Fig. 2 when the interlayer potential difference is zero. The magnitude of the current also is—roughly allowing for the thermal smearing of the Fermi surfaces at 300K—proportional to the number of states in the annular area shown in Fig. 1(d) between the Fermi surfaces defined by the voltage difference between layers.

The above approach, however, is only appropriate for large area devices with tunneling-limited transport. Fig. 3 shows non-self-consistent NEGF based ballistic transmission at a single injection energy, as function of interlayer potential difference, for AB coupling between 5.4 nm wide metallic graphene nanoribbons—used not of necessity but to isolate essential physics—with a 104.3 nm long overlap/channel region. Fig. 3(a) illustrates short-channel effects that broaden the resonance; Fig. 3(b) additionally illustrates injection-limited transport as the transmission probability saturates toward unity. The reference solid lines in Fig. 3 are a fit to the expected form of Heisenberg Uncertainty associated with the finite channel lengths, but are not adjusted for injection-limited transport. There is, however, no additional broadening in 3(b) due to increased interlayer coupling; the lifetime remains quite long in the tails of the distribution so that, self-consistently, the resonance is not additionally broadened in this manner.

This was supported by the SRC NRI SWAN program, and by Intel.

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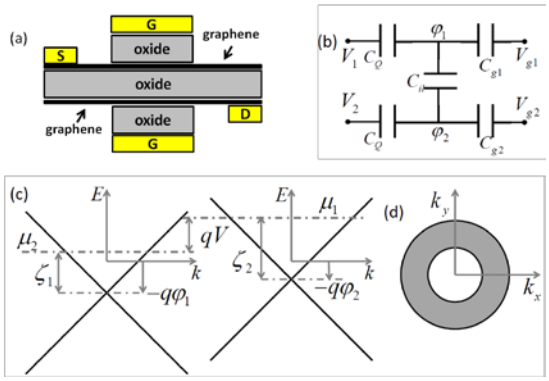

Figure 1 (a) Schematic of the double layer graphene Tunnel FET, (b) Equivalent capacitance circuit of the FET, (c) Band structure of layers 1 and 2 a showing the Fermi level, potential of each layer slightly out of resonance at an applier interlayer voltage bias V and (d) Fermi surface of layers 1 and 2 at resonance. The current is due to all states in the gray annular area

$$\begin{pmatrix} Q_1(\zeta_1) \\ Q_2(\zeta_2) \end{pmatrix} = -\begin{pmatrix} C_{g1} & 0 \\ 0 & C_{g2} \end{pmatrix} \begin{pmatrix} V_{g1} - V_{FB1} - \frac{\zeta_1}{e} - V_1 \\ V_{g2} - V_{FB2} - \frac{\zeta_2}{e} - V_2 \end{pmatrix} + \begin{pmatrix} C_{il} & -C_{il} \\ -C_{il} & C_{il} \end{pmatrix} \begin{pmatrix} \frac{\zeta_1}{e} + V_1 \\ \frac{\zeta_2}{e} + V_2 \end{pmatrix} \quad (1)$$

$$H = \sum_{ks} \varepsilon_{1sk} a^{\dagger}_{1sk} a_{1sk} + \sum_{ks} \varepsilon_{2sk} a^{\dagger}_{2sk} a_{2sk} + \frac{1}{2} \sum_{k} t_k \left(a^{\dagger}_{1ck} - b^{\dagger}_{1vk} \right) \left(a_{2ck} + b_{2vk} \right) + h.c \quad (2)$$

$$I = -\frac{q}{\hbar} \int_{-\infty}^{\infty} T(E) \left[f(E - \mu_1) - f(E - \mu_2) \right] \frac{dE}{2\pi} \quad (3)$$

$$T(E) = \sum_{k;ss'} |t_k|^2 A_{1s}(k, E) A_{2s'}(k, E) \quad (4)$$

$$A_s(\boldsymbol{k}, E) = \frac{2\Gamma}{(E - \varepsilon_{sk})^2 + \Gamma^2} \quad (5)$$

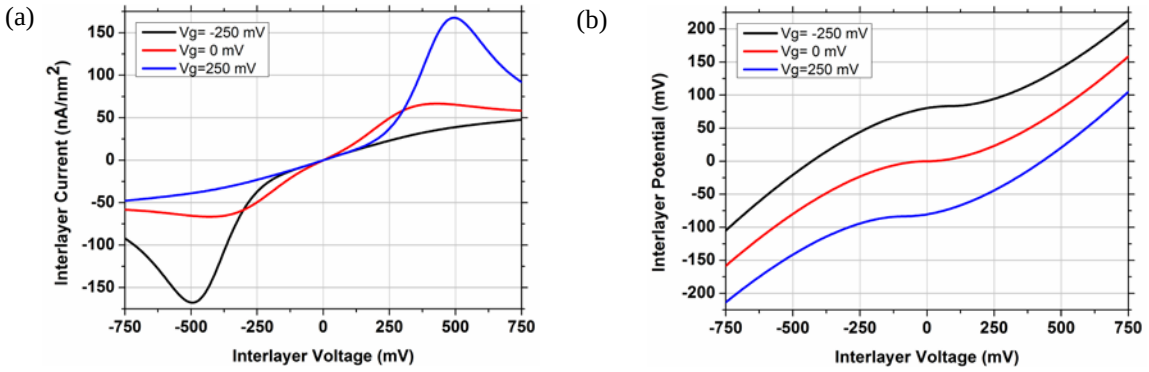

Figure 2 (a) Interlayer tunneling current as a function of interlayer voltage illustrating the negative differential resistance and (b) Interlayer potential as function of interlayer voltage for three different gate voltages split equally with opposite polarity between the gates. The data is obtained using *t*=25 meV and Γ = 10 meV and effective oxide thickness (EOT) of 0.8 nm for the gate and interlayer dielectrics. The graphene layers are assumed to be undoped.

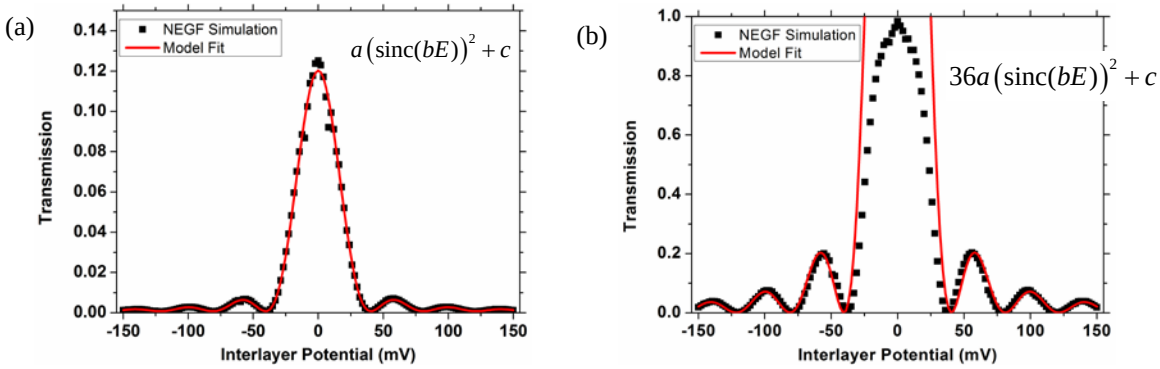

Figure 3 NEGF based transmission as function of interlayer potential at an injection energy of 200 meV for a AB coupled graphene nanoribbons of width 5.4 nm and an overlap region length of 104.3 nm with (a) a weak inter layer coupling t =10 meV and (b) a strong interlayer coupling t =60 meV. The fit to data of (a) is obtained using the function shown in the inset and the fit to (b) is obtained by scaling the prior fit by 36 times as the transmission scales as t^2.

440 V AlSiN-Passivated AlGaN/GaN High Electron Mobility Transistor with 40 GHz Bandwidth

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AlSiN is showing promise as a passivation material for AlGaN/GaN high electron mobility transistors (HEMTs) [1]. The negative fixed charged provided by the dielectric allows for controlled depletion of the ungated portions of the channel, which suggests that this passivation scheme would allow for higher operating voltages without the use of a field plate. Here we report the performance of AlSiN-passivated AlGaN/GaN HEMTs without field plates and small feature sizes for power switching applications.

The epitaxial structure of the devices consisted of an Al nucleation layer, followed by a 0.5 µm GaN buffer, a 220 Å AlGaN barrier with 24.5 % Al fraction, and a 20 Å GaN cap grown on semi-insulating SiC. Device mesas were isolated with a $Cl_2/BCl_3/Ar$ reactive ion etch (RIE). Next, 35nm of AlSiN was deposited by low pressure chemical vapor deposition (LPCVD) at 750 °C using Trimethylaluminum, Dichlorosilane, and Ammonia precursors. The ohmic source/drain contact windows were defined by electron beam lithography and etched using a CF_4 RIE, and the V/Ti/Al/Mo/Au metal stack was deposited in an electron beam evaporator. A thin film (20 nm) of SiN was deposited by plasma enhanced chemical vapor deposition (PECVD) to encapsulate the ohmic contacts during annealing. The Schottky gate was also defined by e-beam and etched with an $SF_6/BCl_3/Ar$ RIE, and Ni/Au contacts were evaporated. See Figure 1 for device cross-section.

The fabricated devices were dual-gated and had 1.5, 1, or 0.5 µm gate lengths, 400 (2 x 200) µm peripheries, and gate-drain spacings of 3 or 5 µm. These features sizes are significant because most high breakdown voltage HEMTs have gate drain spacings in excess of 10 µm [2]. DC, small-signal, and large-signal RF measurements were performed. The pinch-off voltage was -5.5 V, and the quiescent point for small and large signal biasing was chosen at the point of maximum transconductance. Figure 2 shows the combined DC measurements of the parameter space of a typical device, including the output curves, constant power measurements, and high voltage off-state breakdown measurement. At V_{ds} = 10 V and V_{gs} = 2 V, the drain current was approximately 1 A/mm. Constant power measurements were taken up to 200 V. The highest f_T of 18 GHz and f_{MAX} of 40 GHz was obtained on a 0.5 µm gate length device with a 5 µm gate-drain spacing.

For the purposes of the DC high voltage testing, we defined the device off-state breakdown as reaching 1 mA of drain current. The devices were submerged in Diala AX insulating oil to prevent premature air breakdown. With the gate biased at -7 V, breakdown was observed at 440 V for a 0.5 µm gate length device and 470 V for a 1 µm gate length device, both of which had a source-gate spacing of 1 µm and a gate-drain spacing of 5 µm (Figure 3). To our knowledge, this is the highest recorded off-state breakdown voltage for an AlGaN/GaN HEMT device with a relatively small gate-drain spacing and no field plate, exceeding 320 V for a device with similar feature sizes with Al_2O_3 passivation [3] and 238 V with SiN passivation [4]. In fact, with our LPCVD SiN passivation, the 0.5 µm gate length devices typically experience static breakdown at approximately 100 V.

Large signal measurements were performed at 10 GHz on a load pull bench. The input was matched for reflection and the output was loaded for maximum efficiency. A typical device power sweep is shown in Figure 4, which at V_{ds} = 30 V had 12.2 dB of linear gain, 4.9 W/mm of output power, and 41 % peak power-added efficiency, which is in line with our previous measurements on 400 µm gate width devices of 0.25 µm gate length.

In conclusion, we present an AlGaN/GaN HEMT which exhibits a high off-state breakdown voltage with small features and without a field plate, while maintaining high bandwidth. High voltage load line mapping of these devices at 2 GHz is in progress.

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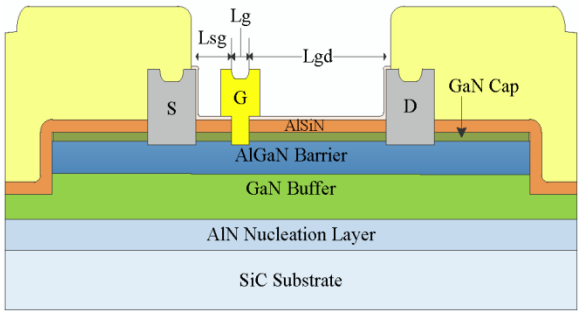

Figure 1. Schematic cross section of the device structure.

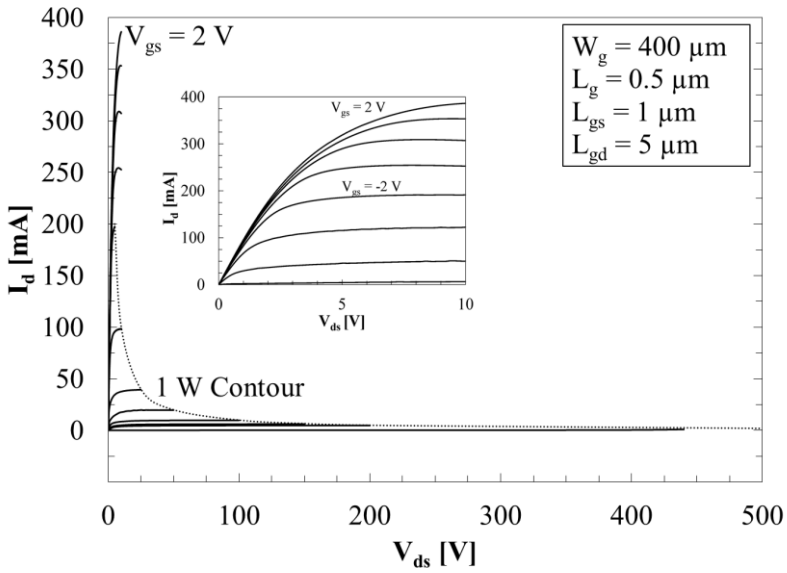

Figure 2. Combined DC parameter space measurements. Inset shows the detailed output curves for this device up to 10 V on the drain.

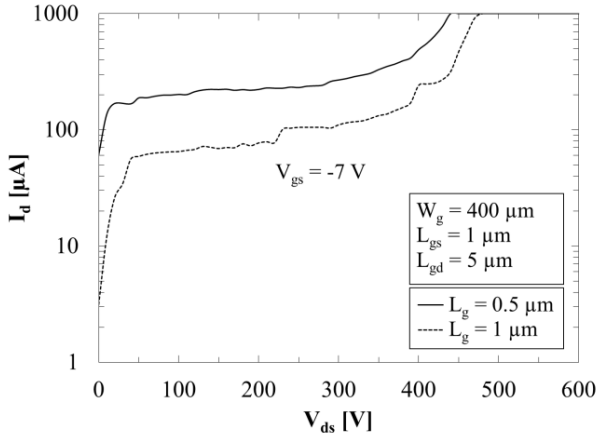

Figure 3. High voltage off-state breakdown characteristics of devices with 0.5 µm (solid) and 1 µm (dashed) gate lengths.

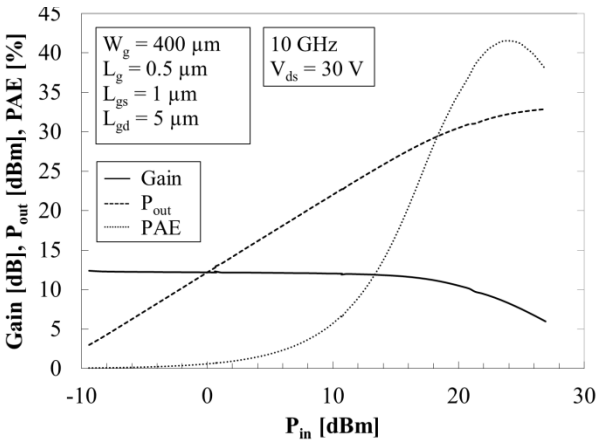

Figure 4. Typical 10 GHz load pull power sweep at 30 V of drain bias.

Analysis of terahertz zero bias detectors by using a triple-barrier resonant tunneling diode integrated with a self-complementary bow-tie antenna

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Recently, heavy emitter doping rather than decreasing the barrier thickness has boosted the peak current density of resonant tunneling diodes (RTDs) above 1,000 kA/cm². Based on this achievement very mature InP-based RTD with current densities above 500 kA/cm² are nowadays the leading solid-state THz device [1, 2]. Here, we show that even triple-barrier RTD (TBRTD) devices now reach a current density in excess of 250 kA/cm² making this element ideally suited for rectification [3] but now at THz frequencies. Figure 1 is the state of art of THz detection sensitivity of previously reported zero bias detectors. Focusing on such zero bias broadband THz detection, we have also been studying on a design policy for a μm-sized on-chip self-complementally antenna and especially we have reported basic performances of a bow-tie antenna[4,5] integrated with a conventional homogeneous semiconductor mesa structure. However, it was still limited studies considering neither of actual nonlinear devices and peripheral circuits.

This paper presents THz detection sensitivity analyzed by considering both measurement-based performance of a InP-based TBRTD and electromagnetic simulation-based equivalent circuit of the μm-sized on-chip self-complementally bow-tie antenna, for the first time, towards feasibilities of ultra wideband low power signal detections.

Figure 2 shows the model of the TBRTD rectifying antenna (rectenna). The layer structure and conduction band diagram of the TBRTD are schematically illustrated in Fig.3 and Fig.4, respectively. The TBRTD exhibits strong asymmetric *I-V* characteristic as shown in Fig.5 at zero bias unlike double-barrier RTD since the TBRTD can be designed having two quantum wells with different width. The large peak current density is achieved by reducing the third barrier height and reducing barrier thickness. The TBRTD structure inherently has an advantage of exhibiting large speed index such as 0.19 V/ps, which is defined as peak current to capacitance ratio. The solid line in Fig.5 denotes a expression on the basis of a physics -based theory.[6]

Figure 6 shows calculated frequency dependency of detection sensitivity which is defined by time average of the output voltage to the input power ratio ($<V_{out}/P_{in}>$) in terms of the input power (Fig.6(a)) and the load resistance (Fig.6(b)), respectively. Calculations are performed on the basis of nonlinear large signal analysis by using harmonic balance method. These calculated examples come from nonlinearly of the particular TBRTD, nevertheless it suggests that the proposed TBRTD zero bias rectenna has feasibility of fairly high sensitivity for low input power in THz range beyond 300 GHz. The maximum available input power is 210 μW which is limited by the peak voltage of the TBRTD to be free from the negative differential resistance region. It should be mentioned that plots in Fig.6 indicate so-called unmatched sensitivity. If ideal matched impedance is employed against the THz input by optimizing antenna structures precisely, each plot is found to be shifted up with 8 dB. Further studies should be on layer and structural optimization for improving the sensitivity.

In summary, a nonlinear large signal analysis is performed for a triple-barrier resonant tunneling diodes integrated with a self-complementally bow-tie antenna and peripheral circuit components for the first time toward investigation of feasibilities of broadband THz zero bias detectors.

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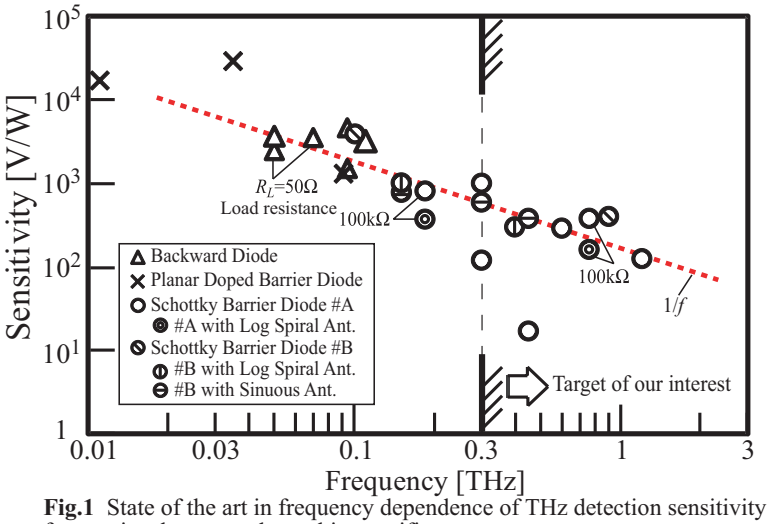

Fig.1 State of the art in frequency dependence of THz detection sensitivity for previously reported zero bias rectifiers.

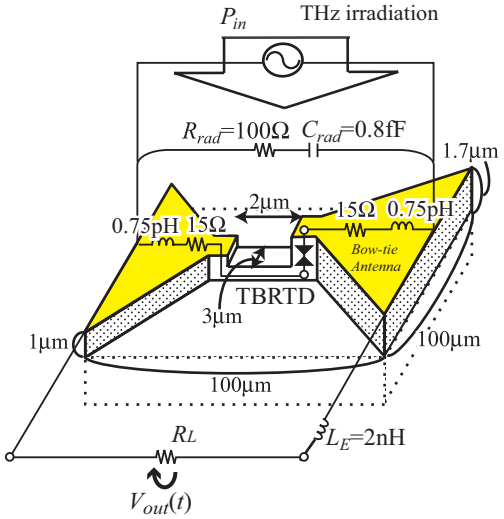

Fig.2 A TBRTD THz detectors integrated with a thin film bow-tie antenna. An equivalent circuit is superimposed with a load resistance R_L and an external inductance L_E .

Layer	Thickness [nm]	Doping concentration [cm^{-3}]
InP	Substrate	Semi-isolated
InGaAs	300	3.74×10^{19}
InGaAs	50	1.0×10^{18}
InGaAs	10	1.0×10^{18}
InGaAs	1.75	Not intentionally doped
InAlAs	1.7	
InGaAs	1.17	
InAs	2.42	
InGaAs	1.17	
AlAs	1.7	
InGaAs	1.17	
InAs	1.21	
InGaAs	1.17	
AlAs	1.7	
InGaAs	1.17	
InGaAs	50	3.74×10^{19}
InGaAs	100	3.74×10^{19}
$In_{0.7}Ga_{0.3}As$	8	3.74×10^{19}

Fig.3 Layer structure of the TBRTD

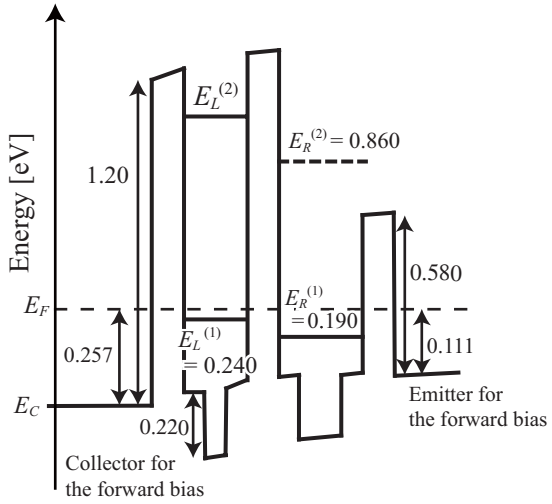

Fig.4 Conduction band diagram of the TBRTD at equilibrium.

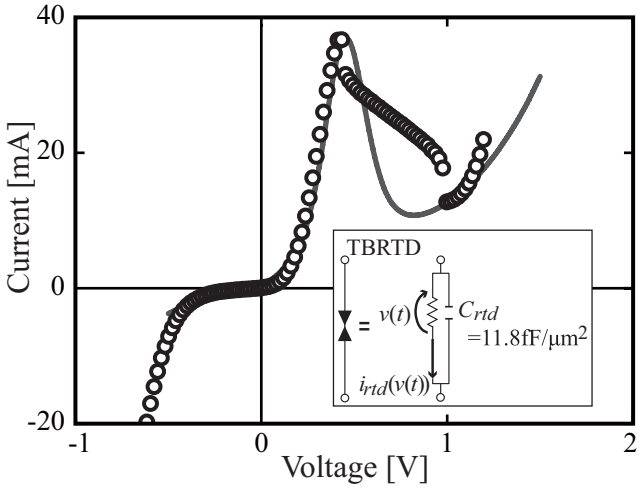

Fig.5 A measured typical asymmetric I-V characterisitcs (a open circle line) of the TBRTD and its physics-based expression (a solid line) used for sensitivity calculations. The area of the TBRTD is 9μm^2.

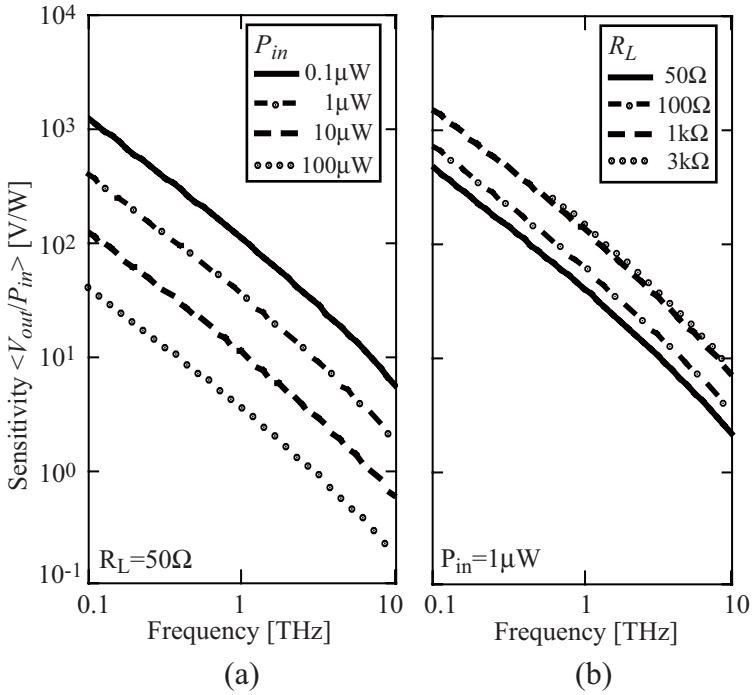

Fig.6 Frequency dependence of detection sensitivity in the TBRTD rectenna for (a) different input power, (b) different load resistance.

An InAs Nanowire Spin Transistor with Subthreshold Slope of 20mV/dec

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We have fabricated a spin transistor based on InAs nanowire. The transistor operates based on Datta-Das type spin transistor mode [1][2][3]. The spin polarized electrons are injected from the ferromagnetic electrodes and synchronized spin precession is controlled by the gate voltage through spin-orbit interaction. We have clearly observed drain current oscillation versus gate voltage as expected from the Dyakonov-Pérel mechanism. By controlling the spin precession, on/off switching is expected to be achieved with the steep slope. The best of our obtained results has shown the steepest slope of 18mV/dec to 23mV/dec near the off-state ((2n+1)π-spin rotation) where vertical electric field meats the condition of persistent spin helix (PSH) motion [3]. The present result provide alternative method of steep slope device mechanism in addition to the conventional ideas such as Tunnel FETs or impact ionization FETs.

InAs nanowires have been grown by VLS methods with Au colloids as catalyst. Nanowires have been grown by MOCVD [4] and MBE[5][6]. The nanowires were dispersed onto the SiO_2/Si substrate and EB lithography was used to define source/drain and gate electrodes. As ferromagnetic electrodes, Fe/Au were employed (Fig.1-2) for source and drain spin injector and detector in spin transistor structures and Ni was employed in magnetic resistance (MR) characterization device (Fig.5). Both Ni and Fe are known to have spin polarization of ≈40%. Spin injection into InAs nanowires has not been reported extensively, but we have obtained preliminary results indicating spin injection (Fig.4). The InAs nanowire transistor showed decent DC characteristics even with non-alloyed source/drain ohmic contact for spin injection. Ids-Vds characteristics (Fig.2) reveal impact ionization in the drain voltage region greater than 0.7V. The Ids-Vgs characteristics (Fig.3) show weak oscillatory behavior even before the magnetization of ferromagnetic electrodes by external magnetic field. The field-effect mobility was estimated to be 2,000cm^2/Vs based on the transconductance results.

When the ferromagnetic electrode was magnetized along the channel direction, the oscillatory behavior suddenly became much pronounced as shown in Fig.5. The single shot measurements reveal clear oscillatory behavior as expected from the enhanced spin-orbit interaction in InAs. We have conducted Monte Carlo simulation assuming 40% spin polarization taking account of degree of spin polarization in Fe electrode. The reason why the off-state current still remains substantial is the limited spin polarization of elementary ferromagnetic electrodes. Minimum current at the off-state is caused by the minimum spin relaxation by the PSH condition. Successful half metal electrodes would eventually realize off-state in the future. Nevertheless, substantial agreement between the experiment and the Monte Carlo simulation results gives strong support to the successful realization of Datta-Das type spin transistor and advantage of employing 1-dimensional InAs spin transistor structures for persistent spin conduction [7]. The relatively long gate length of 2.8μm was designed to assure enough spin precession in order to obtain enough spin current amplitude. In Fig. 6, drain current oscillation is plotted in logarithmic scale against gate voltage. Steep subthreshold slope of 18mV/dec and 23mV/dec near the off-state are seen to be realized. To our knowledge, these are the steepest subthreshould slope reported to date, and the first in Datta-Das type spin transistor. These results strongly indicate the usefulness of InAs nanowire to spin tarnsistors and intruduce an alternative candidate of steep slope devices in the future.

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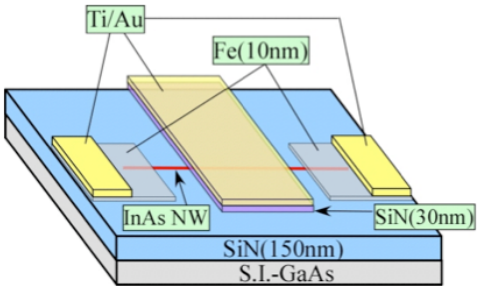

Fig.1(a) Schematic diagram of a spin

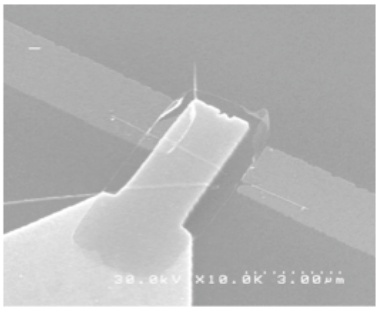

Fig.1(b) SEM photo-micrograph of an InAs spin transistor

$$\mu = \frac{g_m L_g^{\ 2}}{V_d C_g} \approx 2000[cm^2/Vs]$$

$$\varepsilon_r = 7 \qquad d = 40[nm]$$

$$t = 30[nm]$$

$$L_g = 2.3[\mu m]$$

$$g_m = 13.7[\mu S]$$

$$V_d = 0.6[V]$$

$$C_g = \frac{\varepsilon S}{t} = 5.7 \times 10^{-16}[F]$$

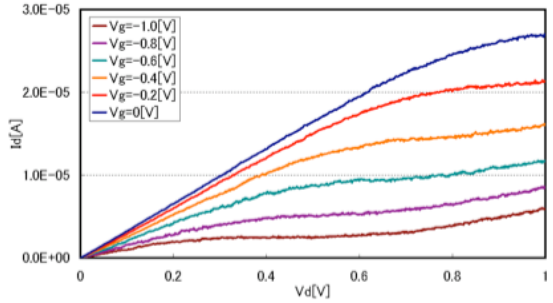

Fig.2 Ids-Vds characteristics of an InAs nanowire spin transistor

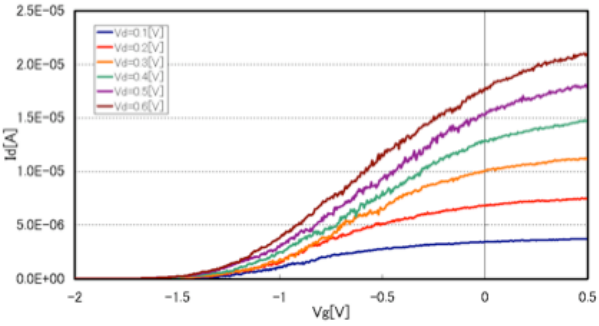

Fig.3 Ids-Vgs characteristics of an InAs nanowire spin transistor

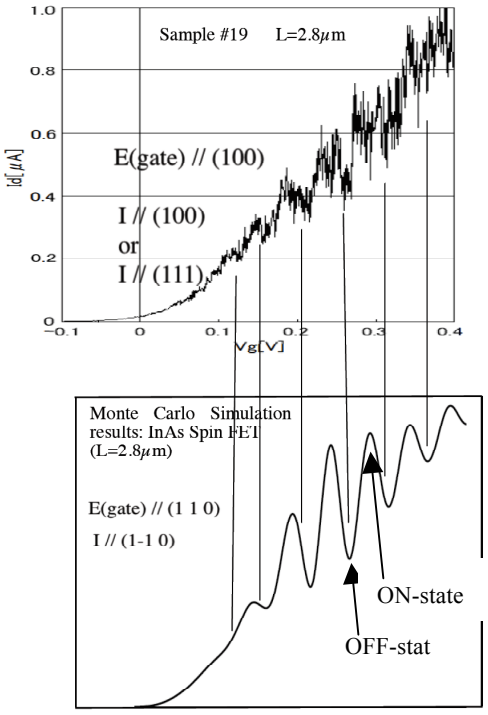

Fig.5 After magnetization of spin injection electrode, Ids-Vgs characteristics was measured. Single shot measurements revealed clear current oscillations. Bottom curve is a Monte Carlo simulation result of spin current oscillations in InAs channel by spin-orbit interactions. Clear agreement with measurement is seen.

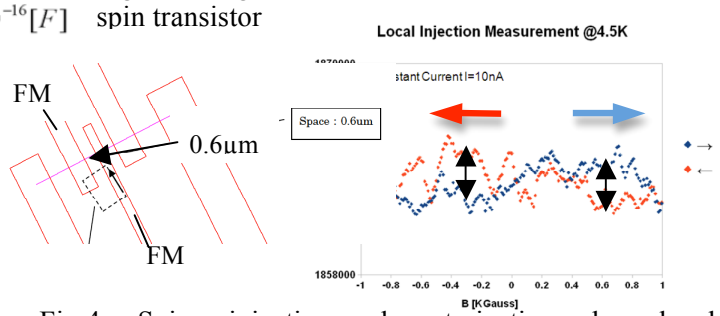

Fig.4 Spin injection characterization by local measurements. Ferromagnetic electrode (Ni) is grown on InAs nanowire. Measured MR ratio was $\Delta R/R \approx 0.1\%$.

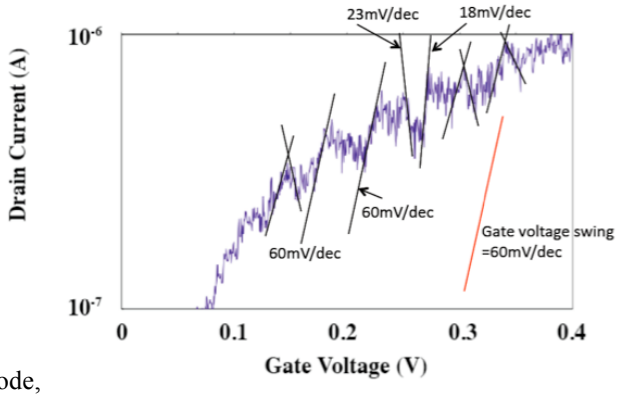

Fig.6 Drain current is plotted in log scale as a function of gate voltage. Gate voltage range near the current minimum at Vg=-0.27 is where the maximum dpin relaxation is expected due to maching of the Dresselhaus and Rashba effect (PSH). Here we observe steep slope of 18 – 23 mV/dec which exceed Bolzmann limit by a factor of 3 at room temperature.

Understanding dual-gate polymer field-effect transistors

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Since the first report that the use of regioregular conjugated polymer semiconductors results in significantly improved device performance in field-effect transistors (FETs), research into polymer FETs such as novel material development, fabrication processes optimization and device architectures employment has been focused [1-2]. One of such attempts is dual-gate configuration based polymer FETs. In a dual-gate device, the semiconductor active layer is sandwiched between two separate dielectrics and carrier concentration or the channel conductivity can be effectively controlled through the voltages applied independently to the top and bottom gate electrodes. Dual-gate devices have been investigated to obtain improved performance such as higher on-current, increased on-off current ratio and decreased threshold voltage [3-4].

In order to understand device physics on improved dual-gate FETs, there have been reports on explanation such as gate screening effects and shift of V_{th} caused by back-gate bias. However, few of the previous approaches have focused on interaction between charge carriers and semiconductor-dielectric interface when dual-gate mode operation. Furthermore, most of the experiments to investigate device physics of dual-gate configuration have been based on steady-state or direct-current measurements. There have been no studies reported that focus on non-quasistatic (NQS) transport measurements for charge carrier velocity distributions to understand dual-gate polymer FETs.

Diketopyrrolopyrrole (DPP) copolymer is a high field-effect mobility polymer semiconductor which can be formed by solution-processable deposition [5]. It is a novel polymer donor-acceptor semiconductor comprised of DPP acceptor and donor blocks. FETs formed from such donor-acceptor systems possess better device characteristics due to good π-orbital overlap [5]. Recently, we fabricated dual-gate FETs with active semiconductor layers consisting of diketopyrrolopyrrole-naphthalene copolymer (PDPP-TNT). Compared to bottom- and top-gate devices, dual-gate mode operation results in the lowest V_{th} and improvement in sub-threshold slope and on-off current ratio. In addition, we measured the entire velocity distribution of charge carriers at each mode operation in dual-gate polymer FETs for the first time.

Device performance and device physics of dual-gate polymer FETs will be discussed by using both steady-state and NQS transport measurements. Temperature-dependent measurements at each mode operation will be compared as well. Velocity distributions of charge carriers obtained by transient measurements can provide additional information useful for understanding charge carrier transport and device physics influenced by device configurations compared to direct-current and temperature-dependent measurements alone.

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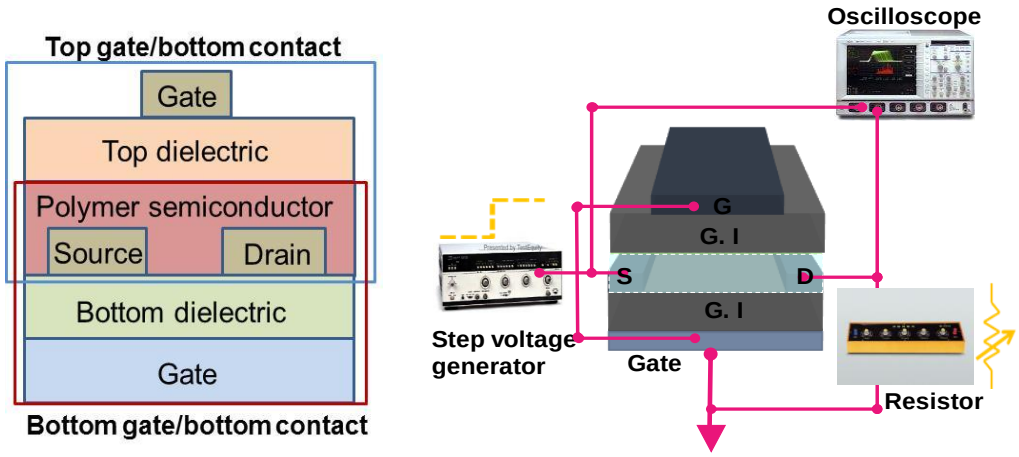

FIG. 1 a) the schematic cross-section of a dual-gate polymer FET possessing a PDPP-TNT semiconductor active layer and b) an illustration of NQS transport measurement circuit using step voltage method

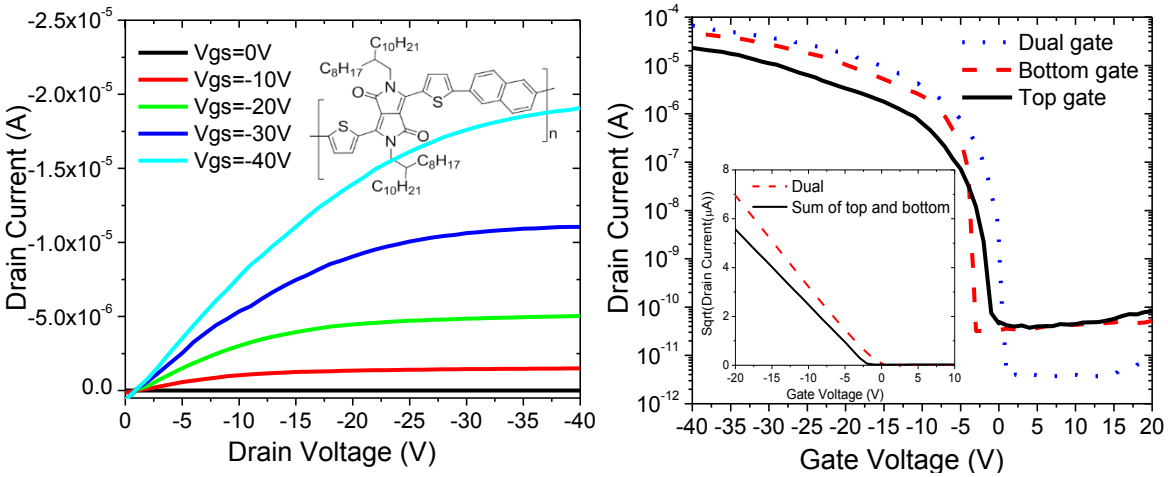

FIG. 2 a) the output characteristics of top-gate PDPP-TNT FET employing organic gate dielectric: The inset shows the chemical structure of PDPP-TNT and b) the transfer characteristics in the top-, bottom- and dual-gate mode operations of a dual-gate PDPP-TNT FET: The inset shows that the current density from a dual-gate device is larger than the sum of current densities of both top- and the bottom-gate devices

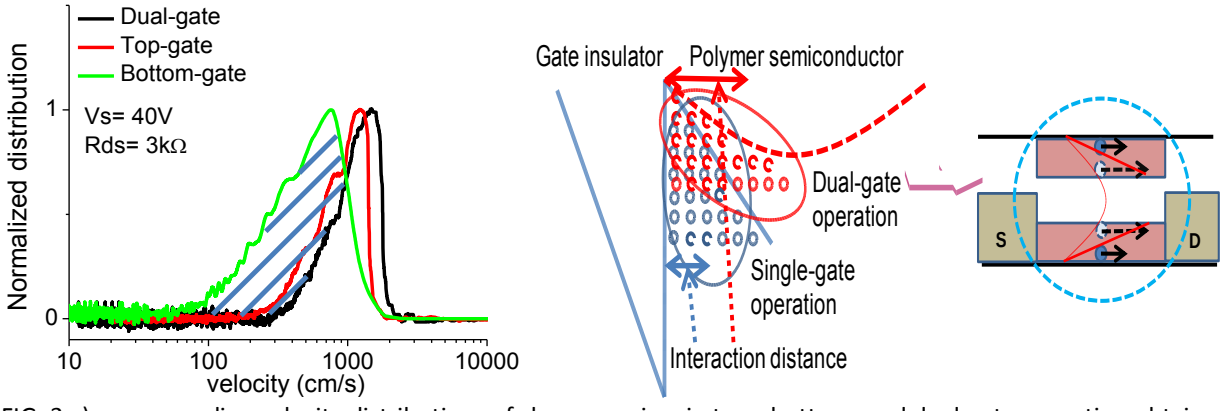

FIG. 3 a) corresponding velocity distributions of charge carriers in top-, bottom- and dual-gate operation obtained by NQS transport measurements and b) the schematic illustration of interfacial energy band diagram of single-gate device vs. dual-gate device

Fundamental Limitations of Conventional-FET Biosensors: Quantum-Mechanical-Tunneling to the Rescue

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Electrical detection of biomolecules using Field-Effect-Transistors (FETs) [1-5] is very attractive, since it is label-free, inexpensive, allows scalability and on-chip integration of both sensor and measurement systems. Nanostructured FETs, especially nanowires have gained special importance due to their high electrostatic control and large surface-to-volume ratio. In order to configure the FET as a biosensor (**Fig. 1(a)**), the dielectric/oxide layer on the semiconductor is functionalized with specific receptors. These receptors capture the desired target biomolecules (a process called conjugation), which due to their charge produce *gating effect* on the semiconductor, thus changing its electrical properties such as current, conductance etc. Thus it is intuitive, that greater the response of the FET to the gating effect, higher will be its sensitivity where sensitivity can be defined as the ratio of change in current due to biomolecule conjugation to the initial current (before conjugation). While the highest response to gating effect can be obtained in the subthreshold region, the conventional FETs (CFET) suffer severely due to the theoretical limitation on the minimum achievable *Subthreshold Swing (SS)* of [$K_BT/q\ ln(10)$] due to the *Boltzmann tyranny* (**Fig. 1(b)**) effect where K_B is the Boltzmann constant and T is the temperature. This also poses fundamental limitations on the sensitivity and response time of CFET based biosensors [6]. In recent times, Tunnel-FETs have attracted a lot of attention for low power digital applications [7]-[17], due to their ability to overcome the fundamental limitation in *SS* (60 mV/decade) of CFETs. Recently, it has been shown that the superior subthreshold behavior of TFETs can be leveraged to achieve highly efficient biosensors [6]. This is possible, thanks to the fundamentally different current injection mechanism in TFETs in the form of band-to-band tunneling [17]. The working principle of TFET biosensors is illustrated in **Fig. 1c**.

It is to be noted that, while the requirement for high ON current in TFETs for digital design still remains a nightmare for engineers, this is not a major concern for its application as a biosensor. For biosensing, what is of utmost importance is the Subthreshold Swing and *SS* of 30 mV/decade averaged over a decade of drain current has already been demonstrated experimentally using Si nanowires [14-15]. In **Fig. 2(a)**, the sensitivity is plotted as a function of the surface potential (ϕ_{bio}) on the dielectric developed due to conjugation of biomolecules, for different values of *SS*. The surface potential (ϕ_{bio}) is computed by solving the kinetics of biomolecules within the electrolyte through diffusion-capture model and the electrostatic screening by the ions in the electrolyte is taken into account by solving the nonlinear Poisson–Boltzmann equation [5]. The electrical response of the biosensor due to the change in the surface potential is determined through numerical simulations based on Non-Equilibrium Green's function formalism. It is observed that lowering the *SS* can lead to substantial increase in the sensitivity since the change in current due to biomolecule conjugation is much higher in case of lower *SS* for the same initial current value (inset figure). **Fig. 2(a)** also illustrates the fundamental limitation in sensitivity of CFET biosensors as highlighted by the shaded region. In **Fig. 2(b),** the sensitivity of CFET and TFET biosensor is plotted as a function of biomolecule concentration clearly showing the advantage of TFET based biosensors.

Apart from sensitivity, another critical parameter for gauging the performance of the biosensors is the response time. Response time is defined as the time required to obtain a desired sensitivity (more specifically the time needed to capture a certain surface density of biomolecules (N_{bio}) in order to achieve a desired change in electrical signal). It is observed that response time is reduced significantly due to decrease in *SS* (**Fig. 3**). This effect can be understood in the following way. Lower *SS* implies that for obtaining the same change in current and hence same sensiivity, the required change in surface potential (ϕ_{bio}) is lower. Now, the response time (t_r) is directly proportional to N_{bio} [18], which is again directly proportional to ϕ_{bio}. Thus, decrease in ϕ_{bio} leads to decrease in N_{bio} and consequently to reduction in the response time. The fundamental limitation on the response time of CFET biosensor is highlighted in **Fig. 3(b)** while it is clear that TFET biosesors can overcome such limitation and lead to significant reduction in response time.

Fig. 4 illustrates the effect of bandgap of the semiconductor on the sensitivity of TFET biosensors. It is observed that there is a optimal value of bandgap, which leads to a peak in sensitivity. Lowering of bandgap leads to improvement in tunneling current but at the same time degrades the *SS* due to channel-drain tunneling. Increasing the bandgap reduces the channel-drain tunneling but the *SS* at measurable current level degrades as explained in **Fig. 4**. Asymmetric design techniques such as employment of heterostructures and lower drain doping concentration can lead to improvement in the sensitivity of TFET biosensors. In **Fig. 5,** sensitivity is plotted as a function of ϕ_{bio} for different diameters of the nanowire. It is observed that decrease in the diameter can lead to increase in sensitivity due to improved electrostatic control. However, very small diameter can lead to increase in variability. **Fig. 6** shows that decrease in the effective dielectric thickness can improve the sensitivity of the biosensors. **Fig. 7** shows the effect of source doping concentration on the sensitivity of TFET biosensor. Very low doping concentration degrades the *SS* and hence sensitivity, since the sharpness of band-bending at the source-channel junction reduces. On the other hand, very high doping concentration hinders effective Fermi-tail cutting since the Fermi-level goes much below the valence band of the source, thus increasing the *SS* and lowering the sensitivity. `

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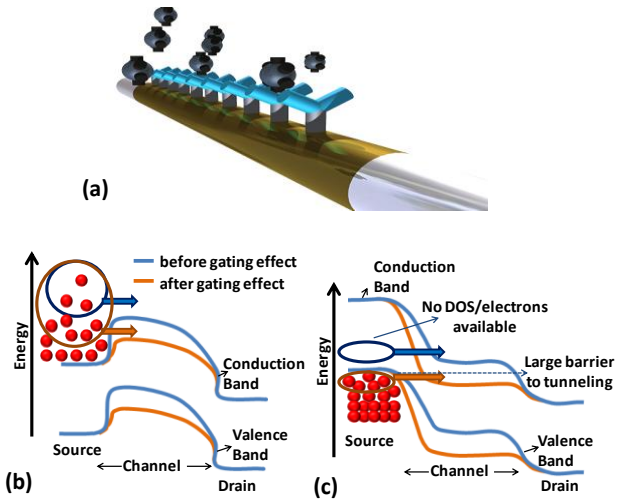

Fig. 1. a) Schematic of a nanowire Field-Effect-Transistor (FET) based biosensor. For a TFET biosensor, the source and drain are to be doped to form a P-I-N structure (with P+ source, N+ drain, and intrinsic channel, for an n-type device). For the operation as a biosensor, the nanowire is covered with a thin dielectric/oxide layer, which is functionalized with specific receptors for capturing the target biomolecules. The charged biomolecules being captured, induce gating effect, modulating the current flow. **b)** Schematic diagram showing origin of the *Boltzmann tyranny effect* in conventional FETs. **c)** Before biomolecule conjugation, the barrier for band-to-band tunneling (BTBT) between the valence band of source and conduction band of channel is large and hence source-channel tunneling current is negligible. After the capture of biomolecules, due to the gating effect, the bands bend down and the barrier for source-channel tunneling reduces, increasing the BTBT current between source and channel. In case of TFETs, the tail of the Fermi distribution is cut-off by the forbidden gap of the semiconductor.

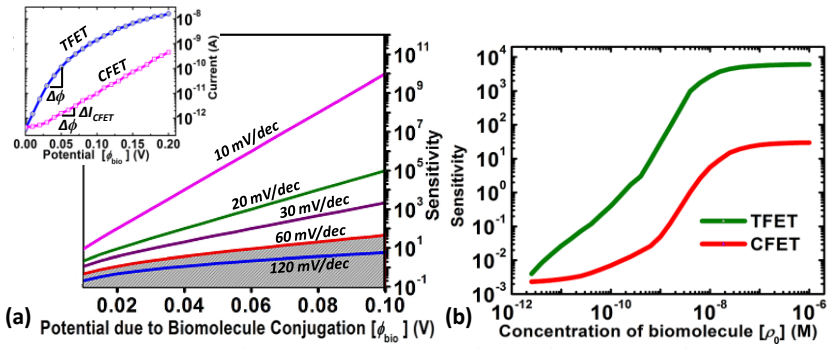

Fig. 2. a) The sensitivity of biosensor as a function of the surface potential (ϕ_{bio}) on the dielectric developed due to conjugation of biomolecules, for different values of subthreshold swing (*SS*). The inset figure shows the current as a function of ϕ_{bio} for both CFET and TFET biosensor. For the same change in surface potential ($\Delta\phi$), the increase in current in TFET is much higher due to its lower subthreshold swing. The sensitivity is found to increase substantially with decrease in *SS*. The red curve that corresponds to the *SS* of 60 mV/decade marks the maximum sensitivity achievable with CFET biosensors as a function of ϕ_{bio}. **b)** Sensitivity of both CFET and TFET biosensor as a function of the biomolecule concentration. The bandgap and the effective masses used in the simulations are 0.4 eV and $0.15m_0$ respectively (where m_0 denotes the mass of a free electron).

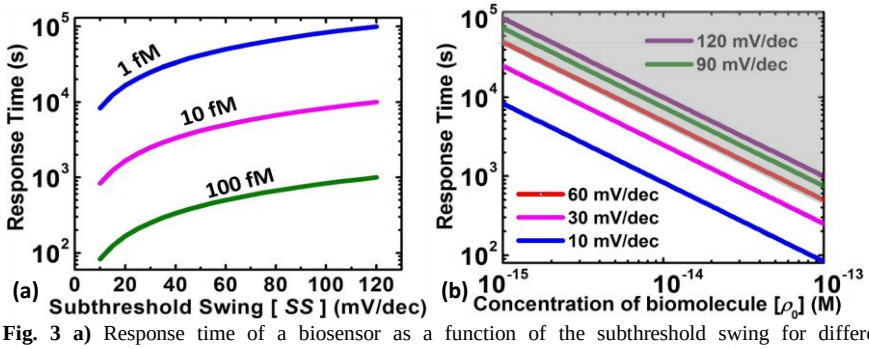

Fig. 3 a) Response time of a biosensor as a function of the subthreshold swing for different concentration of biomolecules. Decrease in subthreshold swing leads to significant decrease in response time. Hence, for detection at same biomolecule concentration, TFETs can be advantageous in reducing the response time and for achieving the same response time and sensitivity, TFETs allows detection at lower biomolecule concentration. **b)** Response time as a function of biomolecule concentration. The red curve that corresponds to *SS* of 60 mV/decade marks the minimum response time achievable with CFET biosensors.

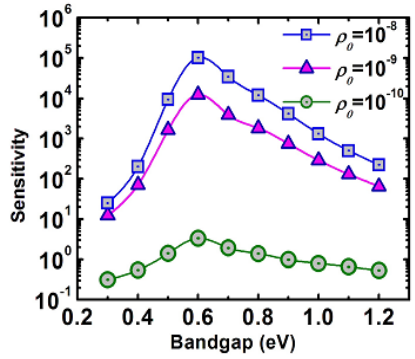

Fig. 4. Sensitivity as a function of bandgap for different values of biomolecule concentrations (unit: M). Sensitivity first increases with increasing bandgap but then decreases again when bandgap increases further. At very low bandgap, the leakage due to channel-drain tunneling degrades the subthreshold swing resulting in lower sensitivity. With the increase in bandgap, channel-drain tunneling reduces but the source-channel tunneling reduces at the same time, which negatively affects the subthreshold swing. Moreover, when the bandgap is very large, the lower values of subthreshold swing often occur at current levels, which are below the measurable limits [15]. This increases the experimentally observable *SS*. All these effects lead to decrease in sensitivity at very low or very high values of bandgap.

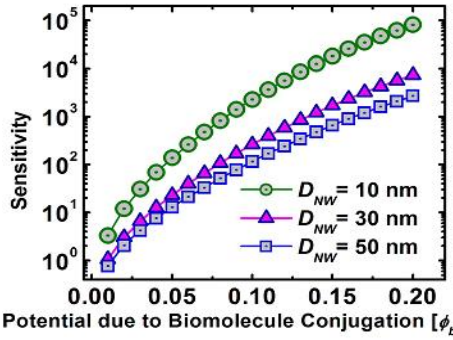

Fig. 5. Sensitivity as a function of the surface potential (ϕ_{bio}) on the dielectric developed due to conjugation of biomolecules, for different diameters of nanowire. Smaller diameter leads to better electrostatic control and hence, increase in the sensitivity.

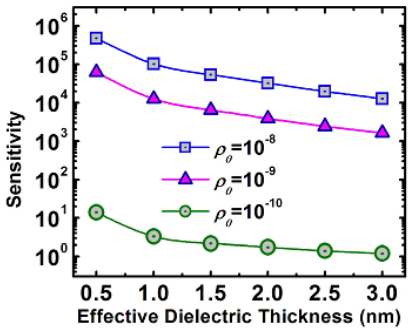

Fig. 6. Sensitivity as a function of the effective dielectric thickness for different values of biomolecule concentration (unit: M). Sensitivity increases with decrease in the dielectric thickness due to more efficient gating effect produced by the biomolecules.

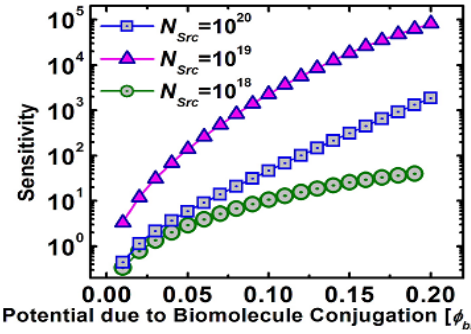

Fig. 7. Sensitivity as a function of the surface potential (ϕ_{bio}) on the dielectric developed due to conjugation of biomolecules, for different doping concentrations in the source (N_{Src}). Increase in the doping concentration from 10^{18} cm^{-3} to 10^{19} cm^{-3}, increases the sensitivity due to the increase in the electric field at source-channel junction. However, further increase in N_{Src} to 10^{20} cm^{-3} decreases the sensitivity due to ineffective Fermi-tail cutting.

Can Quasi-Saturation in the Output Characteristics of Short-Channel Graphene Field-Effect Transistors be Engineered?

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Introduction: The interest in graphene for high-frequency analog and RF applications, where transistor turn-off is not critical, has gained significant traction in recent years [1] - [2]. However, small output resistance continues to be an important limitation. While long-channel graphene FETs (GFETs) have shown quasi-saturation, which has been attributed to velocity saturation [1], saturation has not been observed in short-channel GFETs [2]. On the other hand, Ref. [3] shows that GFETs in the ballistic regime too can exhibit quasi-saturation. In this paper, we propose a novel way to increase the extent of quasi-saturation in the output characteristics of ballistic short-channel GFETs by engineering the gate-drain underlap region. Using self-consistent quantum transport simulations, we explore the factors affecting quasi-saturation and show that a *p*-type doped (~0.2%) drain underlap can significantly enhance output resistance (13x) and intrinsic gain (4x) in GFETs with 20 nm gate-length.

Approach: A schematic of the simulated short-channel GFET is shown in Fig. 1(a). Device dimensions and other parameters used are listed therein. A p_z-orbital basis atomistic Hamiltonian is used. The contact self-energies are calculated using the prescription in Ref. [4]. Periodic boundary condition is used along the width and transverse momentum modes are summed numerically. We perform ballistic quantum transport simulations within the non-equilibrium Green's function (NEGF) formalism. NEGF equations are solved iteratively together with Poisson's equation until a self-consistency between charge and electrostatic potential is achieved.

Results and Discussion: A qualitative understanding of output characteristics can be gained from Fig. 1(b). For small biases, current is predominantly thermionic w.r.t. channel-drain junction (i.e., through upper Dirac cones). But for large drain voltages, there exists an additional current due to tunneling (between lower channel and upper drain cones). Quasi-saturation, the end of which is marked by inflection point in $I_{DS} - V_{DS}$ characteristics, occurs for intermediate voltages, until tunneling becomes appreciable. The simulated output characteristics for different gate voltages, shown in Fig. 2(a), exhibit modest quasi-saturation. Corresponding plots of energy-resolved current $I(E)$ (= $T(E)$x$(f_1(E) - f_2(E))$ with T, f_1 and f_2 being respectively the transmission co-efficient and Fermi-Dirac distributions corresponding to source and drain electrochemical potentials) at V_{DS} = 1.2 V show tunneling and thermionic components. As expected, for a given V_{DS}, larger V_{GS} results in smaller tunneling current. Output characteristics in Fig. 3(a) show that a larger EOT reduces both thermionic and tunneling currents due to thicker tunneling barriers at source-channel and drain-channel junctions, as shown in the potential energy profiles in Fig. 3(b). However, due to smaller band bending, the ratio of tunneling to thermionic current increases, resulting in degraded quasi-saturation behavior. Figure 4 shows the effect of varying the length of gate-drain underlap region. A larger potential barrier results in the underlap with increasing length, as shown in Fig. 4(b). Hence the thermionic component is reduced for small to intermediate drain biases. Moreover, as drain potential is fixed for a given V_{DS}, for large drain voltages, larger barrier increases the electric field near the drain, increasing tunneling and consequently deteriorating the quasi-saturation significantly. This brings us to the central result of our paper. While doping graphene remains an area of active research, both *n*-type (using nitrogen [5]) and *p*-type (gold [6]) doping techniques have been recently demonstrated. In light of this, we examine the effect of varying concentrations of uniform *n*- and *p*-type doping in drain underlap region in Figs. 5 and 6 respectively. As seen in Fig. 5(a), larger *n*-type doping leads to better quasi-saturation. An *n*-type doping decreases the tunneling component by introducing a barrier for tunneling, as seen from logarithmic local density-of-states (LDOS) plotted in Fig. 5(b) for doping concentration N of $1\text{x}10^{13}$ cm^{-2}. It also enhances the thermionic part by increasing the band bending, resulting in improved quasi-saturation. With *p*-type doping, the barrier present in case of Fig. 4(b) in enhanced further, thus suppressing the thermionic part, as shown in the LDOS plot in Fig. 6(b). Larger doping increases the drain bias up to which current is predominantly thermionic, hence preventing the onset of tunneling. To put things into perspective, we compare the output resistance r_0 (= max$(\partial I_{DS}/\partial V_{DS})$) and intrinsic gain $g_m r_0$, (where $g_m = \partial I_{DS}/\partial V_{GS}$ at V_{DS} corresponding to r_0) in Fig. 7. With $1\text{x}10^{13}$ cm^{-2} of *n*-type doping, the increase in r_0 and $g_m r_0$ are marginal compared to the nominal device. A similar *p*-type doping results in a 13x increase in r_0; however, underlap barrier reduces g_m – making the intrinsic gain increase only by 4x.

Conclusions: To summarize, we propose that quasi-saturation in short-channel GFET output characteristics can be effectively engineered by doping in the drain-underlap region and show using self-consistent NEGF simulations that a ~0.2% *p*-type doping can enhance output resistance by 13x and intrinsic gain by 4x in 20 nm gate-length GFETs.

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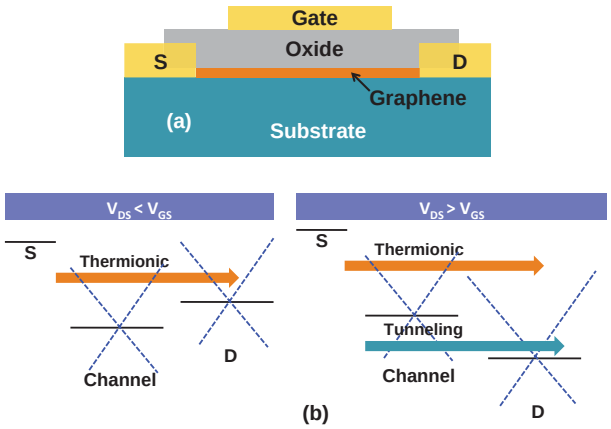

Fig. 1. (a) Schematic cross-section of the simulated short-channel GFET. Gate length and source-side underlap are respectively 20 and 2 nm. While EOT and length of drain-underlap region are varied, the respective values for nominal device are 0.5 and 2 nm. Source and drain contacts are ohmic (zero Schottky barrier height). Substrate interactions are ignored. (b) Qualitative explanation of output characteristics. The black horizontal lines denote the electrostatic potential (equivalently, the Dirac point) in various regions. Graphene Dirac cones in the channel and drain regions are also shown. For $V_{GS} < V_{DS}$, only thermionic (upper cone to upper cone) current flows. For $V_{GS} > V_{DS}$, there is an additional current due to tunneling between lower channel-cone and upper drain-cone. Quasi-saturation is observed for intermediate voltages until the tunneling current becomes appreciably large.

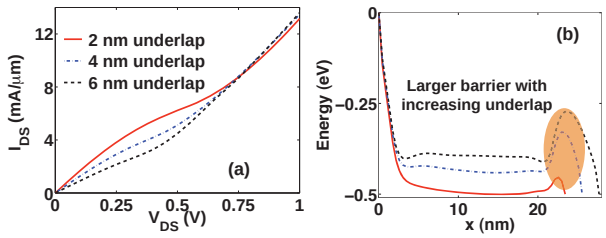

Fig. 4. (a) Output characteristics showing the effect of varying lengths of gate-drain underlap region at V_{GS} = 0.8 V. (b) Corresponding plots of electrostatic potential (also the Dirac point) variation along the device at V_{DS} = 0.5 V. The presence of larger potential barrier with increasing drain underlap, as shown, causes a reduction in the thermionic current component. However, for large values of V_{DS} where tunneling is dominant, a larger underlap also increases the field near the drain end and hence tunneling, thereby deteriorating quasi-saturation.

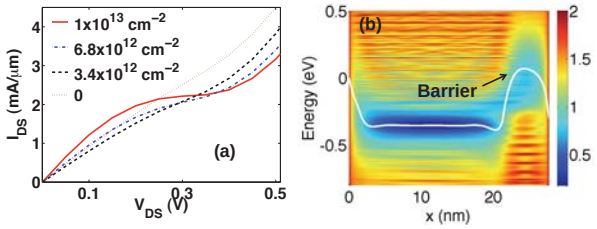

Fig. 6. (a) I_{DS} – V_{DS} characteristics at V_{GS} = 0.8 V for different concentrations of *p*-type doping in the 6 nm drain underlap region. (b) Logarithmic LDOS plot for N = 1x10^{13} cm^{-2} case at V_{DS} = 0.3 V. Variation of Dirac point is also shown in white. Doping increases the potential barrier shown in Fig. 4(b). The voltage window where the current is predominantly thermionic is enhanced leading to a significantly enhanced output resistance. The tunneling dominated region sets in at larger drain voltages with increasing doping density.

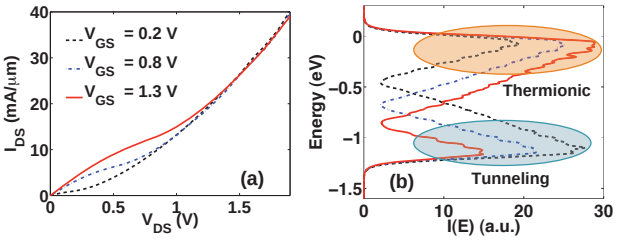

Fig. 2. (a) Simulated I_{DS} – V_{DS} characteristics for the nominal device for three different gate voltages showing quasi-saturation, the end of which is marked by concave to convex transition. Charge – potential self-consistency determines the location of inflection point. However, a direct correlation exists between this voltage and V_{GS}, as expected. (b) Corresponding plots of energy-resolved current ($I(E)$) at V_{DS} = 1.2 V showing thermionic (above the channel Dirac point) and tunneling (below) components of current in each case. At a given V_{DS}, a larger V_{GS} results in smaller tunneling current.

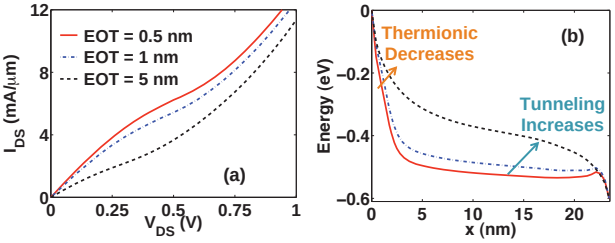

Fig. 3. (a) Output characteristics for GFETs with different EOTs at V_{GS} = 0.8 V. (b) Corresponding plots of Dirac point variation along the device at V_{DS} = 0.6 V. As EOT increases, although the total current decreases, the *relative* contribution of tunneling increases and that of thermionic current decreases due to smaller band bending at a given V_{DS} and a thicker barrier at source-channel interface – leading to a degraded quasi-saturation.

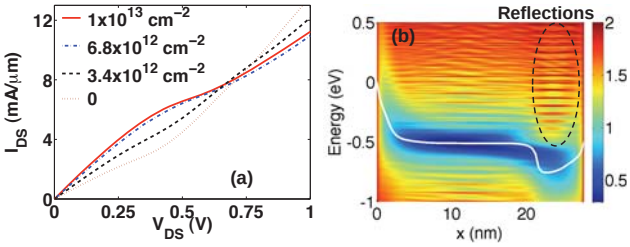

Fig. 5. (a) I_{DS} – V_{DS} characteristics at V_{GS} = 0.8 V for different concentrations of *n*-type doping in the 6 nm drain underlap region. (b) Logarithmic LDOS plot for N = 1x10^{13} cm^{-2} case at V_{DS} = 0.5 V. Variation of Dirac point is also shown in white. The doping reduces the tunneling component by introducing a barrier for holes, as shown, while simultaneously increasing the thermionic current due to enhanced band bending. The voltage at which tunneling current becomes significant is increased, hence improving quasi-saturation.

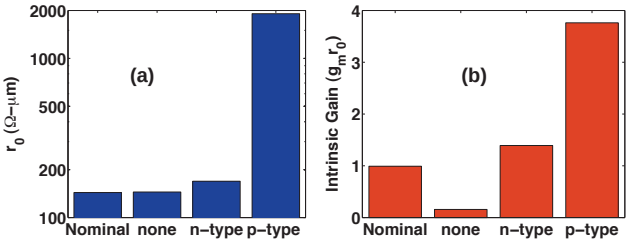

Fig. 7. Effect of drain-underlap engineering on (a) maximum output resistance (r_0) and (b) intrinsic gain ($g_m r_0$). The reported values in case of *n*- and *p*-type doping are for N = 1x10^{13} cm^{-2}. Although *p*-type doping increases r_0 compared to nominal device by 13x, a reduction in transconductance due to increased underlap makes the intrinsic gain achievable 4x.

Phonon Limited Transport in Graphene Pseudospintronic Devices

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Graphene pseudospin (G-PsS) devices have the potential to far outperform traditional CMOS devices. This is due to a predicted room temperature phase transition from Fermi liquid to Bose-Einstein condensate in double layer graphene [1]. The condensate is formed when electrons and holes in residing in opposite graphene layers bind into excitons as a result of strong interlayer Coulomb interactions. This device is expected to exhibit interlayer superfluidity, which allows for large interlayer currents at correspondingly low interlayer bias voltages. As G-PsS device are expected to operate at room temperature, it is important to understand how the electron-phonon interaction (EPI) affects device performance.

In Fig. 1, we plot a schematic of the device geometry we consider in this work. Our G-PsS device consists of two monolayers of graphene separated by 1 nm of SiO_2. We attach metallic contacts from which we may inject and extract current from each layer at the left and right side of the top (V_{TL} and V_{TR}) and bottom layer (V_{BL} and V_{BR}). We adjust the carrier concentrations of the layers using top, V_{TG}, and bottom gates, V_{BG} separated from the graphene layers by 20 nm of SiO_2. In this work, we define the gate voltage as, $|V_G| = V_{TG} = -V_{BG}$ and apply an interlayer voltage such that we measure the current flowing from V_{TL} to V_{BL}. The system temperature is set to $T_{sys} = 300\ K$. We employ the non-equilibrium Green's function (NEGF) formalism to examine the effect that carrier-phonon scattering [2] has on G-PsS device performance [3].

In G-PsS devices, one of the most important device characteristics is the critical current (I_c), or the maximum sustainable interlayer condensate current. In Figure 2(a), we plot the I-V characteristics with $|V_G| = 0.40$ V. We find that the critical current (I_c) for the ballistic case is $I_c \approx 18.4\mu A$, while $I_c^{ph} \approx 17.9\mu A$ with EPI included, representing a change of only 2.7%. This is to be compared with I_c, calculated at lower $|V_G|$. In Figs 2(b) and (c) show the I-V curves for $|V_G| = 0.30$ V and 0.20 V, respectively. At $|V_G| = 0.30$ V, we find that for the ballistic case that $I_c \approx 13.5\mu A$ and $I_c^{ph} \approx 9.2\mu A$ with EPI included representing a 31.9% drop in critical current. These values are to be compared with the results at $|V_G| = 0.20$ V, where we find a critical current of $I_c \approx 10.0\mu A$ for the ballistic case and $I_c^{ph} \approx 3.4\ \mu A$ with EPI included or a 66.0% drop in critical current. The dependence of critical current on $|V_G|$ in and out of the presence of phonon scattering is summarized in Fig. 3.

To explain this behavior, we consider the device coherence length, or the length which carriers propagate in the system before undergoing retroreflection [3]. As $|V_G|$ is decreased, the coherence length is expected to increase linearly for a set interlayer interaction strength. This increased coherence length allows carriers to travel farther into the device before being retroreflected thereby allowing them more opportunity to interact with the phonons in the layers. However, does not fully explain the non-linear drop in I_c when EPI is included. In Fig. 4, we plot the pseudospin stiffness, ρ_s which details the magnitude of the interlayer interactions, normalized to its value at $|V_G| = 0.4$ V. We expect, for a fixed interaction strength, that ρ_s should be nearly constant as seen in the ballistic case. With phonon interactions, we observe a clear non-linear drop is shown as $|V_G|$ is decreased. This is caused by phonon scattering energetically separating the excitons which breaks interlayer coherence and reduces ρ_s.

In conclusion, we find that the effect of carrier-phonon scattering has a strong dependence on the device coherence length. As such, for large $|V_G|$, the effect of phonons on interlayer transport is negligible. This behavior places limits on the gate voltage to achieve maximum device performance and must be considered when designing G-PsS devices.

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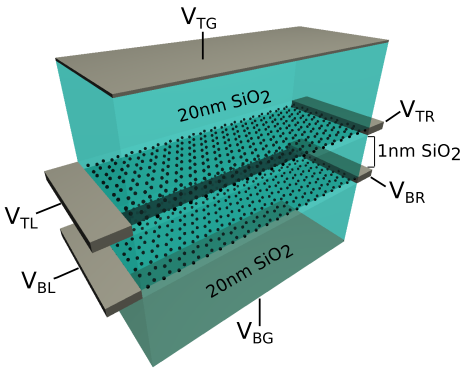

Figure 1: Depiction of the device studied in this work. Two sheets of graphene separated by 1 nm of SiO_2. Each layer has a separate set of contacts (V_{TL} and V_{TR} for the top layer and V_{BL} and V_{BR} for the bottom layer) from which current may be injected and extracted. The top and bottom gates, V_{TG} and V_{BG}, are used to adjust the layer carrier concentrations. The gates are biased such that V_{TG} = -V_{BG}, which provides optimal conditions to observe a room-temperature phase transition.

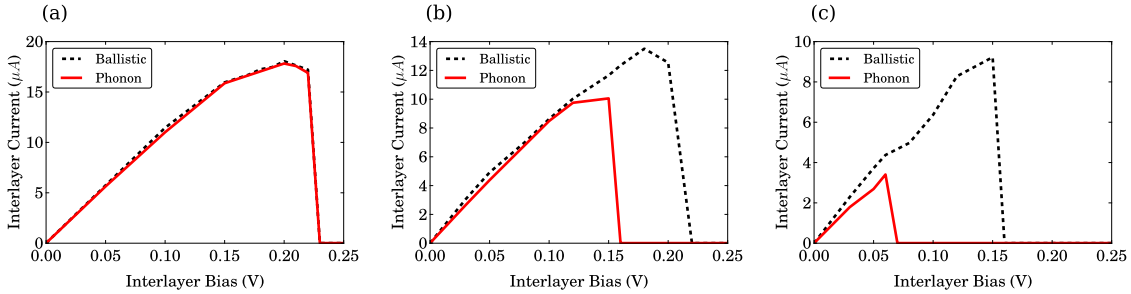

Figure 2: I-V curves showing the differences observed in interlayer transport with decreasing gate voltage, with and without phonon scattering. In the above plots, (a) $|V_G| = 0.4$, (b) $|V_G| = 0.3$, and (c) $|V_G| = 0.2$ V (left to right). As $|V_G|$ is decreased the coherence length increases, allowing phonons to interact more strongly with carriers and degrade the critical current.

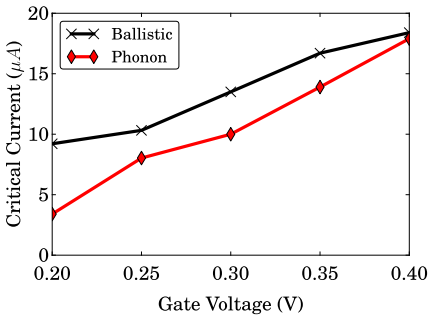

Figure 3: The value of the critical current (I_c) found at different values of the gate voltage ($|V_G|$) for both the ballistic case (black) and the phonon limited case (red).

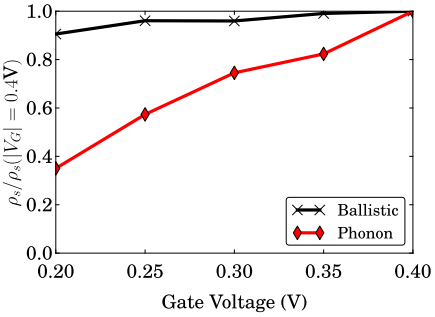

Figure 4: The average self-consistent value of the pseudospin stiffness (ρ_s) normalized to ρ_s at $|V_G| = 0.4$ V with and without phonon interactions. The ballistic value (black) decreases slightly due to confinement effects, but the phonon case (red) decreases more dramatically due to enhanced phonon scattering energetically separating the carriers at lower $|V_G|$ breaking the interlayer phase coherence at smaller interlayer biases.

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Resistive Switching in Aluminum Nitride

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Resistive random access memories (ReRAM), also referred to as memristors, have gained a great deal of attention recently as a potential high density, low energy replacement for flash and DRAM. Furthermore, the analog properties of this device are a potential enabler of neuromorphic computing. Of particular interest are the class of ReRAM based on based on the valence change mechanism and fabricated from transition metal oxides (TMOs) such as TaO_x and HfO_x [1]. This particular class of ReRAM have achieved record endurance (10^{12} cycles) [2], sub-nanosecond switching speeds [3], and demonstrated operation in 10x10 nm devices [4]. For the first time, we present resistive switching in a ReRAM structure with an AlN based switching layer. The electrical characteristics are very similar to those observed in the valence change class of ReRAM. In particular, we have observed bipolar switching at less than ±1V and repeatable linear current-voltage (I-V) behavior at subswitching (read) voltages similar to the electrical characteristics of TaO_x ReRAM. Physical analysis using TEM with electron energy loss spectroscopy (EELS) reveals that the switching layer contains oxygen, likely forming aluminum oxynitride (AlON).

Vertical Al/AlN/W MIM capacitor stacks were formed as illustrated schematically in Fig. 1. Starting with a conducting p-type silicon wafer, a 22 nm TiN adhesion layer, 100 nm Al bottom electrode, and 12 to 50 nm AlN switching layers were deposited in a single physical vapor deposition (sputtering) step, without breaking vacuum. Next, the structure was moved to the chemical vapor deposition (CVD) chamber for deposition of the 500 nm tungsten top electrode. It is important to note that during this transition, the top AlN surface was exposed to air, allowing oxygen to incorporate into the surface. Top electrodes were patterned and etched to form devices of areas ranging from $2.5x10^{-5}$ to 0.11 cm^2. A TEM image of the completed device is given in Fig. 2.

Electrical characterization was performed on a probe station in a dark box, using an Agilent 4156C with a 41501B Pulse Generator/Expander. I-V hysteresis loops (often associated with a memristor [5], sometimes called "figure-8" or "bowtie" curves) were used as a convenient method of demonstrating the highly linear behavior at sub-switching voltages (Fig. 3). This linear I-V behavior is similar to that observed in TaO_x. Linearity is desirable for analog use of the device, such as in a neuromorphic system. However, it creates challenges for use of the device as a ReRAM in large arrays because it necessitates a select-device to reduce "sneak-path" leakage current. Switching is bipolar, with the low to high resistance transition occurring near +1V and the reverse return to high resistance between -0.5 and -1V. Fig. 4 demonstrates bipolar switching between high and low resistance states with a short, high voltage pulse (~1µs at ±5V). Each curve in Fig. 4 is linear with regression coefficients > 0.999. Fig. 5 gives a plot of resistance versus cycle for a device's first 100 cycles. A maximum of 150 cycles has been achieved, but endurance has not yet been systematically studied. Typical R_{OFF}/R_{ON} ratios are on the order of 4 to 6. Devices with the thinnest (~12nm) switching layers had a much greater yield and higher endurance than thicker layer devices.

It is interesting to note that the proposed mechanism of transition metal oxide ReRAM is thought to involve the motion of oxygen anions under an electric field, which create defects that facilitate electron transport [1]. Clearly, oxygen vacancies cannot be created or destroyed in a pure AlN switching layer. It is also known that N has a very low ionic mobility in AlN [6]. However, as noted in the process flow above, the AlN layer is exposed to air before the top electrode is deposited. To further investigate the effect of exposure to air, we examined a device cross-section in a TEM using EELS to map out the chemical configuration. The corresponding EELS results of this are given in Fig. 6, which indicates a strong oxygen presence in the AlN film, likely forming AlON. Hence, it is possible that the switching mechanism in this AlN/AlON layer is still related to oxygen anion motion. Further work is needed to determine conclusively if switching can occur in a pure nitride layer.

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[4] B. Govoreanu et al., *IEDM 2011*, Dec. 2011.
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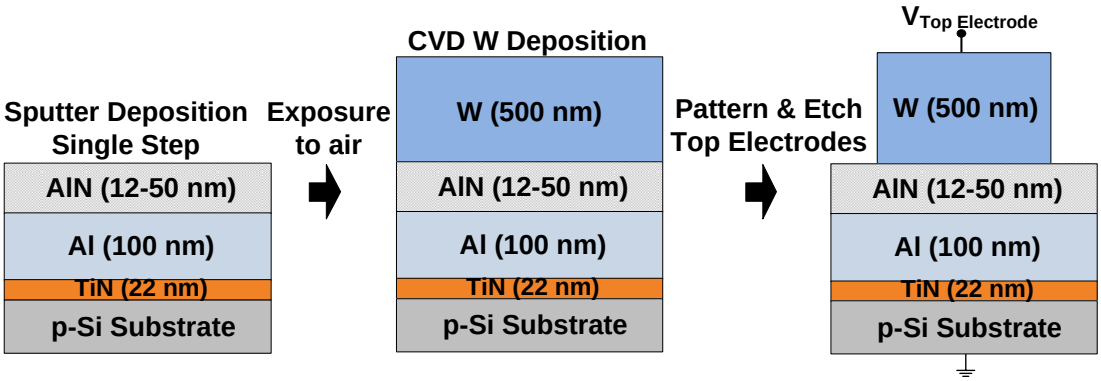

Fig. 1: Schematic illustration of the process used to create the AlN ReRAM structures and electrical connections.

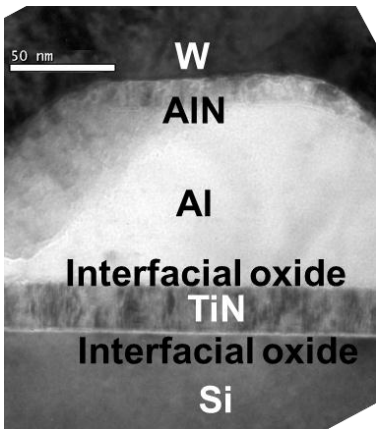

Fig. 2: TEM image of the completed AlN ReRAM.

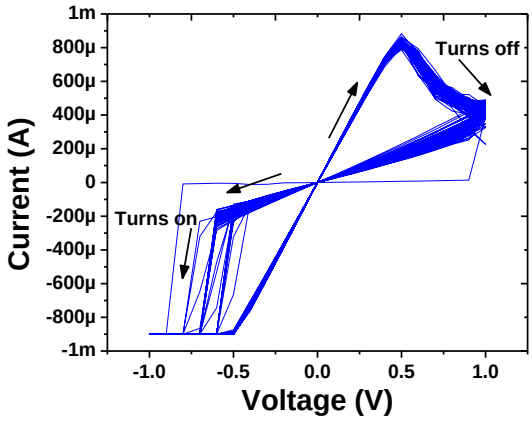

Fig. 3: I-V hysteresis with 100 switching cycles.

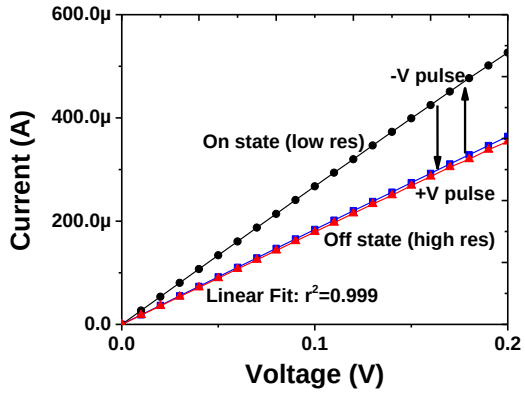

Fig. 4: Highly linear read I-V curves between on/off pulse.

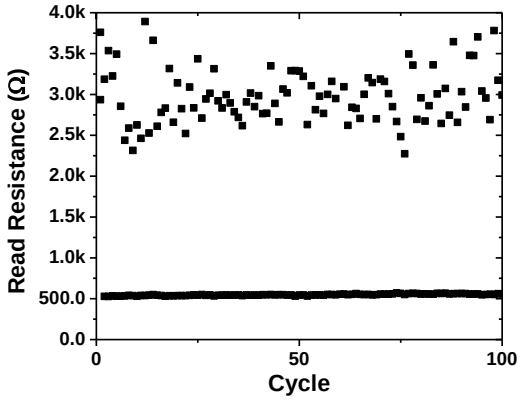

Fig. 5: Read resistance versus cycle for 100 cycles.

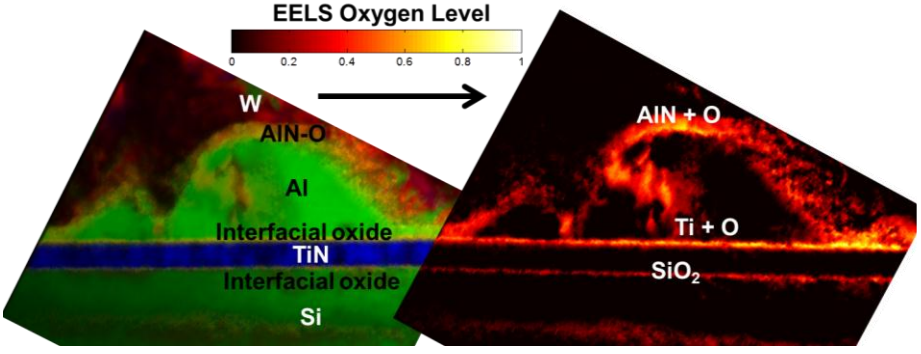

Fig. 6: (Left) False color EELS image with materials color coded matched with the corresponding (right) EELS plot of oxygen content over the device structure. This data indicates the possible formation of an AlON switching layer.

Limits of Detection for Silicon Nanowire BioFETs

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Over the past decade, silicon nanowire/nanoribbon field-effect transistors (NWFETs) have demonstrated phenomenal sensitivity to the detection of biomolecular species, with limits of detection (LOD) down to femtomolar concentrations [1].However, a fundamental understanding of these limits has been lacking until now. Several well known factors limit the LOD; among them, ionic concentration, efficiency of the biomolecule-specific surface functionalization, binding constants, and the delivery of the analyte to the sensor surface. However, the signal-to-noise ratio (SNR) of these bioFET sensors, and the device parameters that determine the LOD, are not well understood. For example, it has been commonly claimed [2] that NWFET sensitivity is maximized in the subthreshold operating regime of the device. We show here, contrary to this claim, that the SNR is maximized at maximum transconductance due to the effects of 1/f noise. These devices currently have a LOD of 4 electronic charges in ambient conditions..

Figure 1 shows a schematic of the device structure and experimental configuration, along with an optical micrograph and a scanning electron microscope image of typical nanowire devices, as well as typical transfer characteristics of a functionalized bioFET (as a function of solution gate voltage (V_{sg})). To determine the SNR, we perform low frequency (1/f noise) noise measurements. Typical normalized power spectral density plots and their gate voltage dependencies are shown in Figure 2. From such spectra the noise amplitude (defined as S_I at f = 1Hz) is extracted and used in calculating the SNR, which is defined as $g_m/\sqrt{(S_I)}$. The SNR is gate voltage dependent, and therefore the operating point needs to be carefully chosen to optimize the SNR [3]. The maximum SNR is obtained close to the peak transconductance, instead of the subthreshold regime due to enhanced 1/f noise in subthreshold as shown in Figure 3.

We additionally quantify the SNR in immersed solution conditions using standard pH sensing (eliminating surface functionalization variances). The response scales with the transconductance (g_m) as seen in Figure 4a. From the response (DI) we can determine the bias-dependent SNR, and obtain a peak SNR of 770 (Figure 4b.) From the measurements in Figure 3, we obtain a peak SNR of $59000V^{-1}$, resulting in a measured SNR of 1200, in reasonable agreement with experiment.

Using these devices, with very good performance in terms of SNR, we were able to measure and extract the binding kinetics of protein interactions, which have never been done with NWFETs. Binding constant determination is a critical parameter for biomolecular design, and has until now been primarily assessed by surface plasmon resonance (SPR) [4]. . Using NWFETs, typical binding kinetic curves are shown in Figure 5. Utilizing the low LOD of these devices, we are able to extract binding constants into the sub-picomolar range (Figure 6). The high sensitivity, reliability, multiplexing, and potential low cost make the nanowire/nanoribbon bioFET sensor a potential alternative to surface plasma resonance.

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[3] Rajan et al. *Applied Physics Letters*, **97**, 243501 (2010)
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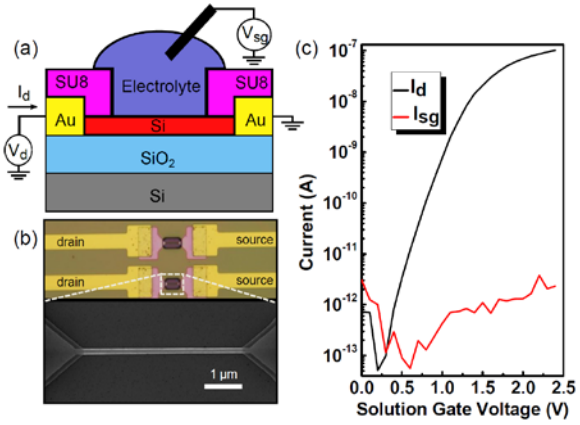

Fig 1.(a) Schematic of the device structure and the experimental setup. (b) Optical micrograph of two parallel nanowiresas well as a scanning electron micrograph of a single nanowire. (c) Typical I-V curve with voltage applied to the solution gate electrode. Gate leakage current is shown in red.

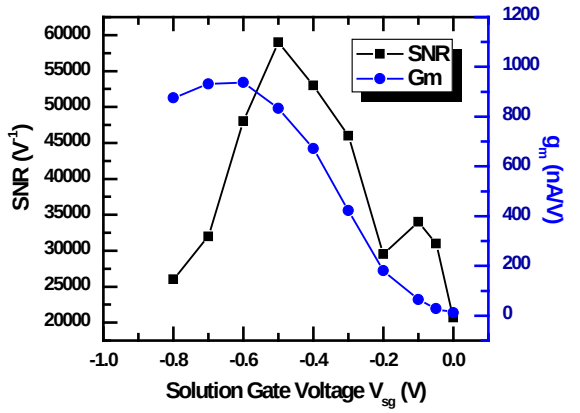

Fig 3. Signal-to-noise ratio plotted as a function of solution gate voltage for a p-type device. Peak SNR occurs at -0.5V and is equal to 59000 V^{-1}. Transconductance (g_m) also plotted as a function of solution gate bias confirming that SNR is maximized close to the peak g_m.

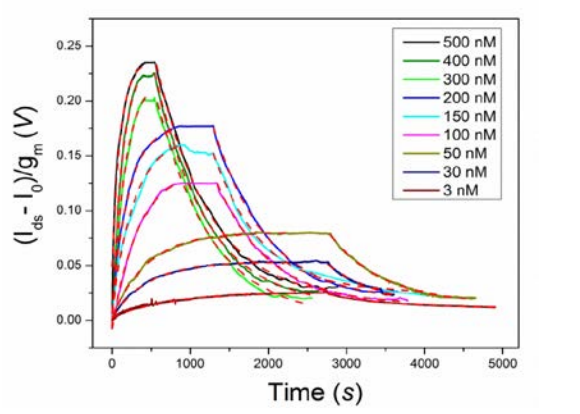

Fig 5. Real-time sensor responses of HMGB1-DNA binding.

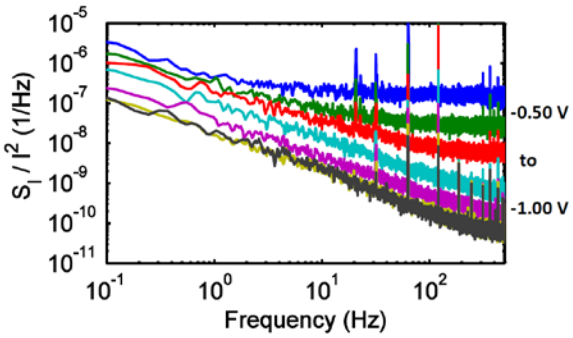

Fig 2. Typical 1/f noise spectra for a solution gated p-type device.

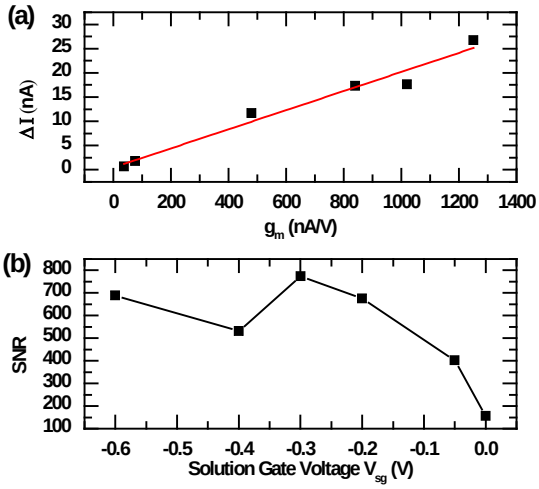

Fig 4. (a) Current response at different solution gate bias points with a pH sensitivity (calculated from the slope of the linear fit) of 39mV/pH. (b) Signal-to-noise ratio determined from pH sensing experiments (pH 7.45 to 7.95). Peak SNR is 770.

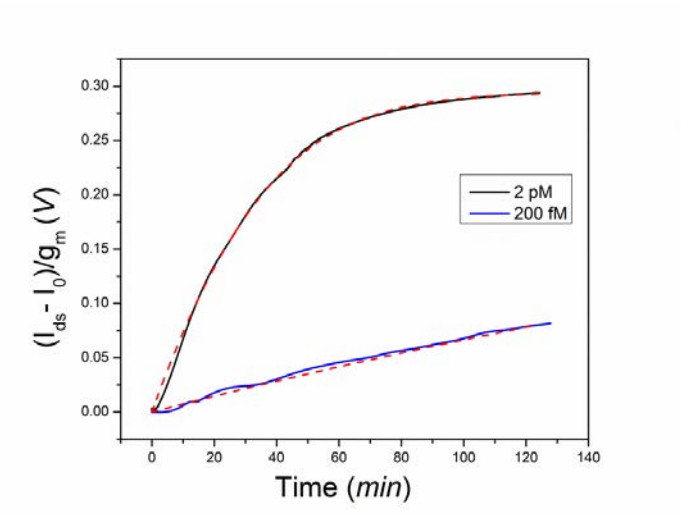

Fig 6. Real-time sensor responses of biotin-streptavidin binding.

Hole-blocking TiO_2/Silicon Heterojunction for Silicon Photovoltaics

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Narrow bandgap heterojunctions on crystalline silicon such as $Si/Si_{1-x}Ge_x$ are now in widespread use, but to date there has been little progress on widegap heterojunctions on silicon. In this abstract, we report:

(i) TiO_2/Si heterojunction with a band alignment which blocks holes from silicon but freely passes electrons, and

(ii) the application of this heterojunction to form a photovoltaic cell on silicon with no p-n junction, and all fabrication below a temperature of 75 ^oC.

TiO_2 is a widegap semiconductor with bandgap 3.2 eV, with conduction and valence bands at 4.0 and 7.2 eV below the vacuum level, respectively [1]. Thus, the TiO_2/Si interface is expected to have a large valence-band (VB) barrier ($\Delta E_V >> 0$) and a small conduction band offset (Fig. 1a). To experimentally test the band-offsets at the TiO_2/Si interface, test diodes were fabricated on p-type and n-type Si (100) wafers (structure and band-diagrams shown in Fig. 1b-d) by depositing 2-3 nm of TiO_2 by CVD at 75 ^oC, followed by a top metal electrode. As a control, diodes without the TiO_2 layer, having a Al/Si Schottky structure, were also fabricated. Ohmic Ag contacts at the bottom of the substrate served as the second electrode. Devices made on p-Si without TiO_2 showed ohmic I-V characteristics, typical of a Schottky barrier with a very low barrier for holes. Devices made on p-type Si with a TiO_2 layer showed rectifying (diode-like) I-V characteristics with a J_0 of ~10^{-8} A/cm^2 (Fig. 2). Since the currents in Schottky-type diode on p-Si are dominated by holes, the change in characteristics from ohmic to rectifying shows that TiO_2 blocks the holes in Si from moving to the top electrode, arguably due to the large hole barrier ($\Delta E_V >> 0$) at TiO_2/p-Si interface. In comparison, devices fabricated on n-Si showed ohmic characteristics even with the TiO_2 layer (Fig. 3). Since for n-type Si the majority carriers are electrons, the ohmic characteristics show that TiO_2/Si interface does not block electrons and ΔE_C is indeed small at TiO_2/n-Si. Assuming that the band-offsets at the TiO_2/Si interface do not change with Si doping type, the I-V characteristics qualitatively confirm the band-alignment posited in Fig. 1a.

We now describe one application of the thin hole-blocking TiO_2/Si heterojunction – Si photovoltaics. One possible approach to low-cost photovoltaics is though a merged TiO_2/crystalline-silicon solar cell in which the silicon p-n junction is replaced by the TiO_2/p-Si heterojunction (Fig. 4a). The light absorption still occurs in silicon, but instead of p-n junction, the cathode/TiO_2/p-Si heterojunction provides the electric field to separate the photogenerated carriers (Fig 4b). Such a TiO_2/Si structure is technologically interesting because it can be fabricated by a very simple low-temperature (~ 75 °C) CVD process, instead of high-purity high-temperature (900 °C) dopant diffusion process required for p-n junction. Motivated by similar arguments, we recently demonstrated a 10% efficient solar cell using an electron-blocking wide bandgap heterojunction on Si, which was fabricated by spin-coating a layer of the organic semiconductor, polythiophene, on n-type Si [2]. The present work demonstrates the complimentary technology, a hole-blocking heterojunction using TiO_2, fabricated by low-temperature CVD.

In this initial work, the transparent conductor is a thin layer of Al metal, 15 ± 5 nm thick. The bottom electrode and TiO_2 were deposited as before (Fig 4a). We also examined methods to the reduce J_0 of the TiO_2/p-Si solar cell because reduction in J_0 is the key to improvement in solar cell efficiency. In a metal/p-Si device, the hole current is the dominant part of J_0. However, TiO_2 blocks holes without affecting the electron, so it is possible that electron injection from cathode into Si (via TiO_2) is the dominant component in the J_0 of TiO_2/p-Si diodes (Fig 4b). To confirm, devices were fabricated on 10^{15} and 10^{16} cm^{-3} doped p-Si wafers. Assuming that the minority carrier diffusion lengths are of the same order in the two wafers, the higher doped devices should have lower electron injection and hence show lower J_0. I-V characteristics in dark (Fig. 5c) clearly show that devices on 10^{16} cm^{-3} Si indeed have a lower J_0 (10^{-9} A/cm^2 instead of 10^{-8} A/cm^2). Under 200 mW/cm^2 of illumination from a halogen lamp, this reduction in J_0 translates to a increase in open-circuit voltage from 0.47 V to 0.54 V (Fig. 5d). Due to unintended variation in the thickness of the semi-transparent top electrode, the short-circuit current varies from 9 mA/cm^2 to 18 mA/cm^2.

In conclusion, we demonstrate a novel low-temperature wide bandgap TiO_2/Si heterojunction, that selectively blocks holes but passes electrons and which could lead to low-cost but efficient crystalline Si solar cells.

[1] D. Gebeyehu, *et al. Synthetic Metals* **125**, 2001, 279. [2] S. Avasthi, *et al. Advanced Materials* **23**, 2011, 5762.

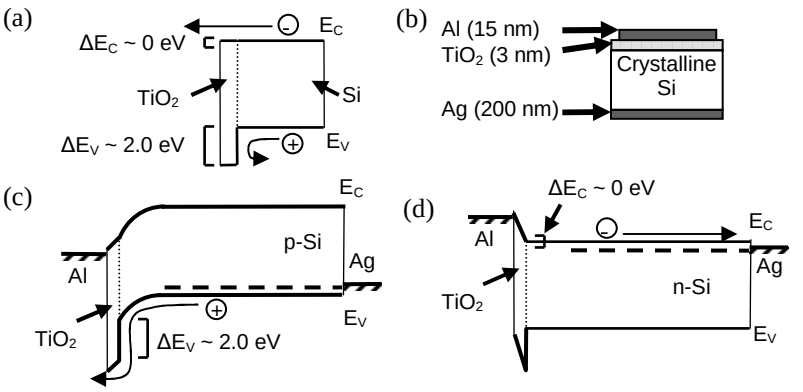

Fig. 1: (a) The expected band-offsets at a TiO_2/Si interface [1]. (b) Structure of the test diodes to experimentally measure the offsets. Band diagrams of the TiO_2/Si heterojunction test diodes on (c) p-Si and (d) n-Si, showing the flow of majority carrier in dark under positive bias on Ag electrode.

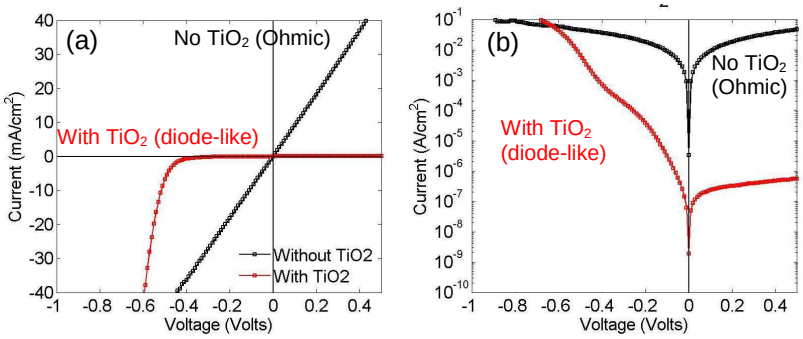

Fig. 2: The dark I-V characteristics of Al/TiO_2/p-Si heterojunction diode compared to Al/p-Si Schottky diode on a (a) linear and (b) semilog scale. Without TiO_2 the junction is ohmic but with TiO_2 the junction is rectifying, indicating that the TiO_2/Si junction blocks holes ($\Delta E_V >> 0$ eV).

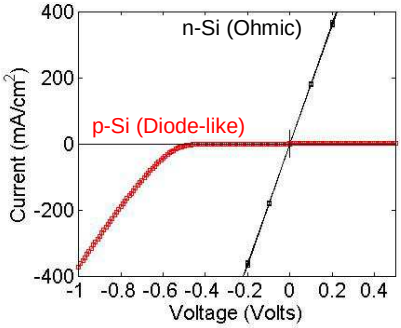

Fig. 3: The dark I-V characteristics of Al/TiO_2/n-Si heterojunction diode (black). Unlike TiO_2/p-Si (red), TiO_2/n-Si interface forms an ohmic contact, indicating that the TiO_2/Si junction does not block electrons

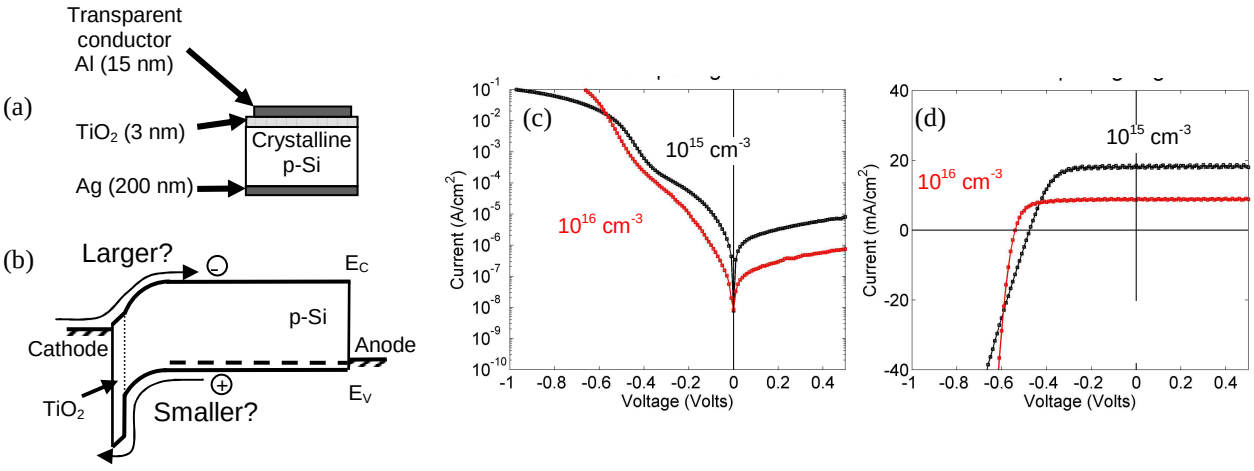

Fig. 4: (a) Structure of the TiO_2/pSi heterojunction solar cell (b) band-diagram of the solar cell, in dark and under forward-bias, showing the hole and electron currents. The I-V characteristics for 10^{15} and 10^{16} cm^{-3} doped Si wafers (c) in dark and (d) under 200 mW/cm^2 halogen lamp illumination. The variation in short-circuit current is probably due to unintended variation in the thickness of the Al electrode.

Recess Integration of Platelet Laser Diodes with Waveguides on Silicon

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We report the first demonstration of in-plane InGaAs/InP laser diodes integrated with SiON waveguides on silicon substrates using a modular recess-integration technique. This technique allows for pre-testing and selection of devices before integration, is compatible with integration on full CMOS wafers after conventional back-end processing is completed, and can be used to integrate multiple types of devices on a single wafer [1]. We feel it is superior to other optoelectronic integration techniques; more broadly, it is ideally suited to realizing robust, planar, monolithically integrated micro-systems incorporating a variety of materials and devices.

In the present research, 1.55 μm InGaAs/InP ridge laser diodes were fabricated in the form of platelets 150 μm wide, 300 μm long, and 6 μm thick [2]. Using a micropipette vacuum pick-up tool, pre-selected platelet lasers were placed into similarly sized recesses etched in a thick SiO_2 layer on a silicon wafer substrate. The recesses intersect SiON waveguides that were fabricated earlier within the SiO_2 layer [3], and the bonding layer thicknesses were chosen so that after assembly the waveguides of the platelet lasers will be co-axial with the SiON waveguides. Once all the lasers are in position, the substrate is placed on a heater strip and the lasers are all simultaneously bonded in place using a pressurized thermoplastic membrane to apply a uniform vertical force to hold them against a contact pad on the bottom of the recess while a solder bond is formed. In the present work contact was made to the upper p-contact of the integrated lasers by direct probing, but thin-film metal contacts deposited and patterned on the top surface could also have been used [1].

The integrated laser/waveguide units operate at room temperature with lasing thresholds of 17 mA pulsed and 19 mA CW, both of which are lower than the thresholds of comparable devices on InP substrates (consistent with the higher thermal conductivity of Si). Single-mode CW output powers in excess of 1 mW are measured from 1 mm long waveguides (the longest available on the present recess chips). Quantitative measurements of the laser-to-waveguide coupling efficiency are now underway, and comparisons to theoretical expectations will be discussed in the talk.

The integration of pre-selected laser diodes with waveguides on Si using a simple, flexible, modular technique is itself a significant accomplishment, and addresses a long standing need in the field of optoelectronic integration[4]. An equally important message, however, is that this integration approach can be used by anyone interested in the heterogeneous integration of a variety of diverse devices on Si integrated circuits and other substrates.

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1 An initial demonstration of this technique in which VCSELs were monolithically integrated with Si-CMOS electronics on a commercially processed IC chip is described in J. M. Perkins, C. G. Fonstad, *Optics Express*, Vol. 16, 2008, pp. 13955-13960.

2 J. J. Rumpler, C. G. Fonstad, *IEEE Photonics Technology Letters*, Vol.21, No. 13, July 2009, pp. 827-829.

3 E. Barkley, PhD Thesis, MIT DSpace, 2007.

4 See for example Di Liang, J. E. Bowers, *Nature Photonics*, Vol. 4, August 2010, pp. 511-517.

Figures for Famenini/Fonstad DRC Abstract:

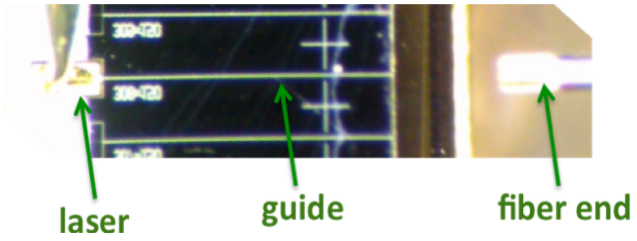

Fig 1a. A platelet laser diode bonded in a recess and coupled to a dielectric waveguide on a Si substrate. The end of a multi-mode fiber leading to a detector is seen on the right.

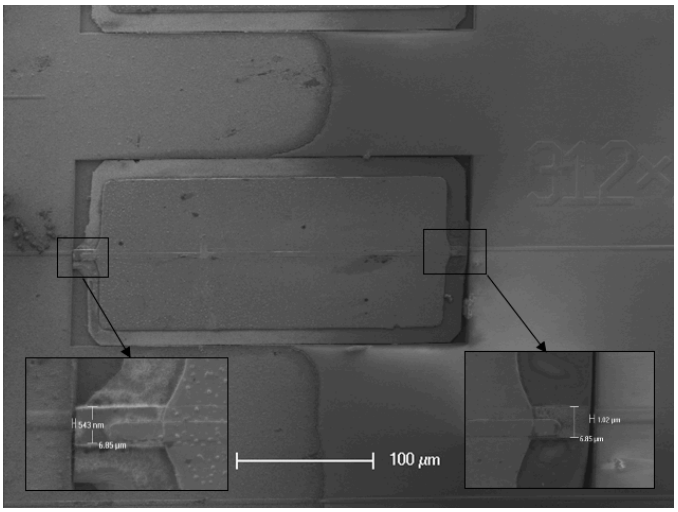

Fig 1b. SEM images of a laser assembled and bonded in a 312μm ×150μm mesa. The inset figures show the good horizontal alignment of laser ridge guide and dielectric waveguide. The gap widths are 1μm (right) and 0.55 μm (left).

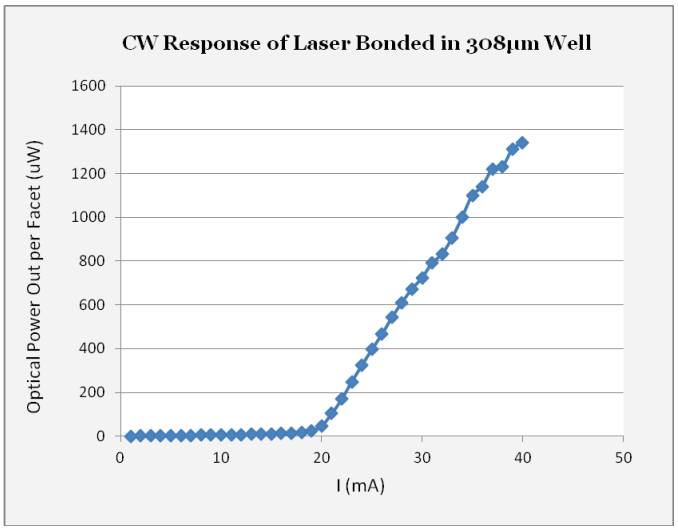

Fig 2. CW response of the integrated laser/waveguide system. I_{th}=19mA and T=15˚C. The response is measured with an InGaAs photodiode; P_{out}=1.34mW @ I=40mA.

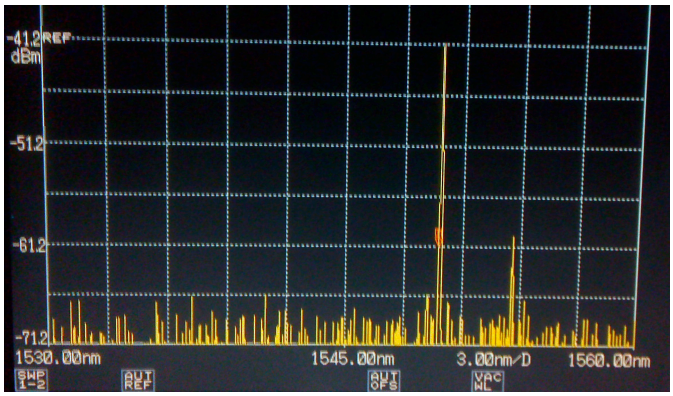

Fig. 3a: Spectrum of an integrated platelet laser measured by coupling the output from the dielectric waveguide through a multi-mode fiber to an optical spectrum analyzer. The CW drive current is I=31mA and λ_{peak}=1549.8nm.

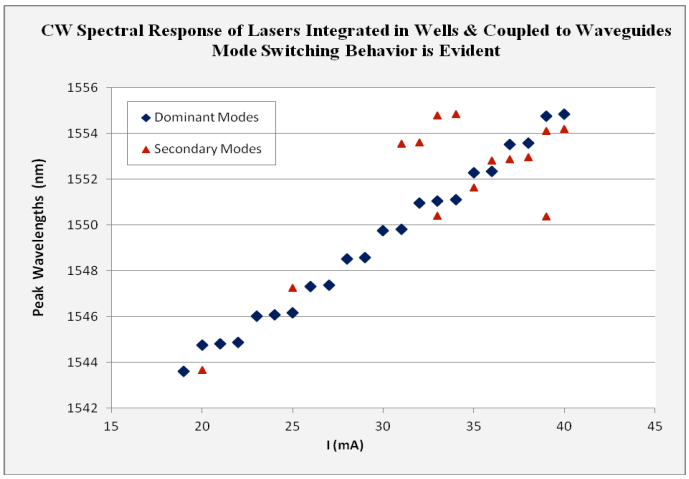

Fig. 3b: Peak lasing wavelengths of the primary mode (diamonds) and secondary modes within 15dB of the primary mode (rectangles) in the spectra. Analysis of this data will be included in the presentation.

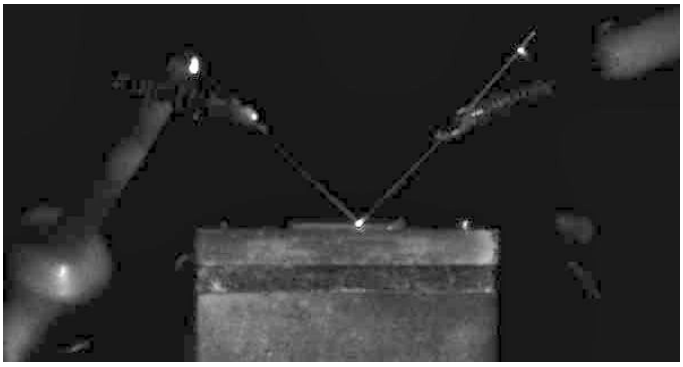

Fig 4: Digital photograph made with a Ge camera looking directly at the waveguide end and confirming that the light is coupled to the core and not traveling through the cladding or above it. The silicon chip is the thin slab immediately under the probes, and the large structure beneath it is the thermoelectric cooler.

NLSTT-MRAM: Robust Spin Transfer Torque MRAM using Non-Local Spin Injection for Write

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In this work we propose a magnetic random access memory (MRAM) bit-cell design based on non-local spin transfer torque (NLSTT) [1-4]. In the proposed bit-cell, the data is written into the free layer of a magnetic tunnel junction (MTJ) using spin diffusion current (non-local spin injection), without injecting charge current into the tunneling oxide [1-4]. Thus, the reliability issues, related to dielectric breakdown due to high tunneling current density (for high switching speed) are significantly mitigated [5]. Separation of read and write current paths in the bit-cell helps in optimizing read and write separately. Hence, higher MgO thickness can be used for higher cell TMR and higher read disturb margin. Higher MTJ resistance resulting from thicker MgO also lets us use voltage mode sensing, that achieves higher speed for read operation. In the proposed bit-cell, we employ two supplementary spin injectors with tilted axis anisotropy, in order to compensate for the comparatively lower efficiency for non-local spin injection [3, 4]. Analysis of the proposed NLSTT-MRAM bit-cell is done using a physics based simulation framework, benchmarked with experimental data for lateral spin valve (LSV) [4, 5]. Apart from high reliability, the proposed bit-cell achieves 110% higher tunnel magneto resistance (TMR) and 4X higher read margin for 1ns switching speed as compared to standard 1-transistor-1 MTJ (1-T 1-R) STT-MRAM of similar area.

The proposed NLSTT-MRAM (fig. 1) consists of an MTJ with its free layer in contact with a metal (Cu) channel. The magnets, m_2 and m_3 inject spin polarized charge current into the channel. Spin-polarized charge current is modeled as a four component quantity: one charge component and three spin components (Is_x, Is_y Is_z) [4, 5]. The low polarization interface of the free layer magnet, m_1 absorbs a fraction of the spin component of the channel current, and hence, experiences spin torque. Efficiency of the non-local spin injection can be defined as the ratio of the spin-current absorbed by the free layer to the net charge-current injected into the channel. It can be divided into two components: injector efficiency, which depends upon the injector-channel interface polarity, P, and non-local spin-absorption efficiency. Spin component of the injected current is only partially absorbed by the free layer, while rest of the portion is lost into the receiving injector (m_2 or m_3, depending on the direction of current flow). The non-local spin-absorption efficiency can, therefore, be enhanced by increasing the effective spin resistance of the injectors, by scaling down their area (fig. 2).This allows larger spin absorption by the free layer. Experimentally, ~10% overall efficiency has been demonstrated for non-local spin-injection, with P~0.5 and non-local absorption of ~20% [1, 4]. There is a scope for enhancement in both the efficiency components through improvement in magnet-channel interface, and, through optimization of the device geometry in order to facilitate higher non-local spin absorption.

For a given interface polarization, spin injection into the channel is enhanced by a factor of ~2, by incorporating two injectors with opposite polarity. For both the directions of current flow in the channel, the two injectors play supplementary roles. For instance, the up-spin electrons passing through the first injector into the channel face higher resistance at the interface of second injector with opposite polarity, and hence, the spin accumulation in the channel is enhanced for a given input current (fig. 3a). For a given spin injection efficiency, use of tilted axis anisotropy (30^o) for both the injector magnets can achieve ~3X reduction in the write-current for the proposed bit cell (fig. 3b) [7].

Use of NLSTT in the bit cell allows ultimate scaling of the free layer, as opposed to the three terminal bit-cell proposed in [6]. Although, the device structure in [6] employs a GMR interface for writing (zero tunneling current), due to write-current injection along the free layer, it necessitates a thicker and larger magnet. This results in significantly higher write-current and large switching delay. Free layer in the proposed bit-cell however, can be scaled to achieve higher switching speed for a given write-current (fig. 4) [4]. In order to maintain the spin-injection-efficiency, area of the injector magnets also needs to be scaled down proportionately.

Since in the NLSTT-MRAM bit-cell, the write current is not injected into the tunneling oxide of the MTJ, a relatively high oxide thickness can be chosen in order to achieve high TMR (fig. 5). Note that, although, the second injector with tilted anisotropy falls in the read current path, incorporation of a 1.6nm thick tunneling oxide still ensures more than 4X higher read disturb margin for the proposed cell as compared to an optimized 1T-1R STT MRAM bit cell, due to comparatively small transient read current (fig. 6). The upper limit of oxide thickness is determined by the speed of voltage mode sensing, which decreases with increasing oxide thickness (fig. 7).

The bit-cell with tilted-anisotropy dual-injectors requires a write current close to that required for local STT writing, even at 20% overall injection efficiency (fig. 8a). Further enhancement in the non-local spin injection efficiency would be conducive to lower write energy. In the proposed NLSTT MRAM bit cell, additional improvement in write energy can be obtained by lowering the bit line voltage (fig. 8b). This is because, the write current path is fully metallic and hence, there is no source degeneration for the write access transistor due to the high resistance tunneling oxide as in a 1T-1R STT MRAM bit cell. The write energy can also be traded with higher switching speed. Note that, the switching speed in a standard STT-MRAM cell is mainly limited by reliability issues, related to time dependent dielectric breakdown (TTDB) of tunneling oxide for high tunneling current density (fig. 9) [5].

Fig. 10 depicts the dual word line architecture for the NLSTT MRAM bit cell. Two word lines are used to control read and write access transistors. The bit-lines(BL) and the source-lines(SL) change roles for writing '1' and '0' in the bit cell, thereby governing the direction of current flow in the metal channel and hence, the write polarity. Note that, the results for comparison between the proposed bit-cell and 1T-1R STTM-RAM, presented in this work are obtained though iso-area analysis. A two-finger layout has been considered for the 1T-1R STT MRAM and a transistor width of 2X has been chosen as compared to that of the two individual transistors in the proposed bit-cell, in order to arrive at iso-area. This allowed a higher cell-TMR and larger write current (required for 1ns switching) for the 1T-1R STT-MRAM as compared to the minimum area case. The table in Fig. 12 compares the performance of the NL-STT MRAM bit-cell with that of a standard 1T-1R STT MRAM bit-cell.

Simulation of the NLSTT-MRAM device involves self-consistent solution of spin transport in the metal channel using Valet Fert's spin diffusion model and magnet dynamics using stochastic Landau-Lifshitz-Gilbert (LLG) equation [3, 4] (fig. 11). The simulation framework for non-local STT has been benchmarked with experimental results for lateral spin valves [3, 4]. For simulating the read operation the spin diffusion model is coupled with MTJ model based on self-consistent solution of Non-Equilibrium Green's Function (NEGF) and LLG (fig. 11) [8].

In conclusion, as compared to a standard STT-MRAM bit-cell, the proposed NLSTT-MRAM bit-cell, apart from exponentially higher reliability, can achieve high speed for read-write operation, high TMR and low read disturb failure. Further enhancement in non-local spin injection efficiency can render the proposed bit-cell structure an attractive alternative for the conventional 1T-1R STT MRAM for high speed non-volatile memory.

Acknowledgement: This research was funded in part by INDEX and Nano Research Initiative (NRI).

Reference: [1] Kimura et. al, Phys. Rev. Lett. 2006 [2] Sun et. al., Appl. Phys. Lett. 2009. [3] Behin-Ain et. al., Nature Nano. 2010 [4] Behin-Ain et. al, Appl.Phys.Lett. 2011 [5] Panagopoulos et al., DRC 2011. [6] Braganca et al., TNANO, 2009 [7] Majumdar et al., DRC 2011. [8] Majumdar et al., TED 2011.

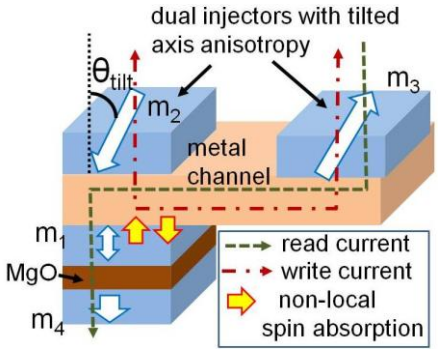

Fig.1 NLSTT-MRAM bit-cell device incorporating dual injectors with 30° anisotropy tilt.

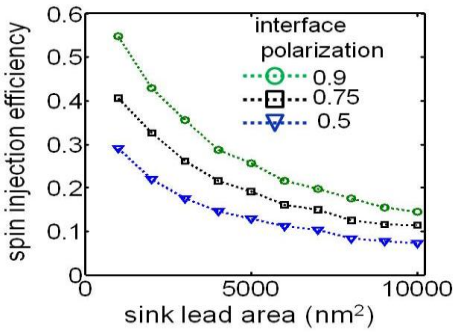

Fig.2 Effect of injector area upon spin injection efficiency for different values of *P* and a fixed input current

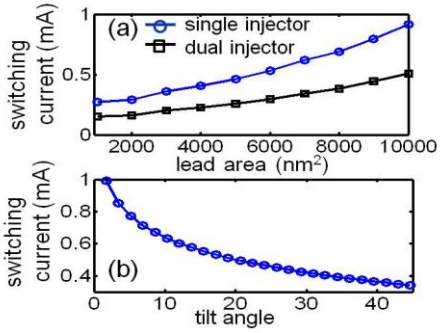

Fig.3 Use of (a) dual injector and (b) tilted anisotropy (30°) can achieve ~2X and ~3X reduction in switching current respectively

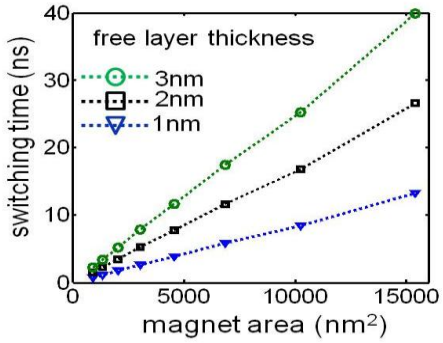

Fig.4 Effect of free layer scaling upon switching time, for a constant switching current

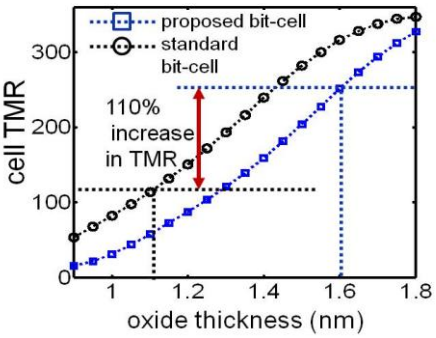

Fig.5 Higher t_{ox} leads to higher cell-TMR in the proposed NLSTT-MRAM and reduces reading errors.

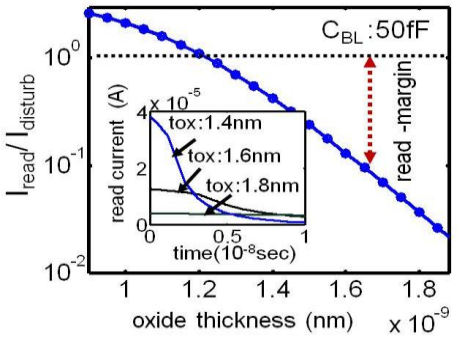

Fig.6 Voltage mode sensing for the thick oxide MTJ results in small transient read current and hence reduced read disturb failure

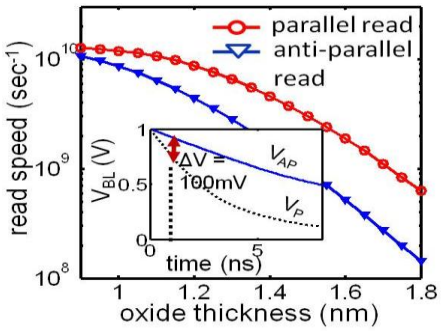

Fig.7 Voltage mode sensing for the high resistance MTJ units can achieve fast sensing at the speed of ~1ns

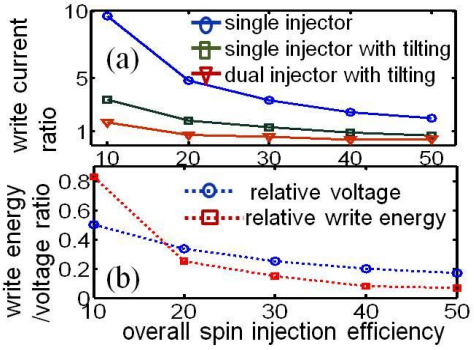

Fig.8 NLSTT-MRAM vs. 1T-1R STT-MRAM (a) write current, (b) write voltage and write energy with increasing non-local spin injection efficiency

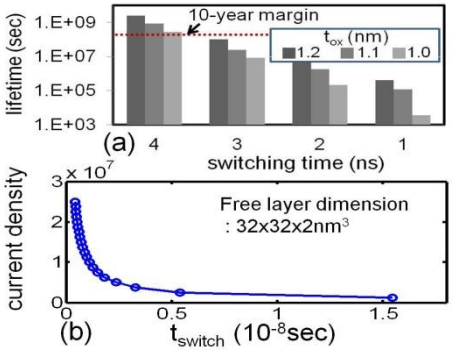

Fig.9 (a) Reliability analysis for 1T-1R STT-MRAM bit-cell using TTDB model in [5], shows poor lifetime below ~4ns of switching speed (b) MTJ tunneling current density vs. switching time

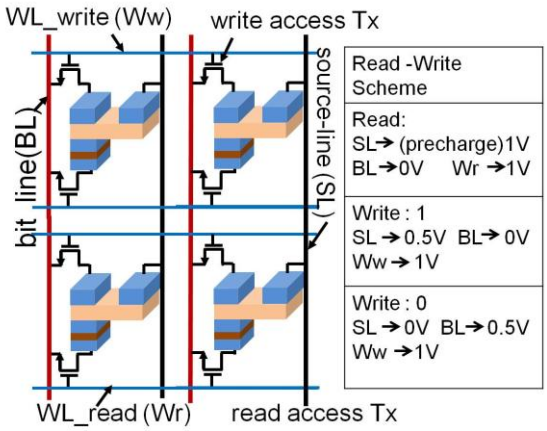

Fig.10 Dual word-line (WL) architecture for NLSTT –MRAM array

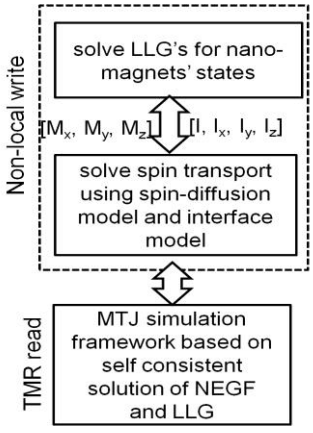

Fig.11 Spin diffusion-LLG simulation for non-local STT write, coupled with NEGF-LLG simulation for TMR read.

Design Attribute	NLSTT-MRAM (with 30° tilt, 20% spin injection)	1T-1MTJ Bit -cell
MTJ feature Size	32x32x2 nm³	32x32x2 nm³
Write Current	120µA	120uA (P→AP)
Transistor Width (16nm CMOS)	72nm (for both Transistors)	144x2 nm
R/W Voltage	1.0V/0.4V	0.3V/1.0V
Tox	1.6nm	1.1nm
Worst $I_{read}/I_{disturb}$	12%	45%
Cell TMR	260%	120%
Write Energy/bit	0.06 pJ	0.14pJ
Read Energy/bit	3fJ	15fJ
R/W Frequency	1GHz	1GHz

Fig. 12 Iso-area comparison of the proposed NLSTT-MRAM bit cell with the conventional 1T-IR STT-MRAM bit cell

All Spin Logic device as a compact artificial neuron

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In our recent work we have proposed the possibility of using magnets interacting via spin currents to implement all-spin logic (ASL) devices for information processing [1], fundamentally different from the standard charge-based architecture. Information is stored in the state of magnetization of the magnets and is communicated between magnets through pure spin currents.

Simulations of these multi-magnet networks (such as in Fig 1) with our experimentally benchmarked model [2] indicate that such spin-magnet circuits can mimic many of the attributes of standard charge-based circuits such as inverters, universal NAND/NOR gates [3], ring oscillators [4] etc.. However, these circuits do not take full advantage of the natural hybrid analog/digital character of spin currents and magnets, the possibility of which we discuss in this paper. Indeed, our contribution in this paper is twofold:

- We show that a simple model (LLG_z, Eqn 2a) of an ASL device (Fig 1), maps on to the well-known 'leaky integrate and fire' equation of neuron dynamics, highlighting the analogy of the magnet to a neuron.
- We introduce LLG_z for the first time in this paper and relate it to our full rigorous model [2]. We also show that LLG_z captures the steady state behavior of magnets predicted by the full model.

LLG_z (Eqn 2a), is a simplified form of LLG equation (Eqn 1); it only considers the dynamics of the easy axis component of magnetization (m_z) in presence of the easy axis anisotropy fields and collinear spin current (I_{sz}), i.e. the components of spin current which are collinear to the easy axis of a magnet. The simplification is inspired by two observations: (a) switching of a magnet implies switching of m_z from +1 to -1 or vice versa (b) stable states in collinear networks (Fig 1) are dependent mostly on I_{sz} and LLG_z predicts the same dynamic response of m_z to I_{sz} as the full model [2]. Analysis of stables states and switching characteristics for one magnet ASL unit (Fig 1b) shows that LLG_z predicts the same characteristics, thresholds and critical switching current ($I_{sz,crit}$) as the full model (Fig 2).

The switching characteristics in Fig 2 highlight two key aspects of ASL neuron behavior. Firstly, the one magnet ASL device switches between m_z=+1 and m_z=-1 with hard thresholds, reminiscent of a McCulloch-Pitts bipolar threshold neuron [5]. Secondly, the device exhibits hysteresis and can be considered as a hardware based device mimicking the characteristics of two state hysteretic neuron introduced by Takefuji *et.al.* [7]. The neuron-like characteristics can easily be understood from LLG_z (Eqn 1), which is equivalent to the well-known 'leaky integrate and fire' neuron equation (Eqn 2b), a commonly used model (Fig 3a) for describing bio-physically inspired artificial neurons. The 'voltage' in Eqn 2b is analogous to the magnetization of a magnet; the resistor is analogous to the damping in the magnetization dynamics. The non-linear 'voltage' dependent capacitor (Fig 3b) accounts for internal fields and stable states of the magnet. When m_z~0, the internal fields attempt to restore the magnet to the stable states. The 'capacitance' is lowest at this point (Fig 4) to allow transition to one of the stable states. However, when $m_z \rightarrow$+1 and $m_z \rightarrow$-1, the preferred stable states due to the internal fields of the magnet, the capacitance approaches infinity. Physically, this signifies that the magnet is stable in any of these magnetization states in the absence of external currents; the corresponding large 'RC time constant' (Fig 3b) prevents the stable magnetization state to 'leak' or flip to the other stable state.

The bipolar thresholds and hysteresis of this neuron can be observed in its response to an external current pulse (Fig 4). When the input spin current is greater than the (+) threshold (upper trip point), the magnet switches to the +1 state. If the input spin current is less than the (-) threshold (lower trip point), the magnet switches to the -1 state. If the value of the input is between the thresholds, the magnet does not change its state. The hysteresis and bipolar thresholds that is observed in ASL neurons may have advantages in neural computation as has been pointed out by various authors (see for example Refs [6], [7]). However, it must be pointed out that the hysteresis in the magnets is a function of the internal field, which can be reduced if so desired.

To summarize, we have discussed that a feature of the spin-magnet pair is that a magnet 'fires' (Fig 4), or switches, when the input spin current exceeds a threshold. The phenomenon can be described fairly well by a simple model (Eqn 2a) which maps on to the well known 'leaky integrate and fire neuron equation' (Eqn 2b). The neuron like behavior of ASL raises the possibility of multi-magnet all-spin networks (Fig 1) behaving as neuromorphic circuits suitable for hybrid analog/digital information processing.

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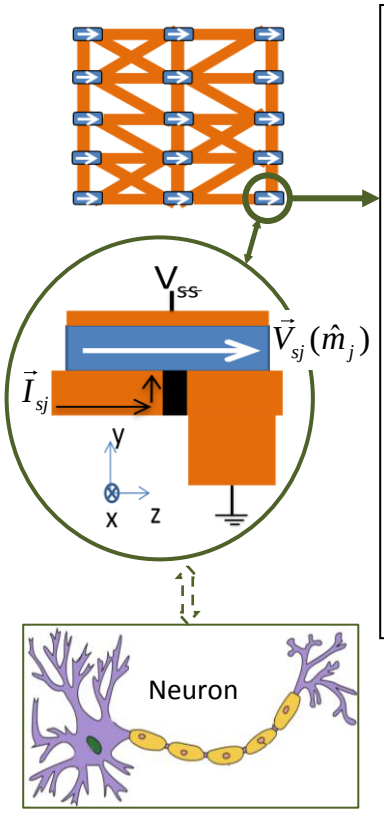


Fig 1. Magnet as a compact neuron. All spin multi-magnet networks consists of one magnet ASL devices whose behavior is similar to a neuron. V_{ss} : supply voltage, $\hat{m}_j$:magnetization of the 'j'th magnet, $\vec{I}_{sj}$ is the input spin current into the magnet. Neuron picture adapted from http://en.wikipedia.org /wiki/File: Neuron_Hand-tuned.svg

LLG

$$\frac{dm_j}{dt} = -|\gamma|(m_j \times \vec{H}_{int,j}) + \alpha m_j \times \frac{dm_j}{dt} + \frac{(\hat{m}_j \times \hat{m}_j \times \vec{I}_{sj})}{qN_j}$$

$\Downarrow$

LLG_z

$$\frac{dm_{jz}}{dt} = \frac{m_{jz}}{\tau}(1-m_{jz}^2) + \frac{I_{sjz}}{N_j q}(1-m_{jz}^2)$$

$\Updownarrow$

LIF

$$\frac{dV_{sjz}}{dt} = -\frac{V_{sjz}}{R_j C_j} + \frac{I_{sjz}}{C_j}$$

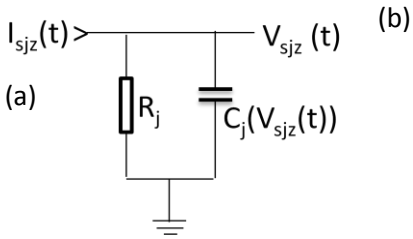
$$\frac{1}{C_j} = \frac{V_0}{N_j q}(1-m_{jz}^2)$$

Eqn 1. Landau-Lifshitz-Gilbert (LLG) Equation of magnetization dynamics in response to the spin current ($\vec{I}_{sj}$) computed using our 4-component spin circuit model [2].

Eqn 2 (a). LLG_z :A simplified model for getting insight into multi-magnet networks as in Fig 1. This equation was arrived at by considering only the easy axis ($\hat{z}$) component of LLG (Eqn 1). $\tau = 1/(\alpha|\gamma|\mu_0 H_k)$

Eqn 2(b). Eqn 2(a) can be rewritten as a 'leaky integrate and fire' (LIF) neuron equation, with a non-linear capacitor (Fig 3b). $V_{sjz} = V_0 m_{jz}$ $V_0 = -\left(\frac{\mu_B \mu_0}{q}\right) H_{kj}$

$$R_j = \frac{\hbar}{2\alpha N_j q^2}$$



(b)

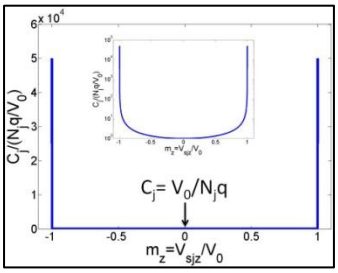


Fig 3(a). A schematic circuit representation of the 'leaky integrate and fire' (LIF) neuron equation (Eqn 2b) (adapted from C. Koch *et.al.* (1998)) with the voltage dependent capacitor (b) which approaches infinity when $m_z \rightarrow \pm 1$. The non-linearity of the capacitor explains the hard thresholds and hysteresis in Fig 2.

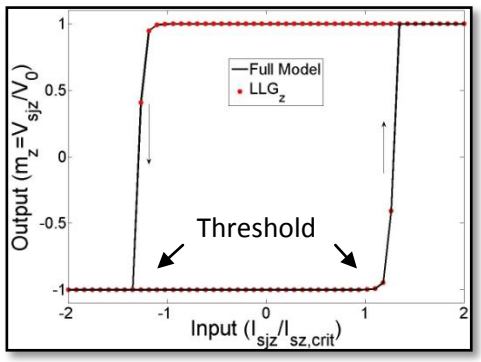


Fig 2. LLG_z (Eqn 2a) predicts the same characteristics as the full model [2]. The switching characteristics can also be considered to be the hysteretic activation function of the ASL neuron.

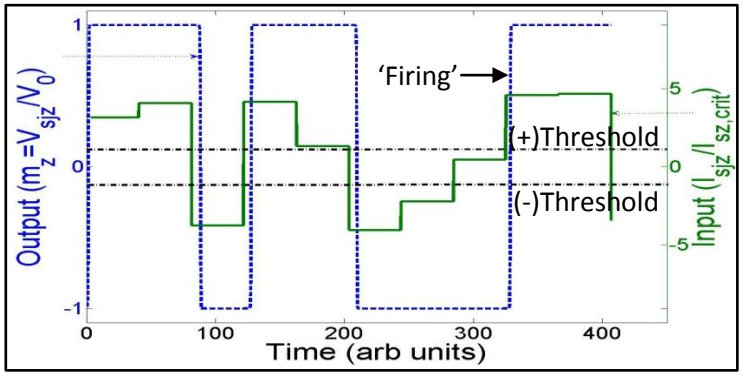


Fig 4. Response of an ASL 'neuron' in the multi-magnet network (Fig 1) to input spin currents from the neighboring neurons. The behavior of the neuron can be explained from Fig 2, it 'fires' to +1 whenever the input current is over (+) threshold and resets to -1 when the input is less than the (-) threshold. If the value of the input is between the thresholds, the magnet does not change its state.

Experimental Demonstration of "Cold" Low Contact Resistivity Ohmic Contacts on Moderately Doped n-Ge with in-situ Atomic Hydrogen Clean

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Abstract—Low contact resistivity ohmic contacts are demonstrated on *n*-Ge at doping level N_D of 1×10^{19} cm^{-3}. Atomic Hydrogen (**H***) clean was shown to reduce the specific contact resistivity (ρ_C) by 7% for the first time, due to reduction of barrier height of 70meV compared to the unclean sample. Improvement was primarily due to the reduction of the germanim oxide, GeO_x, and surface passivation at the interface by H atoms as confirmed by energy-dispersive X-ray spectroscopy (EDS). The ρ_C of 2.7×10^{-5} Ω-cm^2, at a moderate doping density of 1×10^{19} cm^{-3}, is the lowest with the minimum possible thermal budget.

Introduction—A metal-oxide-semiconductor field effect transistor (MOSFET) with Ge as the channel material has received much attention, mainly because the electron and hole mobilities are 2× and 4× higher than those in Si, respectively. Key challenges faced by Ge for *n*-MOSFET is the Fermi level pinning near the valence band which prevents formation of low contact resistivity ohmic contact, thereby degrading ON-current. Further, n-type dopants diffuse readily in Ge, limiting the thermal budget for formation of ohmic contact. In this work, we demonstrate formation of "cold" ohmic contact to n-Ge and study the effect of in-situ atomic H* clean on ρ_C for moderately doped *n*-Ge. Finally, we benchmark it with existing experimental and modeled results.

Results and Discussion—Fig. 1(a) shows the schematic of a 10^{19} cm^{-3} doped *n*-Ge structure grown on *p*-Si as substrate with i-Ge as a metamorphic buffer layer to accommodate the dislocations due to lattice mismatch. In-situ atomic H* clean was performed before PVD TiN deposition for one sample, in addition to an unclean, control sample of TiN/*n*-Ge. Fig. 1(b) shows the simulated energy band diagram indicating high Schottky barrier height of 0.57 eV [1] from conduction band edge due to pinned Fermi level. In order to extract the experimental ρ_C of deposited TiN on *n*-Ge, self-isolating circular TLM (CTLM) structures were fabricated on the unclean and H* dry cleaned samples. I-V data was measured for increasing TLM contact spacing (Fig. 2a); both samples showed symmetric, linear, non-rectifying characteristics for the entire current range, indicating ohmic contact formation between TiN and *n*-Ge. The total resistance extracted from I-V results as a function of contact spacing for both samples is shown in Fig. 2b. By numerically fitting the experimental resistance based on the CTLM model, ρ_C was extracted for both the samples. Low ρ_C of 2.9×10^{-5} Ω-cm^2, a sheet resistivity of 45 Ω/□ and L_T=8μm was obtained for unclean sample. An improvement of 7% was observed on H* cleaned sample exhibiting ρ_C of 2.7×10^{-5} ohm-cm^2. Cross-section TEM showed the presence of an interlayer at the TiN/n-Ge interface for the unclean sample, which was absent for the atomic H* cleaned interface. Energy Dispersive Spectroscopy (EDS) performed at the interface indicated monolayer oxide at the interface for unclean sample (Fig.4a); a clear reduction in the O peak was observed with atomic H* clean (Fig4b). In order to understand the dominant conduction mechanism across the contact, measurements at high temperature upto 150°C were performed on both the samples. As shown in Fig. 5, reduction in ρ_C was observed for T=25°C to 150°C for both samples. Modeling indicated thermionic field emission (TFE) as the dominant conduction mechanism for transport across TiN/n-Ge for $N_d=10^{19}$ /cm^3. To assess the observed improvement in contact resistivity with other data in the literature, we have benchmarked our experimental results (Fig. 6). Additionally, ρ_C as a function of N_D was modeled for Ge for comparison considering thermionic emission, thermionic field emission and field emission conduction mechanisms depending on the doping range. We have obtained the lowest contact resistivity for a non-alloyed, un-annealed M-S contact on *n*-Ge for $N_D=10^{19}$ cm^{-3}, which is 4 orders of magnitude lower than a similar M-S structure reported for similar doping [1]. The calculated ρ_C for the given N_D is 4× higher than that obtained experimentally, indicating a reduced Schottky barrier height of 0.5eV. In-situ H* clean results in removal of O from the surface and passivates with H* before metal deposition as confirmed by EDS, alleviating Fermi pinning [2]. If similar surface condition is maintained, very low ρ_C of $2\text{x}10^{-9}$ Ω-cm^2 can be obtained for high $N_D=10^{20}$ cm^{-3} using this process. Experimentation with higher doped n-Ge is in progress. The low contact resistivity achieved using minimal thermal budget is of much significance in order to prevent S/D dopant diffusion during high temperature contact annealing processes (Fig. 7), increasing the junction depth and in turn, degrading short channel effects for scaled n-Ge MOSFETs. Table I summarizes the experimental ρ_C data along with dopant and thermal treatment to elucidate the low thermal budget advantage of this process.

Conclusion—We demonstrate the lowest specific contact resistivity of $2.7\text{x}10^{-5}$ Ω-cm^2 for a non-alloyed, un-annealed M-S contact on *n*-Ge for low doping $N_D=10^{19}$ cm^{-3} with in-situ atomic H* dry clean and PVD TiN deposition. Fermi pinning was reduced by surface passivation by H* treatment resulting in decrease in SBH. Low thermal budget processing allows this process to be well-suited for ultra-scaled quantum well FET applications preventing diffusion of dopants in source/drain or channel material into the barriers.

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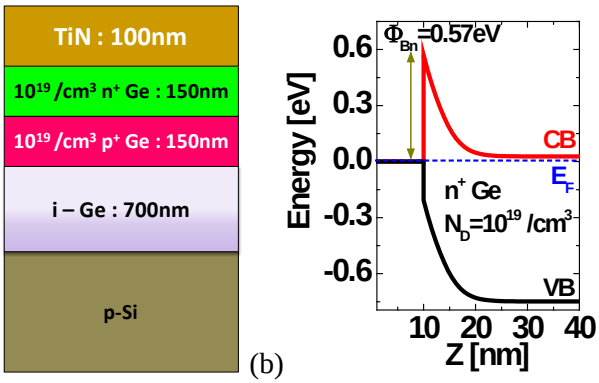

Fig. 1(a) Schematic of the TiN/n-Ge layer structure grown on p-Si (b) Calculated energy band diagram for TiN/n-Ge for $N_d=10^{19}$ /cm^3 indicating pinned Schottky barrier height of 0.57eV.

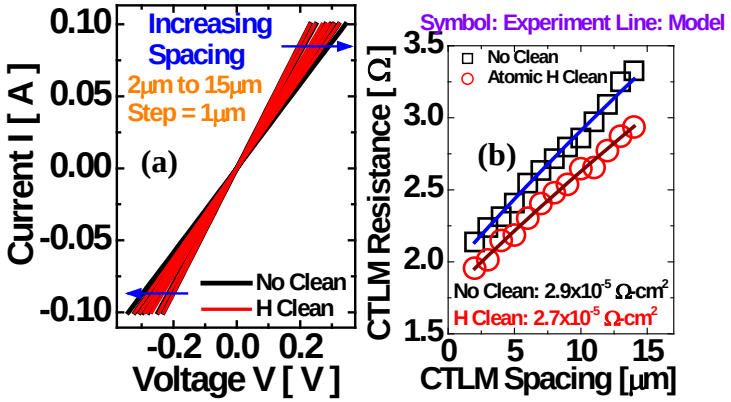

Fig. 2 (a) Experimental I-V characteristics of unclean and in-situ H cleaned samples for increasing slit width (b) Extracted total resistance as a function of CTLM spacing for unclean and atomic H cleaned samples, indicating reduced contact resistivity for latter case.

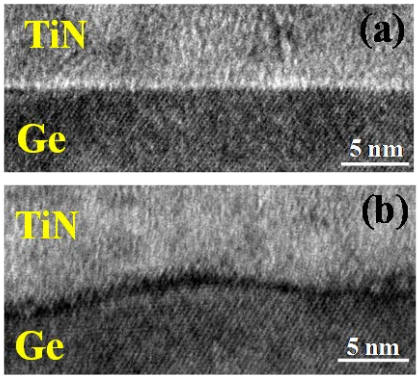

Fig. 3 Cross-section TEM of (a) unclean TiN/n-Ge sample showing thin interlayer at the interface , (b) atomic H* cleaned sample showing no interlayer at the TiN/n-Ge interface

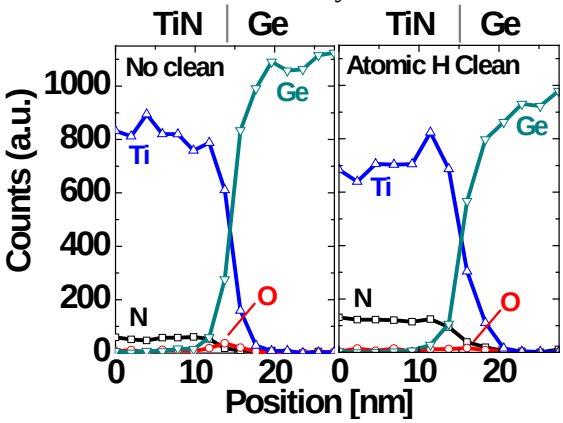

Fig. 4 Energy Dispersive Spectra (EDS) of unclean and atomic H cleaned sample at the interface. Oxygen peak is observed at the interface of unclean sample, which was reduced as a result of atomic H* clean, resulting in improved contact resistivity for latter sample.

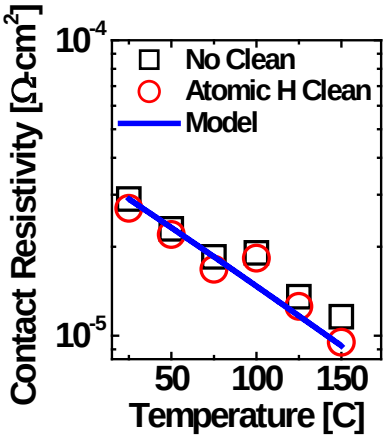

Fig. 5 Experimental and modeled contact resistivity characteristics at T=25°C to 150°C for unclean and atomic H cleaned samples.

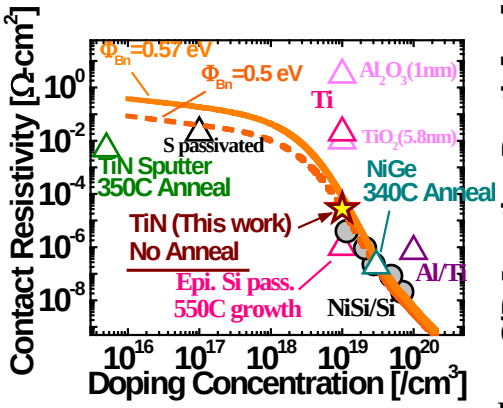

Fig. 6 Benchmarking of experimental contact resistivity as a function of doping concentration for various contact architectures on *n*-Ge, along with analytical model for SBH=0.57eV and 0.5eV. Measured contact resistivity on n-Ge is similar to NiSi/n-Si for same doping.

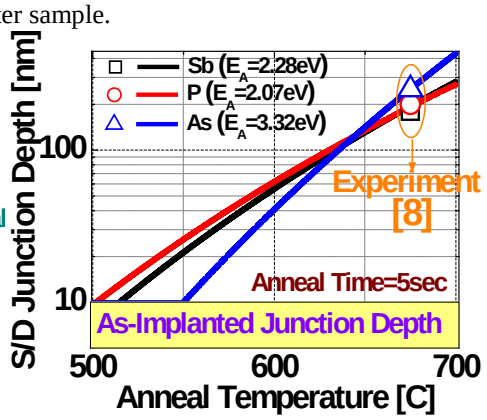

Fig. 7 Simulated source/drain junction depth vs. contact anneal temperature for common n-type dopants P, As and Sb on Ge with indicated activation energy. As implanted junction depth was assumed to be 10nm and anneal time was set as 5sec. Minimal thermal budget prevents dopant diffusion leading to better short-channel effects for scaled n-Ge MOSFETs

Contact	Dopant	Doping (/cm^3)	Anneal. (C)	ρ_C (Ω-cm^2)	
Ti	P	N.A.	650	6x10^{-5}	[3]
Ti	Sb	10^{20}	LSA	7x10^{-7}	[4]
NiGe	As	10^{19}	250/300	2.5x10^{-6}	[5]
NiGe	N.A.	N.A.	300	4x10^{-5}	[6]
TiN	N.A.	6x10^{15}	340	4x10^{-3}	[7]
TiN	P	10^{19}	No Anneal	2.7x10^{-5}	--

Table I Contact resistivity values on *n*-Ge reported till date for various contact architectures indicating doping and annealing conditions.

Mobility and Scattering Mechanisms in Buried InGaSb Quantum Well Channels Integrated with in-situ MBE Grown Gate Oxide

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InGaSb material family with its higher hole transport properties are potential candidates for group III-V CMOS circuits. Understanding of the dominant scattering mechanisms is crucial for the development of future high speed, low power device applications. We present Hall mobility data of p-type InGaSb quantum well (QW) channels and derive the dominant scattering mechanisms related to the interface and trapped charges that degrade mobility in these structures.

The $In_{0.36}Ga_{0.64}Sb$ QW structures were grown on semi-insulation (SI) GaAs(001) substrates by molecular beam epitaxy. Fig. 1 shows a schematic of these structures. A 1.3 μm thick undoped metamorphic $Al_{0.8}Ga_{0.2}Sb$ buffer layer grown at 520^0C was completed with a 3.4nm thick modulation Be-doped layer to achieve dopant concentration of 1.5×10^{12} cm^{-2} and 14nm thick AlGaSb spacer serving as a bottom barrier of the QW. In the buried channel samples, the QW channel grown at 460^0C was capped with a top barrier layer of various thicknesses of $Al_{0.8}Ga_{0.2}Sb$ with 1nm thick top GaSb or InAs capping layer. The samples were then transferred to high-k deposition chamber under UHV conditions and then aluminum was evaporated in O_2 gas environment (~10^{-6} Torr) to grow 10nm thick Al_2O_3. Hall mobility and sheet concentration data were measured using Van der Pauw configuration under magnetic field of 0.5 T.

By varying the top barrier thicknesses of GaSb/$Al_{0.}$GaSb on QW, we observed the influence of interface and oxide related scattering on the hole transport in QW structures. Fig. 2 illustrates a degradation of mobility by about 30% when the barrier thickness is reduced from 50nm (that can be considered to have negligible effect of interface-related scattering) to 0 nm (surface QW channel). The effect of the semiconductor/oxide interface is remarkably low as compared to its influence on electron mobility in InGaAs channels, where the mobility drops by 6-7 times in the similar structures. The Hall mobility dependence on hole sheet concentration (Fig. 3) shows the peak at about 10^{12} cm^{-2}. The temperature dependence (Fig. 4) of thick top barrier showed a slope close to $\mu_{bulk}\sim T^{-1.1}$ when mobility μ is limited by dominant bulk phonon scattering whereas for thinner top barrier and surface channels, the slope is approaching $\mu\sim T^{-0.66}$. Interface-limited mobility, μ_{int} has been extracted using Matthiessen's rule (equation in the Fig. 5 captions). Fig. 5 (left) shows that the interface-limited mobility curves level out for the samples with thin barriers. This behavior is consistent with dominating interface roughness scattering that is typically temperature insensitive. In the samples with the hole density below 10^{12} cm^{-2} (sample with the 5nm top barrier) the room temperature slope becomes slightly positive that likely indicates the remote Coulomb scattering (RCS) by the oxide and interface charges. It is also clearly seen in Fig.5 (right) where the samples with 3nm-thick barriers and different hole concentrations are shown.

Instead of 1nm thick GaSb capping layer, we also tested a 1nm InAs capping or 0.5 nm thick amorphous Si interface passivation layer (IPL) (which is oxidized to SiO_x layer during high-k oxide deposition) on top of GaSb capping layer. The InAs capping have shown up to ~25% improvement of room temperature mobility RT for 3nm thick total InAlSb/InAs top barrier (Fig. 2). Use of a-Si IPL has resulted in a significant (over an order of magnitude) reduction of the hole density in QWs and corresponding drop of mobility which is clearly becomes RCS-limited (Fig. 6). Interestingly capacitance-voltage (CV) studies of p-GaSb MOSCaps (Fig.7) show visible improvements in CV's but a considerable negative flat band voltage shift in the structures with a-Si IPL which is in agreement with the depletion of the channel.The trap density values are also reduced when a-Si IPL is used (Fig. 7) and cannot be responsible for hole trapping. Reduction of the channel hole density is, therefore, explained by the formation of the dipole layer in the GaSb/SiO_x/Al_2O_3 interface.

10nm in-situ Al_2O_3
GaSb(or InAs)+AlGaSb top barrier
10nm $In_{0.36}GaSb$ QW
14nm $Al_{0.8}GaSb$ spacer
3.4nm p-AlGaSb modulation doping
1.5 μm NID-$Al_{0.8}Ga_{0.2}Sb$ buffer
0.2 μm NID GaAs buffer
Semi-Insulating GaAs substrate

Fig. 1: Schematic of QW structures used for transport measurements.

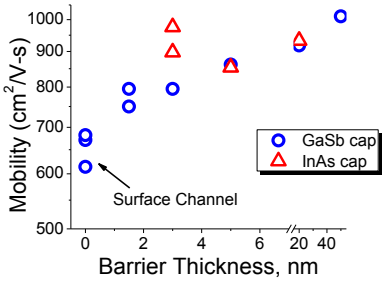

Fig. 2: Dependence of room temperature Hall mobility on top barrier thickness in InGaSb/InAlSb/cap/Al_2O_3 QW stacks with 1nm thick cap GaSn or InAs layers . Hole density is (1-2)×10^{12} cm^{-2}.

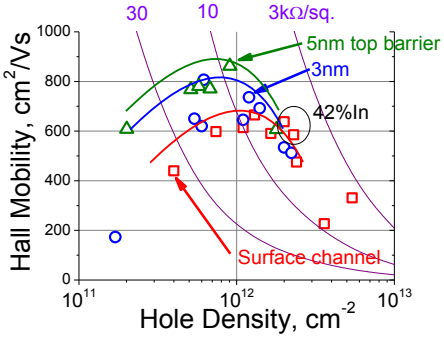

Fig. 3: Hall mobility as a function of sheet hole density in InGaSb/InAlSb/GaSb/Al_2O_3 QW stacks with different top barrier thicknesses. Lines are drawn to aid the eye.

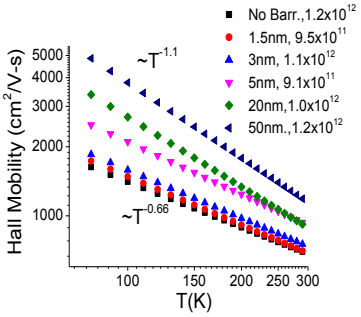

Fig. 4: Temperature dependence of Hall mobility for varying top barrier thickness and specified sheet hole density.

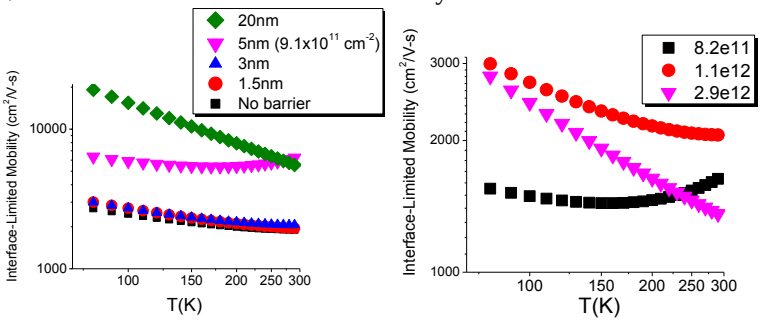

Fig. 5: Extracted interface related mobility using Matthiessen's rule: $\mu^{-1} = \mu_{bulk}^{-1} + \mu_{int}^{-1}$, (left) for various top barrier thicknesses hole density of ~(1.1-1.2)×10^{12} cm^{-2} (except the 5nm-barrier sample with lower concentration); and (right) for 3nm top barrier sample with different sheet hole densities.

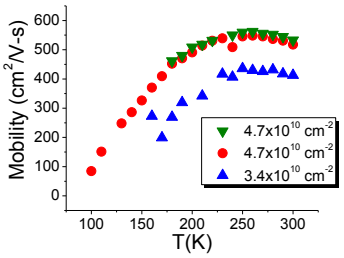

Fig. 6: Temperature dependence of Hall mobility for samples with a-Si passivation layer that resulted in significant reduction of hole density in QW and RCS-dominating mobility.

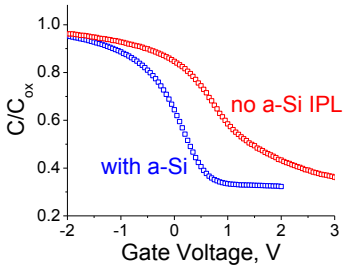

Fig. 7: 1MHz capacitance-voltage characteristics of p-GaSb/Al_2O_3 gate stack with and without 0.5nm thick a-Si interface passivation layer showing negative shift in flat band voltage with a-Si IPL.

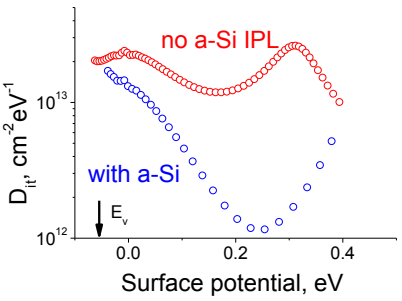

Fig. 8: Interface trap density (D_{it}) extracted from CV curves in Fig.7 using Terman method. Curves when a 0.5nm thick a-Si IPL is used.

Dielectric Thickness Dependence of Quantum Capacitance in Graphene Varactors with Local Metal Back Gates

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Introduction: It has recently been proposed that the quantum capacitance effect in graphene could be utilized as a platform to realize passive wireless sensors [1]. The very high mobility and energy-dependent density of states make it an ideal material for realizing high quality factor (Q) variable capacitors (varactors), which, when combined with on-chip inductors, could enable ultrasmall sensors with wireless readout capability. It has previously been reported that varactors with capacitance tuning ratios as high as 4:1 and $Q >$ 40 at 1 GHz could be possible using realistic assumptions for the graphene properties [2]. However, in order to achieve such performance, metal-dielectric-graphene capacitors with effective oxide thicknesses (*EOT*) values ~ 1 nm need to be realized. Most previous work involving thin dielectrics on graphene have been performed using top-gated devices [3]. However, it is difficult to achieve low *EOT* with top gates due to the problem of nucleating high-κ dielectrics directly on graphene [4]. Furthermore, varactors using top-gated geometries are not well-suited for sensing applications, since the graphene is not exposed to the surface. In this work, we study the gate dielectric thickness dependence of quantum capacitance using ALD-deposited HfO_2 layers with varying thickness. Varactors with tuning ranges >1.5:1 at room temperature are demonstrated and the effect of random potential fluctuations and area-transfer efficiency are studied.

Device Description: The fabrication sequence for the varactors is shown in Fig. 1(a)-(d) and started by growing 280 nm of thermal SiO_2 on a lightly doped p-type silicon substrate. Next, a quasi-planar gate electrode was formed by patterning photoresist and recessing the SiO_2 before evaporating Ti/Pd (10/40 nm). HfO_2 was deposited by atomic-layer deposition (ALD) at 300 ^oC, and annealed to 400 ^oC for 5 minutes in N_2. Single-layer graphene grown by CVD on a Cu foil was then transferred onto the wafer using an aqueous transfer process. The graphene was then patterned and etched in an O_2 plasma, and finally, contact electrodes to the graphene consisting of Ti/Au (10/100 nm) were patterned and lifted off. An optical micrograph of a completed device with gate area of 8 x 5 x 40 μm^2 is shown in Fig. 1(e). The samples were tested in vacuum (~ 10^{-7} Torr) using a cryogenic probe station. Before measurement, the samples were vacuum baked at 380 ^oC for 30 hours to desorb moisture from the graphene. The C-V measurement were performed using a Agilent B1500A with a capacitance-measurement unit using an ac voltage of 50 mV and a frequency of 500 kHz.

Results: The temperature-dependent C-V characteristics for two samples with target HfO_2 thicknesses of 20 nm (sample A), and 10 nm (sample B) are shown in Figs. 2 and 3. The results show that the capacitance tuning range increases with decreasing HfO_2 thicknesses, as expected. A comparison of the normalized C-V curves for both samples at room temperature is shown in Fig. 4. The capacitance tuning range from $V_g - V_{Dirac}$ = 0 to +1.5 V is 1.17:1 for sample A and 1.38:1 for sample B. Fig. 5 shows a comparison of the C-V characteristics for the varactors with MIM capacitors fabricated on the same sample. A very consistent trend is observed where the capacitance-per-unit-area for the MIM capacitors is significantly higher than for the varactors. The *EOT* values extracted from the MIM capacitors are found to be 4.1 nm and 2.7 nm for samples A and B, respectively. In order to understand this behavior in more detail, numerical modeling was performed on the temperature-dependent C-V characteristics where the random potential fluctuations, σ, in the graphene was used as an adjustable fitting parameter [5]. The results are shown in Fig. 6. The fact that the fitted *EOT* values cannot completely account for the capacitance reduction in Fig. 5 is a strong indicator that the effective device area of the varactors is less than the layout area. However, additional modeling, particularly taking into account the effect of interface traps, and other imperfections between the graphene and HfO_2 [6-7] is needed to fully understand the observed behavior. In the future, further scaling of the *EOT* needs to be investigated, as well as fabrication of the devices on insulating substrates for eventual use in resonator circuits. As a preliminary demonstration (Fig. 7), we have fabricated a single-finger varactor on a quartz substrate, with *EOT* (as determined by MIM capacitors) of 1.9 nm and tuning range >1.5:1 at room temperature.

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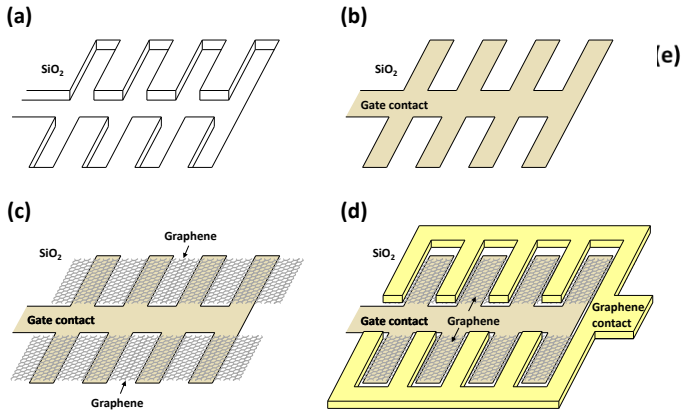

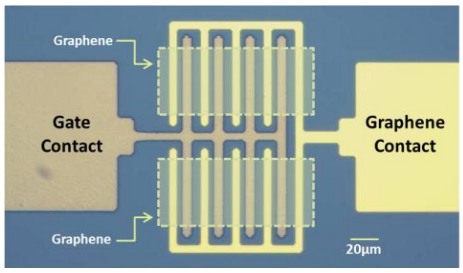

Fig. 1. (a)-(d) Fabrication sequence for local-backgated graphene varactors. (e) Optical micrograph of completed graphene varactor, where the graphene location has been highlighted for clarity.

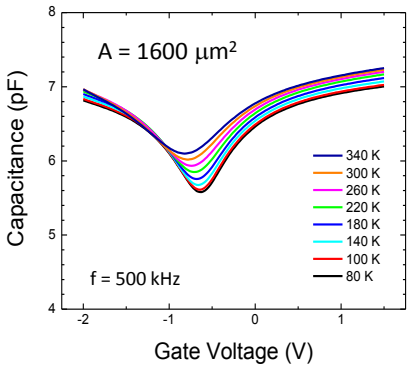

Fig. 2. Temperature-dependent C-V characteristics for a graphene varactor on sample A.

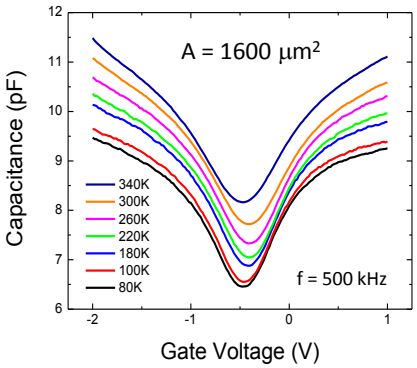

Fig. 3. Temperature-dependent C-V characteristics for a graphene varactor on sample B.

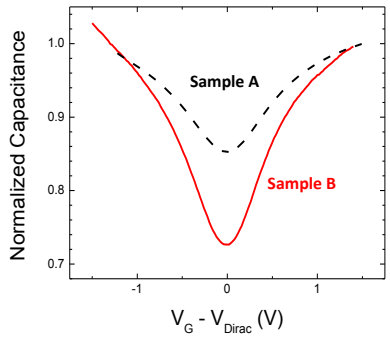

Fig. 4. Comparison of normalized C-V curves for varactors on samples A and B at T = 300 K.

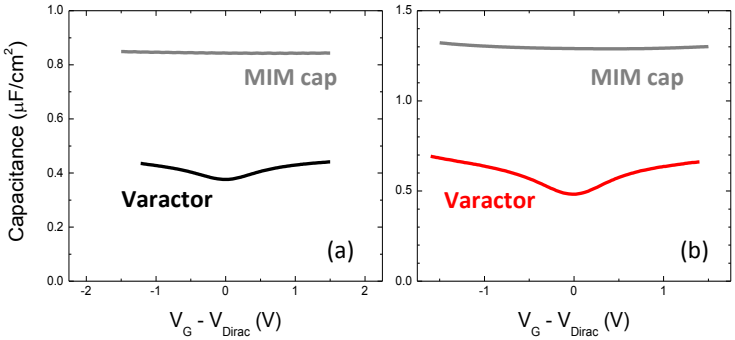

Fig. 5. Capacitance per unit area comparison for MIM capacitors and varactors on (a) sample A and (b) sample B. The *EOT* values extracted from the MIM capacitors are (a) 4.1 nm and (b) 2.7 nm.

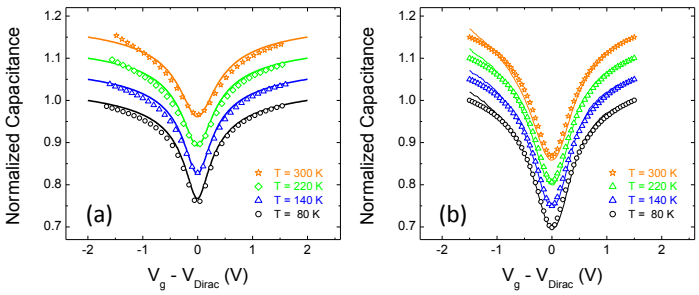

Fig. 6. Experimental (points) and calculated (lines) C-V curves for varactors using a model including random potential variations. The fitting values are (a) *EOT* = 6.8 nm and σ = 65 mV for sample A and (b) *EOT* = 2.7 nm and σ = 105 mV for sample B.

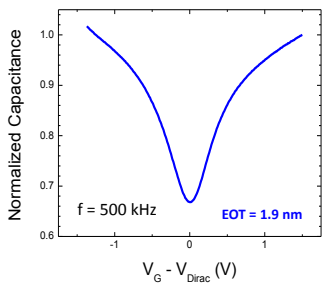

Fig. 7. C-V curve at T = 300 K for a varactor on a quartz substrate with MIM-cap-extracted *EOT* of 1.9 nm. The tuning range between $V_g - V_{Dirac}$ = 0 and 1.5 V is 1.50:1.

Negative differential resistance in short-channel graphene FETs: semianalytical model and simulations

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We discuss the phenomenon of negative output differential resistance of short-channel graphene FETs at room temperature, whose physical origin arises from a transport-mode bottleneck induced by the contact-doped graphene. We outline a simple semianalytical model, based on semiclassical ballistic transport, which captures this effect and qualitatively reproduces results from the non-equilibrium Green's function approach (NEGF). We find that this effect is robust against phonon scattering.

Introduction. Graphene is receiving considerable attention for potential applications in analog RF electronics due to its high carrier mobility and Fermi velocity, which could allow device operation in the THz range of frequencies. Recently, negative differential resistance (NDR) has been demonstrated in experimental graphene field effect transistors (GFETs) with long-channel lengths [1], and also in quantum transport simulations of ballistic short-channel devices [2, 3]. However, in the latter case, its origin has not been completely elucidated, in particular with regard to the role of self-consistent electrostatics. In this work, we develop a new semianalytical model for GFETs which is able to explain the origin of the NDR effect in short-channel devices, and we compare it with NEGF results.

Models. The semianalytical model assumes an ideal square potential barrier and a fixed shift $\Delta E_{\rm con}$ of the Fermi level with respect to the Dirac point in the metal-doped source and drain regions (Fig. 1-top). The semiclassical ballistic transport model is summarized by Eqs. 1–2, where $D_{S/D}$ is the density of states in the channel relative to injection from source/drain, and M is the number of propagating modes. The model for D_S, D_D, and M (Eqs. 4–6) is illustrated in Fig. 1-bottom (ϑ is the Heaviside step function; $k_{S/D/G}$ and $\theta_{S/D}$ are defined in the figure) and accounts for the transport modes bottleneck effect across the series of p-n junctions as described in [4]. The same model for M has also been used to describe NDR in single p-n junction devices [5]. Essentially, the transmission probability across the junctions is either 0 or 1 as dictated by the conservation of the transverse k. The Dirac point in the channel $E_{d,G}$ is self-consistently computed through the capacitive model in Eq. 3, which assumes a zero workfunction difference between gate and graphene. To benchmark the simple model, we use an atomistic full-quantum code for graphene nanoribbons [6], based on the self-consistent solution of the NEGF and 3D Poisson equations and optionally including acoustic and optical phonon scattering. The source and drain regions are treated as in the semianalytical model with a given $\Delta E_{\rm con}$ and semi-infinite extensions (as in [3] with $\Delta = 0$). The parameters for scattering are $D_{\omega,\rm AP} = 0.03$ eV^2, $D_{\omega,\rm OP} = 0.027$ eV^2, and $\hbar\omega_{\rm OP} = 160$ meV: the symbol definition can be found in [7].

Results. In Fig. 2, we plot the output characteristics for $V_{\rm GS} \leq 0$ (p-type channel) obtained with the semianalytical model and $\Delta E_{\rm con} = 0.4$ eV (n-type contacts), EOT = 0.5 nm, which clearly show NDR. Interestingly, if one neglects the finite number of modes in the source and drain, i.e. by setting $k_S, k_D > k_G$ and thus $\theta_S = \theta_D = \pi/2$ in Eqs 4–6, the current increases monotonically (cfr. [8]). The origin of the NDR effect is explained by looking at the energy spectra in Fig. 3: for energies close to $E_{d,S}$, M is limited by the number of modes in the source and leads to the quasi-saturation behavior of the current for μ_D approaching $E_{d,S}$ [3]; in addition, due to a hole pile-up in the channel and the electrostatic feedback, $E_{d,G}$ is lowered and the current actually decreases rather than saturating due to the decrease of $M(E)$ for energies between μ_S and μ_D. The qualitative shape of the output characteristics is confirmed by ballistic NEGF simulations (Fig. 4) considering a 50-nm-channel length. From Fig. 5, it can be seen that the assumption of square potential barrier is well justified and that the barrier lowering is similar; the lower current spectrum in the NEGF case can be explained with wavefunction mismatch at the junctions causing partial reflection [4]. Finally, we have investigated the effect of phonon scattering and found that, at this channel length, it is too weak to affect the NDR. (Fig. 6).

Conclusions. The semi-analytical model presented here is shown to capture and explain the NDR effect in short-channel GFETs. The discrepancy with the NEGF simulations is attributed mainly to quantum reflection at the junctions, while phonon scattering does not alter the picture. The model could be used in the first optimization pass towards the engineerization of the NDR.

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Equations of the semi-analytical model:

$$n = \int_{E_{d,G}}^{\infty} \mathrm{d}E\,[D_S(E)f_S(E) + D_D(E)f_D(E)] \quad (1)$$

$$I = \frac{2q}{h}\int_{-\infty}^{\infty} \mathrm{d}E\,M(E)[f_S(E) - f_D(E)] \quad (2)$$

$$q(n-p) = C_{\mathrm{ox}}\,(-\mu_S/q + V_{\mathrm{GS}} + E_{d,G}/q) \quad (3)$$

$$D_S(E) = \frac{|E - E_{d,G}|}{(\pi\hbar v_F)^2}\,2\,[\theta_S + (\theta_S - \theta_D)\vartheta(\theta_S - \theta_D)] \quad (4)$$

$$D_D(E) = \frac{|E - E_{d,G}|}{(\pi\hbar v_F)^2}\,2\,[\theta_D + (\theta_D - \theta_S)\vartheta(\theta_D - \theta_S)] \quad (5)$$

$$M(E) = \frac{2W}{\pi}\min\{k_S, k_D, k_G\} \quad (6)$$

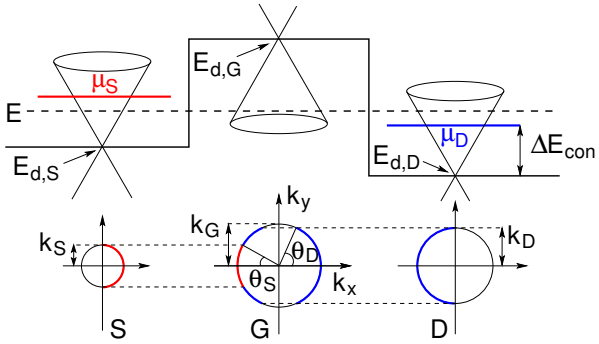

FIG. 1. Dirac point profile (top) and population of states in k-space (bottom) corresponding to the indicated energy E: electrons from the source (red) are perfectly transmitted through both junctions (thus populating only rightward propagating states in the channel); the ones from the drain (blue) enter the channel with probability one and are either perfectly transmitted or totally reflected at the source-channel junction depending on the angle of incidence (thus populating both left- and rightward propagating states).

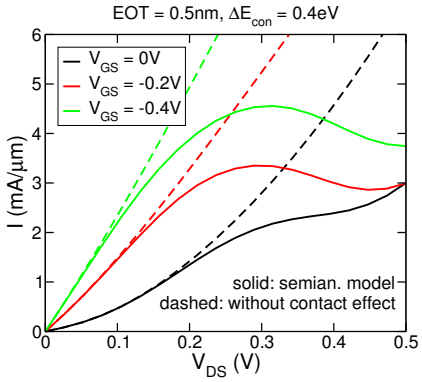

FIG. 2. Normalized output characteristics for $V_{\mathrm{GS}} \leq 0$ (n-p-n configuration) from the semianalytical model and the one obtained by assuming $k_S, k_D > k_G$: the former shows an NDR effect.

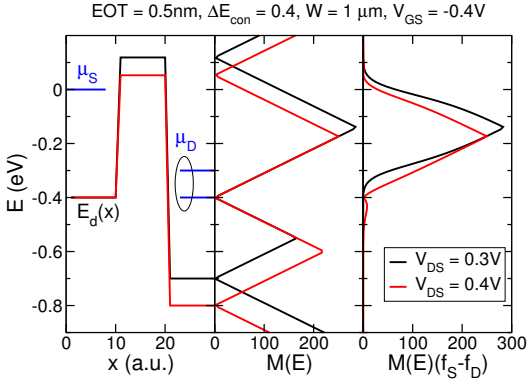

FIG. 3. Dirac point profile (left), number of propagating modes versus energy (center), and current spectrum (right) from the semianalytical model, for two different V_{DS}. By lowering μ_D, a hole pile-up is induced in the channel; this, in turn, causes a lowering of the Dirac point and a decrease in $M(E)$, which is not fully compensated by the larger $(\mu_S - \mu_D)$, resulting in a smaller current.

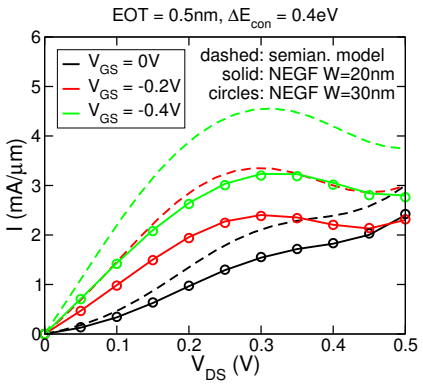

FIG. 4. Normalized output characteristics for $V_{\mathrm{GS}} \leq 0$ from the semianalytical model and ballistic NEGF simulations of nanoribbons with two different widths W: the two NEGF sets overlap indicating that the nanoribbons are wide enough to behave as 2D graphene.

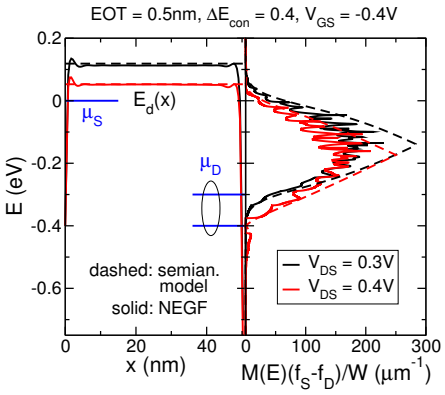

FIG. 5. Dirac point profile (left) and current spectrum (right) from the semianalytical model and from ballistic NEGF simulations. The barrier lowering is similar, while the difference in the current spectra can be attributed to wavefunction mismatch at the junctions.

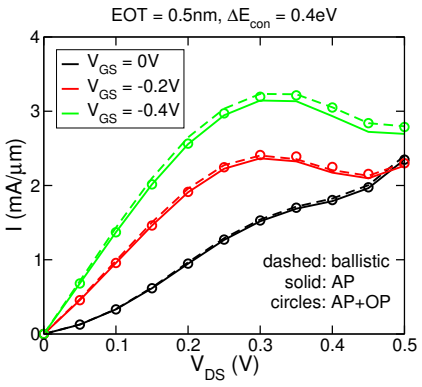

FIG. 6. Normalized output characteristics for $V_{\mathrm{GS}} \leq 0$ from NEGF simulations with ballistic transport, with acoustic phonon (AP) scattering, and with both AP and optical phonon (OP) scattering: the effect of phonon scattering is almost negligible.

Drain-Induced-Barrier Lowering and Subthreshold Swing Fluctuations in 16-nm-Gate Bulk FinFET Devices Induced by Random Discrete Dopants

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Management of process variation and random fluctuation is one of severe challenges in scaling down silicon-based devices continuously according to Moore's law. Emerging fluctuation sources [1-3] consists of the most critical random dopant fluctuation (RDF) which degrade device characteristic significantly. Unfortunately, recent studies on RDDs were reported for SOI FinFETs [1,5,8]. In this work, we for the first time statistically study characteristic fluctuation of 16-nm-gate high-κ/metal gate (HKMG) bulk FinFETs with different aspect ratios (AR = 1 and 2; AR = H_{fin}/W_{fin}) by random-discrete-dopants (RDDs) inside silicon fin channel, based upon our recent simulation studies [1-2,4-7]. Randomly generated devices with three-dimensional (3D) RDDs inside device channel is incorporated into quantum-mechanically corrected 3D device simulation. We compared the DC characteristics for planar and bulk FinFET devices. For the N-type bulk FinFET with AR = 2, it has higher I_{on} and lower I_{off}, further more the fluctuation of I_{on} and I_{off} are both smaller than the results of planar one, and the fluctuation of threshold voltage (σV_{th}) is 46.2 mV for the simulated N-MOSFETs which is significantly reduced to 22.9 mV for the bulk FinFET with AR = 2. We also discuss drain induced barrier lowering (DIBL) and subthreshold swing (S.S) for all devices, and the AR2 FinFET possesses the best performance no matter for the DIBL or S.S effects. There is 68.7% improvement on DIBL and 30.1% improvement on S.S from the planar [1,5,7-8] to AR2 FinFET. The findings of this study indicate that there is a relation between DIBL and RDD's position in which they are near or away from the silicon fin channel surface. It explains the different fluctuation magnitudes of the degraded DIBL effect on devices with the same number of RDDs.

To assess the most critical impact of RDDs on device's DIBL and S.S characteristics, the studied devices are assumed to have the same channel length and device width of 16 nm and all devices' V_{th} (Planar MOSFET, AR1, and AR2 FinFETs) are experimentally calibrated to 250 mV [1] for low power applications. Fig. 1(a) is a 3D illustration of 16-nm-gate bulk FinFET with RDDs inside the silicon fin channel (blue dots are discrete dopants) and an experimentally validated average concentration of $1.5\text{x}10^{18}$ cm^{-3} is studied as shown in Fig. 1(b). The size of each sub-cube is $(16\text{ nm})^3$ for AR1 FinFET and (16 nm x 16 nm x 32 nm) for AR2 device. Total random generated fin channels are then mapped into device's 3D channel for RDDs position/number-sensitive device simulation, where the device parameters are listed in Fig. 1(c). Fig. 1(d) is the RDDs-induced DC characteristic fluctuation between planar MOSFET and bulk FinFET with AR = 2; Fig. 1(d') is the I_d-V_g characteristic, where the red solid lines are the nominal cases and the dashed lines are fluctuated cases. Figs. 1(d'')-(d''') are normalized σI_{on} and σI_{off} vs. RDDs and Fig. 1(d'''') is the σV_{th} as a function of the number of RDDs. The σV_{th} is 46.2 mV for the simulated N-MOSFETs which is significantly reduced to 22.9 mV for the bulk FinFET with AR = 2.

Figures 2(a)-(b) show the DIBL and S.S vs. the number of RDDs and the nominal, averaged, and fluctuated results of DIBL and S.S for the 16-nm-gate planar N-MOSFETs, bulk FinFET with AR = 1, and bulk FinFET with AR = 2, are listed in Fig. 2(c), respectively. The bulk FinFET with AR = 2 has 68.7% improvement of DIBL's fluctuation and 30.1% improvement of S.S' fluctuation, compared with the result of the planar devices. To further examine the RDDs' effect on DIBL and S.S fluctuations, as shown in Fig. 3 for the bulk FinFET with AR = 2, we explore the fluctuated surface potentials for the corresponding random position effects of RDDs on DIBL's fluctuation, as shown in Fig. 3(a). For the case of RDDs away from the channel surface, as shown in Fig. 3(b), the device has relatively smaller fluctuation of DIBL degradation, compared with the case of Fig. 3(f), where the RDDs are near the silicon fin channel surface, for all devices having the same number of RDDs. As shown in Fig. 3(b), the surface potentials are shown in Figs. 3(c) and (d) for AR2 FinFET with V_d=0.8 and 0.05V. The yellow and pale blue cutting lines of Fig. 3(c) and (d) are extracted and compared in Fig. 3(e) along the source to drain. Similarly, Figs. 3(f), (g), (h), and (i) are showed for the case of RDDs near silicon fin channel surface. Compared with the red circle part in Fig. 3(e), there is a higher fluctuation of energy barrier for device with different drain voltage which accounts for the serious DIBL's fluctuation for the case of RDDs near the silicon fin channel surface. This analysis also assesses the RDDs-induced S.S' fluctuation.

In summary, we have estimated the impact of RDDs on the fluctuation of DIBL and S.S of 16-nm-gate planar, AR1 and AR2 FinFETs. AR2 FinFET has best performance of DC characteristic, and suppresses the fluctuation induced by RDDs significantly compared to the planar one including significant improvement for both the fluctuations of DIBL and S.S (68.7% and 30.1%). We are currently estimating the leakage power fluctuations induced by RDDs for the 16-nm-gate bulk FinFET devices.

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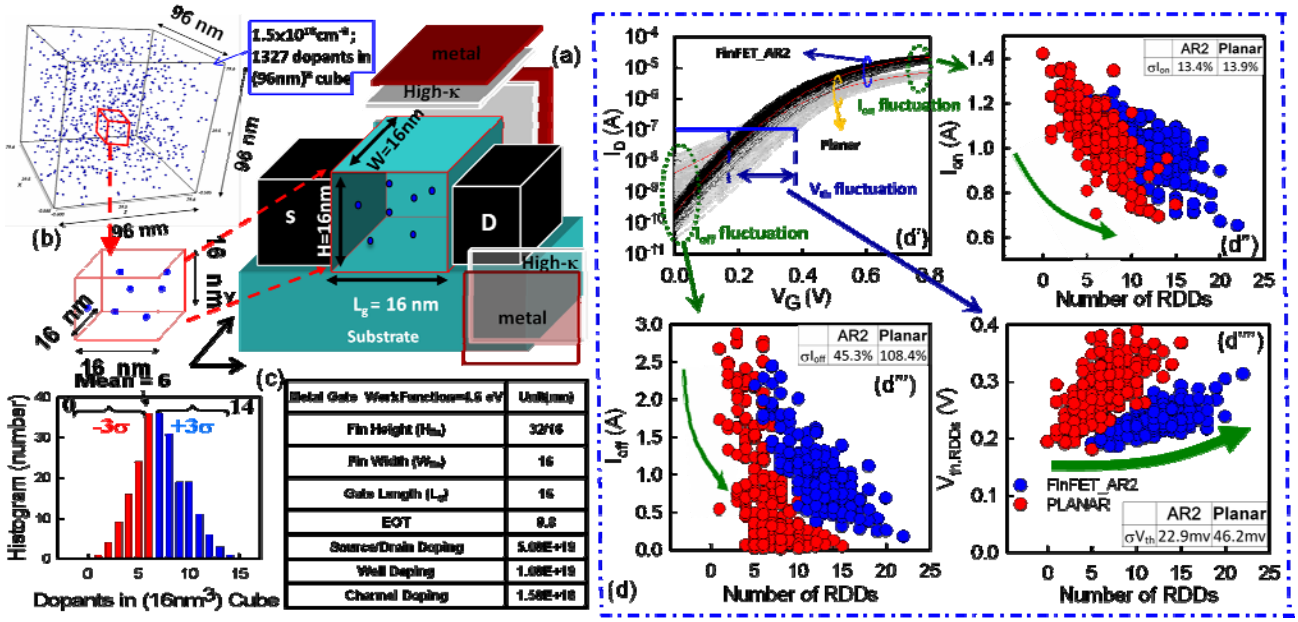
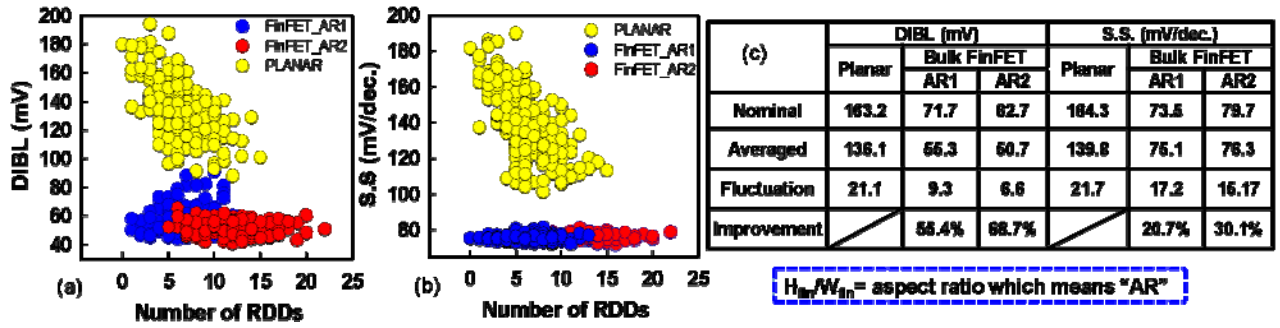


Fig. 1. (a) 3D illustration of 16-nm-gate bulk FinFET with random discrete dopants (RDDs) inside the silicon fin channel (blue dots are discrete dopants). (b) RDDs are distributed in $(96\ nm)^3$ cube with an experimentally validated average concentration of $1.5 \times 10^{18}\ cm^{-3}$. There will be 1327 dopants within the cube and dopants vary from 0 to 14 (the average number is 6) for all 216 sub-cubes. The size of each sub-cube is $(16\ nm)^3$, where aspect ratio AR = H/W = 1 in this plot. The total sub-cubes and sub-planes are then mapped into device's 3D channel for RDDs position/number-sensitive device simulation, where the device parameters are listed in (c). (d) The RDDs-induced DC characteristic fluctuation between planar MOSFET (named as PLANAR) and bulk FinFET with AR = 2 (denoted as FinFET_AR2); (d') I_d-V_g characteristic, where the red solid lines are the nominal cases and the dashed lines are fluctuated cases. (d'')-(d''') are normalized σI_{on} and σI_{off} vs. RDDs and (d'''') is the σV_{th} as a function of the number of RDDs. The σV_{th} is 46.2 mV for the simulated N-MOSFETs which is significantly reduced to 22.9 mV for the bulk FinFET with AR = 2.



(c)	DIBL (mV)			S.S. (mV/dec.)		
	Planar	Bulk FinFET		Planar	Bulk FinFET	
		AR1	AR2		AR1	AR2
Nominal	163.2	71.7	82.7	184.3	73.5	79.7
Averaged	136.1	66.3	60.7	139.8	75.1	76.3
Fluctuation	21.1	9.3	6.6	21.7	17.2	16.17
Improvement		55.4%	68.7%		20.7%	30.1%

Fig. 2. (a) DIBL vs. the number of RDDs. (b) S.S vs. the number of RDDs (c) The nominal, averaged, and fluctuated results of DIBL and S.S for the 16-nm-gate planar N-MOSFETs, bulk FinFET with AR = 1, and bulk FinFET with AR = 2, respectively. The bulk FinFET with AR = 2 has 68.7% improvement of DIBL and 30.1% improvement of S.S, compared with the result of the planar devices.

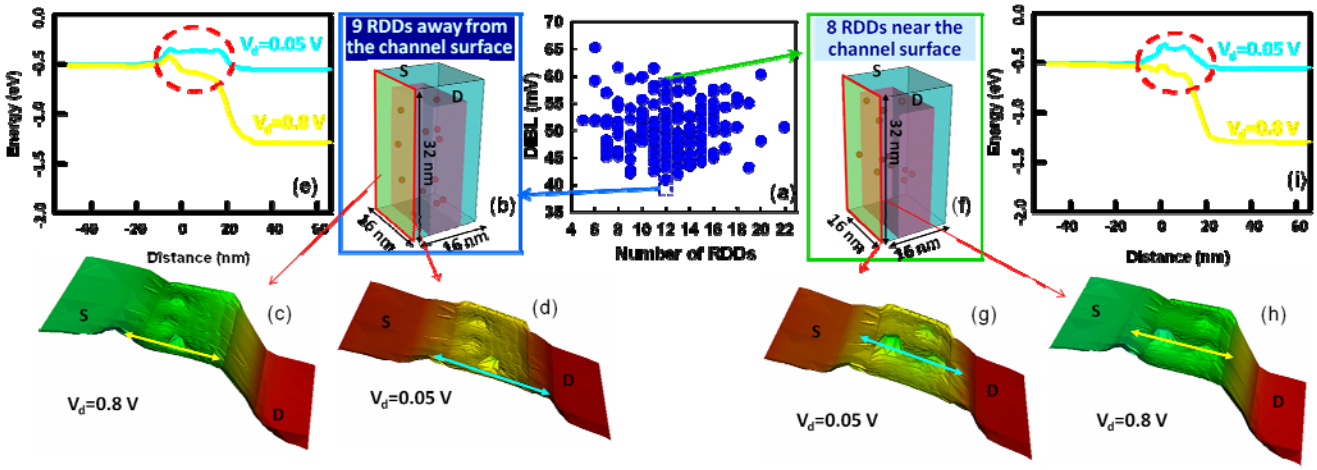


Fig. 3. For the bulk FinFET with AR = 2, we explore the random position effects of RDDs on DIBL's fluctuation. (a) DIBL vs. the number of RDDs. (b) RDDs away from the channel surface which implies the device has relatively smaller fluctuation of DIBL degradation, compared with the case of (f), where the RDDs near the channel surface, for devices having the same number of RDDs. Surface potentials of the plot (b) are shown in (c) and (d) for device with V_d=0.8V and 0.05V. The yellow and pale blue cutting lines of plots (c) and (d) are extracted and compared in (e) from source to drain. Similarly, (f), (g), (h), and (i) are showed for the case of RDDs near silicon fin channel surface. Compared with the red circle part in (e), there is a higher fluctuation of energy gap for device with different drain voltage. That gives the main reason caused serious DIBL's fluctuation for the case of RDDS near channel surface. This analysis can be applied to study the RDDs-induced S.S.

THz Detector Based on Proximity Effect of Topological Insulator

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Designing THz detectors that operate at room temperature is highly desirable and challenging for practical applications, such as imaging and quality control. Since the THz photon energy is very close to the thermal excitation, the room temperature operation is very restricted in conventional devices. In contrast, the topological insulators (TIs), e.g. Bi_2Se_3, pave a way to a new paradigm in low energy optoelectronics due to unique electronic properties of surface electrons. In this work, we analyze THz photodetectors based on the proximity effect in the hybrid TI- ferromagnetic insulator (FMI) structure (Fig.1). The predicted photocurrent of the unit cell can reach the order of 10^{-7}A•cm/W, which is of practical importance. Moreover, the sensitivity of the proposed devices can be extended beyond the thermal limit, since the output signal can be readily distinguishable from the background thermal excitation for signals in THz/far infrared frequency domain even at room temperature.

Fig. 1(left) shows the configuration of bulk TI photodetector and surface state band structure modified by proximity with FMI. The latter brings about time reversal asymmetry in the form of the Dirac cone shift Δk and the asymmetric energy band due to the k^2 term. For the given energy of incident photons, the engineered surface states will lead to imbalance in electron excitation with opposite group velocity, i.e. photocurrent. Fig. 2 shows the calculated characteristics of bulk TI detector at room temperature, assuming 40meV exchange energy between TI and FMI (ref.1). In Fig. 2(left), when the signal frequency increases, the absorbance will gradually reach the upper limit 0.57%, which is one fourth of that in graphene. Fig. 2 (middle) shows the photocurrent, assuming the momentum relaxation time of surface carriers is 1 ps. The maximum density of photocurrent per normalized incident photonic flow achieves 0.15 μA•cm/W. Both the absorbance and the peak of the photocurrent are dependent on the electro-chemical potential, for which the device can be used as frequency-tunable detector. Fig. 2(right) shows the responsivity and absorbance versus electro-chemical potential for signal frequency 36 THz with 10μm device length.

More advantages are expected for a thin TI photodetector (Fig. 1, middle) if electron transitions are allowed between top and bottom surface states. Such scenario can be realistic for 5 or less TI quintuple layers (QL). The attached FMI introduces a spin-independent potential difference (U) between two surfaces, in addition to a displacement Δk of Dirac cone. Fig. 1(right) shows the device schematic for the thin TI detector. The contacts supply the potential measure. Fig. 3 demonstrates the calculated characteristics of a 4 QL TI photodetector, assuming U=0.1 eV. Fig. 3 (left) plots the absorbance versus frequency for different electro-chemical potential. The upper limit absorbance for thin TI is 1.15% as twice as that in the bulk TI, since two surfaces are included. The resonance appears at the signal frequency 17 THz, corresponding to the case shown in Fig. 1(middle). The photocurrent is demonstrated in Fig. 3(middle). The maximum effect is 0.43 μA•cm/W for signal frequency 17 THz. Fig. 3(right) shows the responsivity and absorbance versus electro-chemical potential for signal frequency 36 THz with 10 μm device length.

In summary, compared with the photogalvanic effect in Ref. 2, the proposed TI detectors have photocurrent two orders of magnitude larger if same device area is used, and do not require the circularly polarized light, which could significantly diminish the potential for practical application. Also, the optical excitation and response photocurrent are engineered through the proximity effect by breaking the symmetry of the band structure, so that even at room temperature the output signal is still safely shielded from thermal excitation. In practical use the multilayer structure can be adopted to enhance the light absorption and responsivity. As an example, for signal frequency 36 THz with 10 μm device length, 20 layers of stacked unit cell may easily achieve ~10% absorbance and 8mA/W responsivity.

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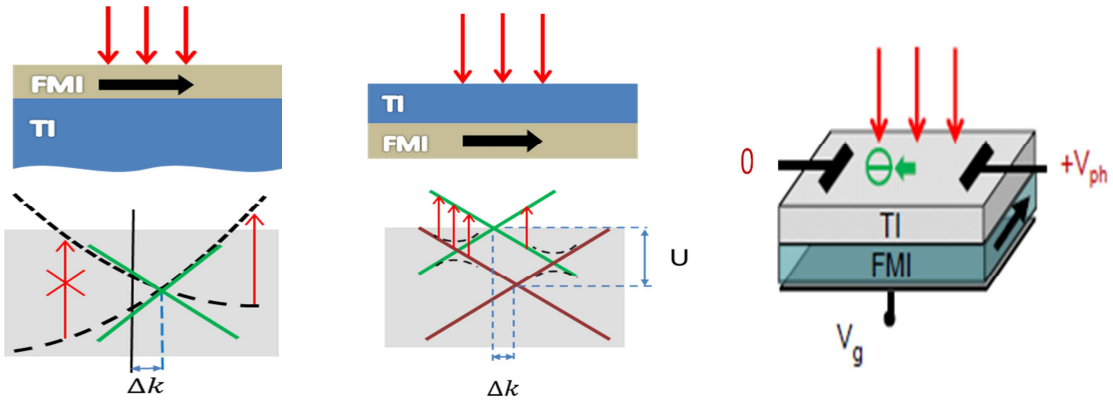

Fig. 1: Configuration of proposed photodetector. Left: bulk TI detector; middle: thin TI detector; right: schematic illustration of the proposed THz detector based on modified TI surface states. The photon signal can be observed by measuring the induced potential difference or the subsequent current.

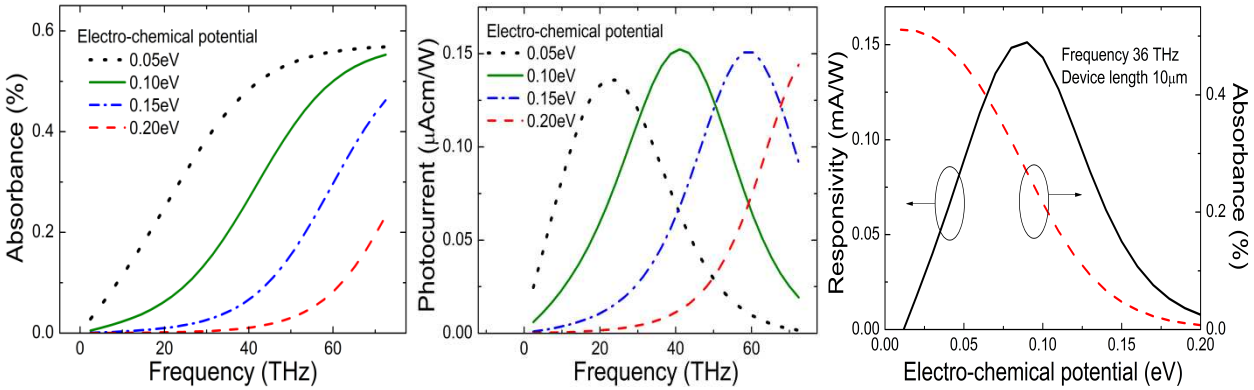

Fig. 2: Bulk TI photodetector performance. Left: absorbance vs. signal frequency; middle: photocurrent vs. signal frequency; right: Responsivity and absorbance vs. Electro-chemical potential at the signal frequency 36 THz, assuming device length 10μm.

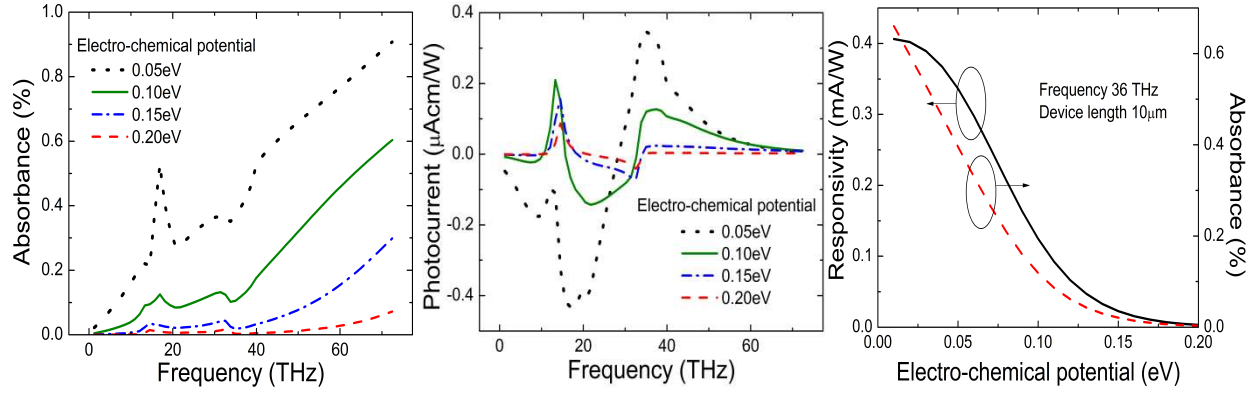

Fig. 3: Thin TI photodetector performance. Left: absorbance vs. signal frequency; middle: photocurrent vs. signal frequency; right: Responsivity and absorbance vs. Electro-chemical potential at the signal frequency 36 THz, assuming device length 10μm.

Transverse-Field Bandgap Modulation on Graphene Nanoribbon Transistors by Double-Self-Aligned Spacers

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Abstract: *Independently-driven tri-gate graphene nanoribbon transistors were implemented by CMOS-compatible double-self-aligned spacer lithography, which effectively suppresses the line edge roughness and width variation. The consistent electrical characteristics show bandgap modulation with transverse electrical fields and ambipolar conduction with perpendicular fields in graphene film.*

Semiconductor industry is facing steep technology scaling challenges due to the fundamental limitation in the subthreshold slope. Therefore, to achieve high-speed electronic switching device with low OFF current, low supply voltage and significant self gain, transistors with new operational principles and scalability below 10nm have been broadly investigated. The transistor based on channel materials with bandgap or bandwidth modulation is one of the alternatives for steeper subthreshold slope. The high carrier mobility and unique symmetric band structures of graphene has already drawn great attention. Recently, tunable bandgap and bandwidth of graphene nanoribbons (GNR) by transverse fields have been predicted theoretically [1,2]. However, experimentally the controllability on GNR width and line edge roughness (LER) remains problematic in top-down lithography approaches.

In this work, we designed a double-self-aligned spacer process for independently driven tri-gate GNR transistors, as depicted in the Fig. 1. Instead of using E-beam lithography, the GNR width is defined by the area clamped by the first two spacers in Fig. 1(a), while side gate separation is determined by the top area of the mushroom-shape silicide spacer in Fig. 1(c). Spacer lithography is CMOS compatible and well developed for FinFET [3]. The spacer width is not limited by the lithography and both width variation and LER of GNR can be prominently reduced, as shown in Figs. 2 and 3, respectively. Through image processing, the pixel intensity distribution and the spatial frequency spectrum are calculated, as shown in Figs. 3(b) and. 4. The double-spacer lithography effectively suppresses the LER by 34% and reduces width variation by 4.4 times, as described in the Table 1. In Fig. 4, the spatial frequency spectrum shows that the line edge of GNR closely follows that of the side gate at low spatial frequency, which corresponds to the long term LER. On the other hand, the signal intensity decreases as the frequency increases, which is the supporting evidence that proposed double-spacer lithography reduces the short-term LER.

To compare our results with previous publications, back-gate biases are swept while both side gates are left floating for the 22nm channel width GNR. The SEM image of channel (the bright dots are etch residuals on GNR) and drain current versus gate bias (I_d-V_{bg}) curves are plotted in Fig. 5. The back-gate GNR transistor with (W/L) = (40nm/15μm) presents a clear ambipolar behavior on monolayer graphene and the Dirac point locates around 1V.

To probe the bandgap modulation properties, the device is operated at the side gate mode, as shown in the Fig. 6. The drain currents show strong dependence on the transverse field. In order to exclude the contribution from electrostatics induced by the side gates, three different biasing strategies are implemented: biasing the side gates differentially such as 2V and −2V (I), grounding one of the side gates while biasing the other (II), and floating one of the side gates while biasing the other (III). These can be interpreted as pure bandgap modulation (I), bandgap modulaton plus electrostatics (II), and pure electrostatics (III), respectively. Subtracting the values of curve III from that of curve II will match closely to curve I, which validates the bandgap modulation from transverse fields. Figure 7 shows the increasing bandgap narrowing on increasing transverse fields on three different devices, which can be fitted to the following relation:

$$\Delta E_g = 3.8 \times 10^{-4} eV \times \exp\left(\frac{F_{tranverse}}{6.3 \times 10^{-3} V/nm}\right)$$

We also found the ambipolar behavior of bilayer GNR in one of the devices under the independently driven tri-gate operation, as shown in Fig. 8. Minor bandgap modulation (about 1.5meV at $F_{transverse}$ = 0.01 V/nm) was observed, which is comparable to the normal field modulation on bilayer bandgap [4]. This may be useful as the bandgap opening in bilayer transistors can be obtained from stacking faults instead of quantum confinement.

Acknowledgement: We thank Si Ping Wang for help with CVD graphene preparation. This work is supported by AFOSR-MURI award. The device fabrication was performed at CNF.

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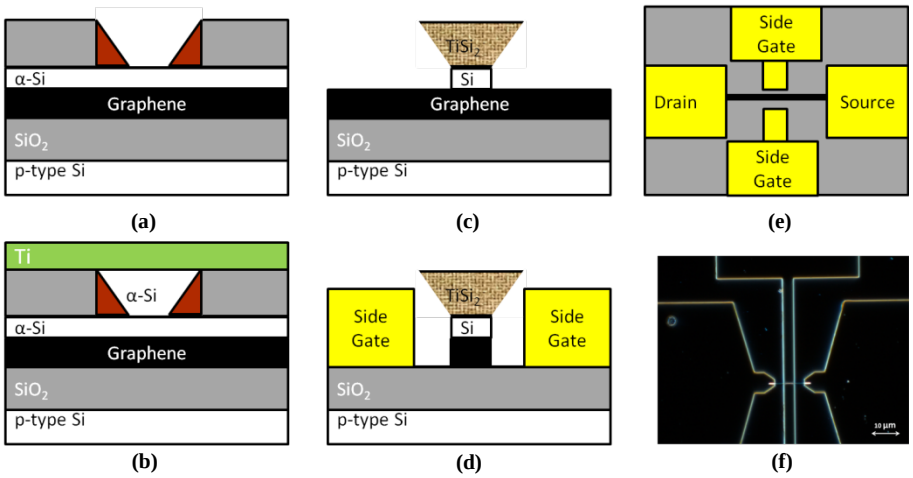


Fig.1.Process flow for double-self-aligned spacer tri-gate GNR transistors: (a) spacer formation on the sidewall, (b) polishing back the α-Si and depositing titanium for following silicidation, (c) etching the SiO_2 and double spacer, (d) side gate formation, (e) top view of device after putting metal contact and (f) dark field image on the top of device.

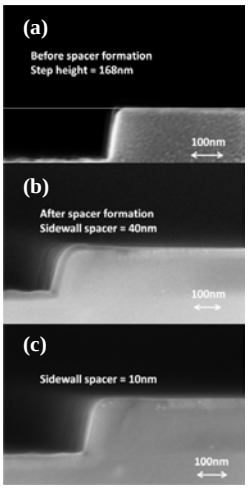


Fig.2. SEM cross section images of the first spacer in Fig. 1(a).

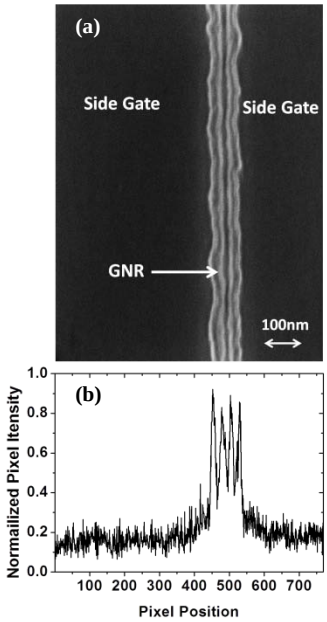


Fig.3. (a) SEM top view images of GNR and side gates and (b) pixel intensity distribution.

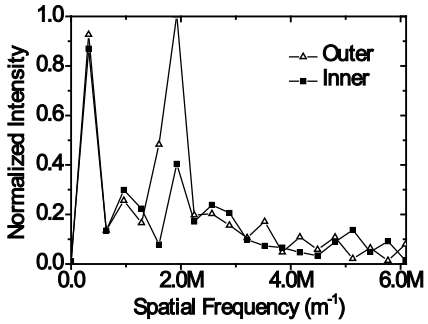
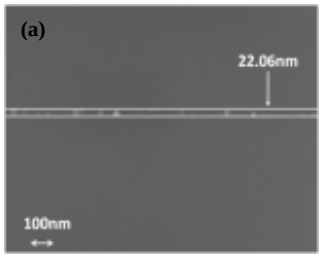


Fig.4. Spatial frequency versus intensity extracted by image processing.

Table.1

	Average Width	Standard Deviation of Width	Line Edge Roughness
Side Gate	227.3nm	15.8nm	43.8nm
GNR	46.4nm	3.6nm	28.8nm



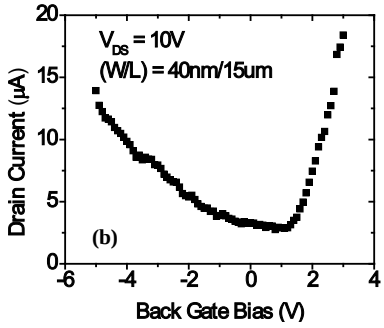


Fig.5. (a) SEM top view images of GNR and (b) I_d-V_{bg} curves of tri-gate GNR transistor.

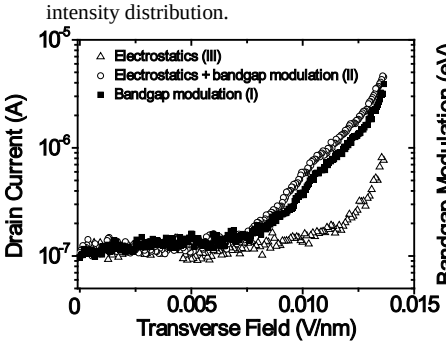


Fig.6. I_d-V_{sg} curves of independently driven tri-gate transistors operated at the side gate mode.

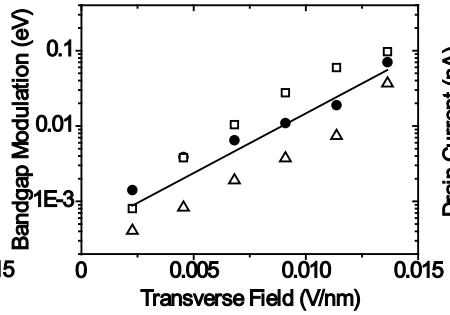


Fig.7. Bandgap modulation versus transverse fields extracted from curve I in Fig. 6.

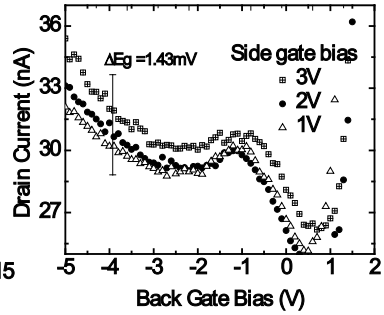


Fig.8. I_d-V_{bg} curves of independently driven tri-gate GNR transistors on a bi-layer.

Epitaxial Si Punch-Through based Selector for Bipolar RRAM

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Resistive RAM is a very promising candidate for high density non-volatile memory. Although bipolar operation has been shown to work at lower current (essential for low power, mobile computing) [1], a suitable selector device that delivers high current density and high on/off current ratio is challenging [2-4]. We demonstrate a $4F^2$ bipolar selector device based on the punch-through mechanism. An npn vertical junction device fabricated using in-situ doped epitaxial silicon is presented. Superior on-current density (J_{on}=1MA/cm^2) and high on-off current ratio (I_{on}/I_{off}) of 300-5000 is experimentally demonstrated. TCAD simulations based performance, variability and scalability are presented.

In a large array implementation of RRAM, a V/3 scheme maybe used to "write" memory cells as shown in Fig. 1 where unselected cross-points have an inadvertent "V/3" bias when a "V" bias is applied to a selected cross point. To cut-off leakage current at these cross-points, a selector maybe placed in series with the memory element. For a bipolar memory device, a device with a symmetric IV is preferred. Fig. 2 shows the SIMS data of the Si:C epitaxial n+/p/n+ layers where l_p is length of p-layer and N_A and N_D are p and n+ layer doping respectively. C is added to limit dopant-diffusion and ensure sharp dopant profiles. This wafer is patterned into vertical diodes of circular footprint by a process flow and cross-sectional schematic shown in Fig. 3. To evaluate the performance of these diodes, the experimental IV of 300nm diameter diode is shown in Fig. 4. A small area diode is necessary for measurement of high current density as the actual current measurement is limited to ~10mA for current meters/set-up. Based on the V/3 scheme, on-current density of 1MA/cm^2 is measured on both polarities while the on-off current ratio is 300 in negative and 5000 is positive polarity. Sentaurus^{TM} based TCAD simulations [5] based on doping profile and device structure show reasonable match with experimental IV characteristics. The slight asymmetry is ascribed to the unintentional doping gradients in p-region. Bulk traps (10^{18}/cm^3) are added to match the IV characteristics at low bias (similar to recombination current at low forward bias in pn junction diodes) and at high bias a series resistance (5kOhm) is employed. These are not fundamental limits as epitaxy can be engineered to obtain much lower defects and contact resistances can be improved in poly diode selectors [6]. Fig. 5 compares J_{on} and J_{on}/J_{off} performance of competing 2-terminal selector technologies. Pt/TiO_2/Pt [1] and poly npn diode [2] based selectors suffers from low J_{on} and VO_2 based metal-insulator transition type selector has high J_{on} but poor J_{on}/J_{off} of 50 [3]. In comparison, this work experimentally demonstrates the best simultaneous J_{on} and J_{on}/J_{off} performance.

To evaluate scalability, we derive an constant off-current scaling rule in Fig. 6 by using simple 1D Poisson solution for punch-through [7] assuming that the n+ regions are highly doped (E1) where in the low bias regime, the off-current is V_b potential barrier limited (E2). To maintain constant off-current i.e. a constant V_b for a given applied bias V_a, a $N_A^2 l_p$=constant rule is applied (E4). As N_A is increased, l_p is reduced. This increases the space charge limited current at high bias regime (E4). To demonstrate the extent of Random Dopant Fluctuation (RDF) with higher doping, Table 1 shows the mean (μ) and standard deviation (σ) number of dopant atoms as N_A is increased in a 20nm technology. As N_A is increases σ/μ decreases. To highlight the doping variability effect on performance, 3D TCAD simulations presented at 20nm node without non-ideal series resistance and bulk traps. Fig. 7 shows that IV changes due to 3σ dopant fluctuation about a nominal doping concentration for a 20nm diameter selector diode. In addition to nominal J_{on} (at V_{on}=2.5V) and J_{off} (at V_{off} = V_{on}/3), J_{onmin} and J_{offmax} are important parameters which can be extracted. J_{onmin} defines "writability" i.e. that minimum current density available from the selector (with high confidence 3σ>0.97%). So the RRAM write current must be limited by the available selector on-current. Similarly, J_{offmax} is the maximum off-current density in a distribution of selectors which increases the off-state leakage. The current variability due to RDF is calculated by impedance field method (IFM) [8]. As N_A is increased the I_{on} and I_{on}/I_{off} increases because increasing N_A reduces l_p (Table 2) and thus improve I_{on} based on (E5). At high N_A, I_{on} improvement diminishes because N_A~N_D violates assumption (E1). Consequently, increasing N_D has two effects. Firstly, it improves series resistance which increases J_{on} at low N_A. Secondly, it boosts improvement at higher N_A by increasing the validity of (E1). I_{on}/I_{off} also improves with increasing both N_A and N_D as I_{off} remains roughly constant but I_{on} increases. Variability benefits are seen in Fig 8b where ratio of standard deviation of off-current due to RDF to nominal off-current i.e. $\Delta I_{off}/I_{off}$ decreases from ~45 to ~4.5 (ideally 0 for no fluctuation) for increasing N_A and N_D. Similar $\Delta I_{on}/I_{on}$ reduces from 0.45 to 0.1(ideally 0 for no fluctuation) by increasing N_A and N_D. Note that the 1D analysis in Fig. 6 predicts trends well for the 3D simulations results. Performance and variability are simultaneously improved by high N_A and N_D. In terms of scalability Fig. 9 shows that J_{on} increases with scaling as fringing fields get enhanced. In conclusion, a punch-through based $4F^2$ epitaxial Si selector is experimentally demonstrated with excellent performance. Selector design improvements from both performance and variability perspectives are presented.

The authors wish to acknowledge support of the Department of Information Technology, MCIT and DST, Government of India.

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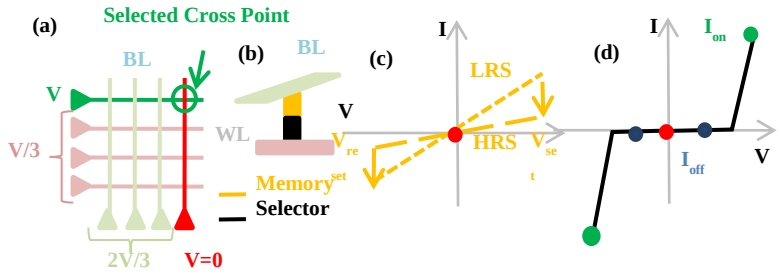

Fig. 1. (a) Schematic of the cross-point architecture using the "V/3 biasing scheme" Selected (green circle) marked. Other cross-points are at V/3 (b) Schematic of a memory and selector circuit in series at each cross-point. IV characteristics of (c) bipolar memory and (d) selector device

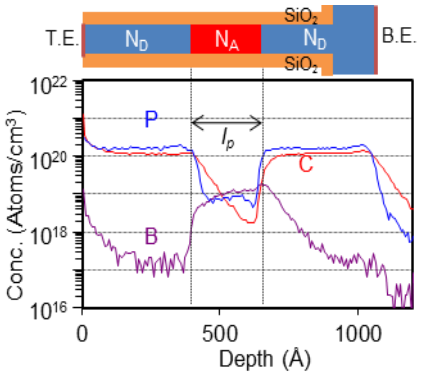

Fig. 2. SIMS of n+/p/n+ stack fabricated by epitaxial Si:C process. l_p is the p-region length and N_A and N_D are n+ and p region doping density respectively.

(a) Process Flow

1. Epi on n-type wafer
2. Active area Litho
3. Si RIE
4. Isolation SiO_2 deposition
5. Via hole etch
6. Contact Pads

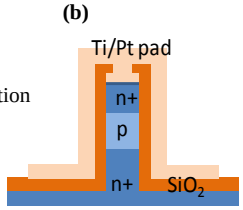

Fig. 3. (a) Process Flow
(b) Schematic of Cross-section

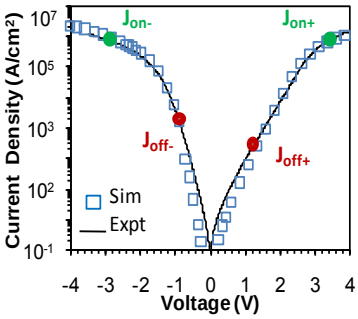

Fig. 4. Experimental and simulated JV characteristics of a 300 nm diameter selector device. J_{on+} = J_{on-} = 1MA/cm^2; J_{on}/J_{off} is 300 in negative polarity and 5000 in positive polarity

Spec	Ref. [2]	Ref. [3]	Ref. [4]	This work
Technology	Pt/TiO_2/Pt	Poly npn	VO_2 Metal Insulator Transition	Epi- npn
Current density (MA/cm²)	10^{-4}	0.02-0.08	1	1
On/Off Ratio	10^4	500-5000	50	300-5000

Table. 1. Comparison of epitaxial Si based punch-through selector with literature [1-3] shows highest J_{on}>1MA/cm^2 with excellent J_{on}/J_{off} ~300-5000 dependent upon polarity

Low bias regime: Barrier limited current

$$N_A << N_D \quad [E1]$$

$$I = I_o \exp\left(\frac{qV_b}{kT}\right) \quad [E2]$$

$$V_b = \frac{(V_a - B)^2}{4B} \quad [E3]$$

$$B = \frac{qN_A l_p^2}{\varepsilon_{Si}} \quad [E4]$$

High bias regime : Space Charge limited current

$$I = \frac{2V\varepsilon_{Si} v_{sat} A}{l_p^2} \quad [E5]$$

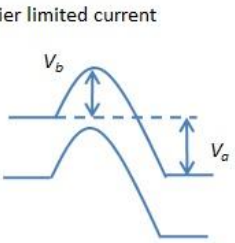

Fig. 6. Under assumption [E1], at low bias regime, if B is kept constant, I_{off} (V_{off}) is constant; N_A can be increased at constant I_{off} [E4]; i.e. l_p should decrease; This should increase high bias regime current which has the form [E5].

Doping (cm^{-3})	l_p (nm)	μ (# of atoms)	σ (# of atoms)	σ/μ
2.5×10^{17}	160	16	4	25%
1×10^{18}	80	32	5.66	18%
4×10^{18}	40	64	8	12.5%
1.6×10^{19}	20	128	11.3	9%

Table 2. Based on $N_A l_p^2$ = constant, increasing N_A reduces l_p. Doping in fully depleted p-region (punch-through condition) is susceptible to RDF. % RDF decreases with increase in N_A.

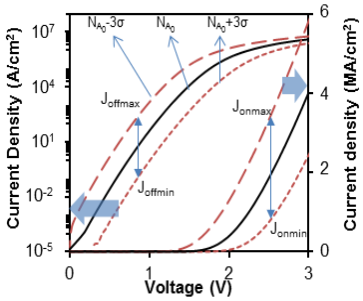

Fig. 7. Doping change by 3σ in "p" region causes a large change in JV (shown in only positive polarity for clarity); J_{onmin} and J_{offmax} are extracted from these JVs at V_{on}=2.5V and V_{off} =V_{on}/3 and compared to nominal J_{on}, J_{off} as metrics of selector variability due to RDF

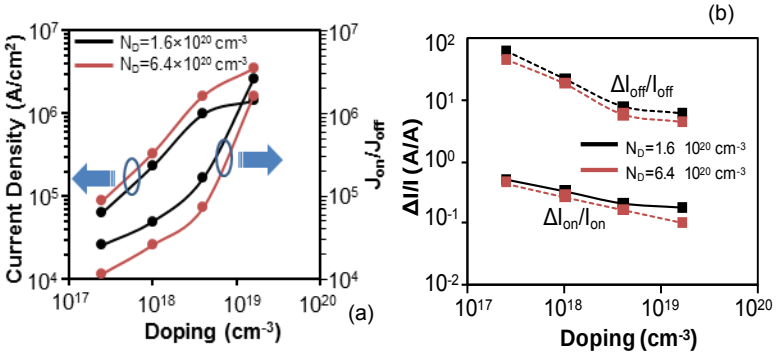

Fig. 8. Effect of N_A and N_D on (a) performance i.e. J_{on} and J_{on}/J_{off} and (b) variability i.e. (i.e. std. deviation/mean of current) are shown for on and off current where. J_{on} and J_{on}/J_{off} increase for higher N_A and N_D. Similarly, $\Delta I_{on}/I_{on}$ decreases to 0.1 and $\Delta I_{off}/I_{off}$ to ~5 (ideally 0 for no variability) for high N_A and N_D. Thus higher N_A and N_D improves performance and variability.

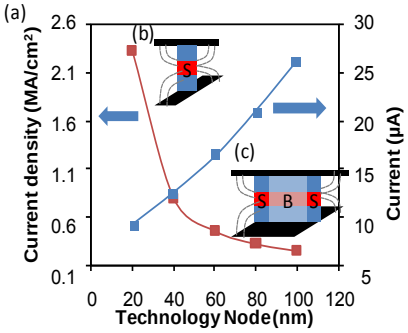

Fig. 9. As the device is scaled the current density increases due to the effect of strong fringing electric field (grey dash) in small area diode (b) which has more surface 'S' compared to larger area diode (c) which has more bulk 'B' that is unaffected by fringing fields. Fringing fields (grey dashed line) cause more electron barrier modulation at the surface and produce higher surface current density compared to bulk.

A Figure of Merit for Oscillator-Based Thin-Film Circuits on Plastic for High-Performance Signaling, Energy Harvesting and Driving of Actuation Circuits

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For even basic sensing and energy-harvesting functions, large-area systems-on-plastic require digital oscillators as a key circuit block [1]. However, their use to generate control signals, or drive actuator/energy-harvesting circuits requires different performance metrics compared to conventional digital circuits. In this abstract we (1) propose a figure of merit for these applications and (2) show experimentally how the dependence of this new metric on the scaling of resistive loads differs from that of the conventional digital circuit metric of power-delay (PD) product [2].

Large output voltage swings are desirable for signal transmission, energy-harvesting or overdriving of a subsequent actuating circuit block. This is in addition to the usual low power and high frequency considerations. Thus we propose the following oscillator design metric: $M_o = (f_{OSC} \times V_{SWING}) / (P_{SUPPLY})$, where f_{OSC} is the oscillator frequency, V_{SWING} is the voltage swing at the oscillator output and P_{SUPPLY} is the power consumption of the oscillator. This metric differs from standard power-delay product analysis ($M_{PD} = f_{OSC}/P_{SUPPLY}$), which simply quantifies the relation between oscillator power consumption and frequency, by now also incorporating a dependence on output voltage swing.

For this analysis, we fabricated 5-stage NMOS ring oscillators based on a-Si TFTs with doped a-Si thin-film integrated pull-up resistors (TFR) on flexible 50µm polyimide (Fig. 1). The TFT channel lengths are 6µm and mobility is 0.7 $cm^2/(Vs)$ (Fig. 2). Resistive load values are chosen as in Fig. 4 to initially maximize the output swing of the oscillator for C_{LOAD}=10pF and are then all scaled by a *resistor scaling factor* (RSF), which is experimentally varied from 0.1 to 5. To enhance the drive capability of a reference (10pF-1nF) capacitive load (C_{LOAD}) whilst minimizing power consumption from the supply (V_{DD}) each inverter stage in the ring oscillator is up-sized from its predecessor by a constant ratio r= 1.6. Fig. 6 illustrates typical oscillation waveforms at the output node of the oscillators as a function of C_{LOAD}. Measured parameters are similar on plastic and glass substrates, and experimental results were validated with a developed Level 61 a-Si TFT SPICE model.

Power consumption scales inversely with stage load resistances (Fig. 7), dominated by on-state static current. For lower power, larger load resistances are required. Frequency is inversely proportional to the signal propagation delay through the oscillator so with fixed W/L ratios for the driver TFTs, frequency scales down with larger loads due to the larger RC time constants from the pull-up paths (Fig. 8). For decreasing output C_{LOAD}, the frequency increases until the 10pF range when the load capacitance becomes comparable with the gate capacitance of the first oscillator stage. Larger resistors limit the critical output swing as the pull-up paths become weaker (Fig. 9), affecting the high output level. This effect is the same as that seen for large capacitances in Fig. 6. Conversely, with smaller loads, the low output level is degraded which also degrades the output swing. Increasing C_{LOAD} also significantly limits the rise time of the output (Fig. 6) which further degrades the voltage swing.

As a constant V_{DD} is used, the conventional PD product should remain fairly constant with load resistor scaling (Fig. 10), but for large load resistors the metric increases due to reduced swings in the oscillator stages and hence weaker pull-down paths. The new metric M_O shows qualitatively similarly behavior for low pull-up resistors, however differs substantially from the inverse power-delay product for large load resistors (large RSF) (Fig. 11). Because of the reduced voltage swing at large resistances (Fig. 9), M_O decreases rather than increases, leading to an optimum load resistor scaling. Maximizing this metric becomes particularly important for C_{LOAD} values comparable to gate capacitances in the oscillator, and an optimum choice of resistor loads is even clearer. A complication not embedded in our metric, however, is that low resistance loads built using the doped TFT a-Si layer, though achievable, require small L/W ratios, so load resistors may significantly dominate the area occupied by the oscillator compared to the driver TFTs.

In conclusion, a design metric for TFT digital oscillators used to drive actuator/sensor/power loads which require large voltage swings has been defined. The optimum load resistance for this metric is different from that for the power-delay product due to reduced voltage swings for large and small load resistive loads.

[1] Liechao Huang, Warren Rieutort-Louis, Yingzhe Hu, Josue Sanz-Robinson, Sigurd Wagner, James C. Sturm, Naveen Verma, "Integrated All-silicon Thin-film Power Electronics on Flexible Sheets For Ubiquitous Wireless Charging Stations based on Solar-energy Harvesting," 2012 Symposium on VLSI Circuits (Submitted)
[2] D.B. Thomasson, H. Klauk, D. Gundlach, T. N. Jackson, "Integrated a-Si:H/pentacene inorganic/organic complementary circuits," IEDM '98 Technical Digest., pp.249-252.

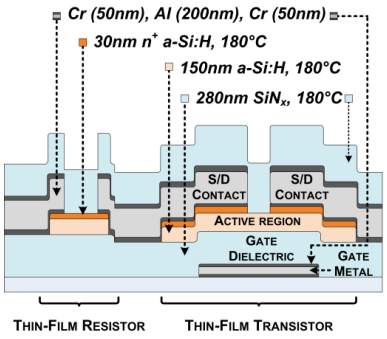


Fig. 1: Schematic cross-section of thin-film devices

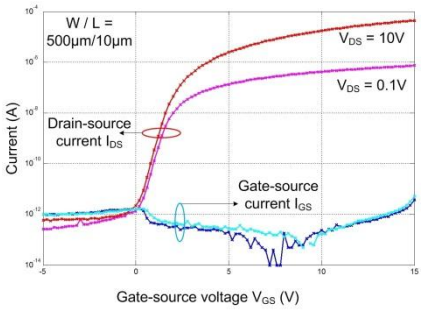


Fig. 2: I-V characteristic of a-Si TFT on 50µm polyimide

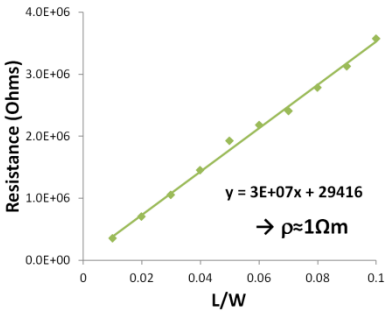
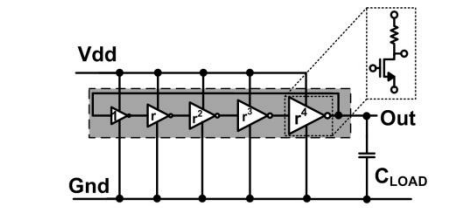


Fig. 3: Resistance characteristics of n-doped a-Si resistors (L=20µm)



Stage	1	2	3	4	5
TFT W/L (µm)	600/6	960/6	1540/6	2460/6	3940/6
Load Res. (MΩ)	10xRSF	6.3xRSF	3.9xRSF	2.4xRSF	1.5xRSF

Fig. 4: Ring oscillator TFT and TFR circuit

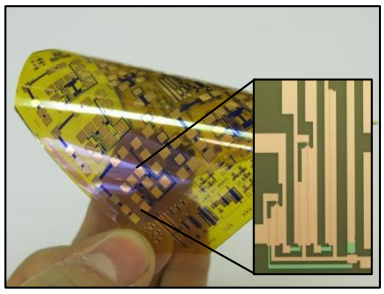


Fig. 5: Flexible oscillator test sample; inset shows ring oscillator TFTs

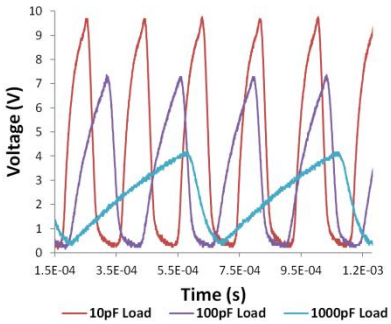


Fig. 6: Ring oscillator waveforms for different output loads (RSF=1)

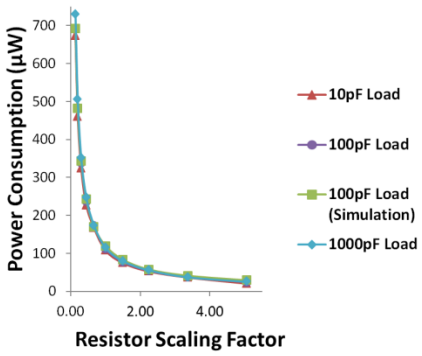


Fig. 7: Load scaling effect: *power*

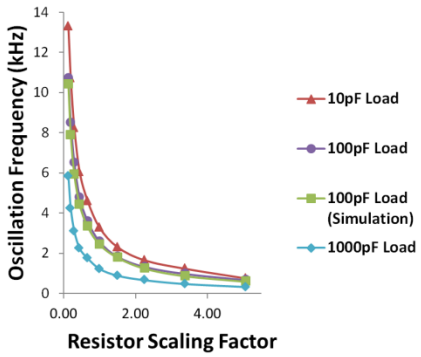


Fig. 8: Load scaling effect: *frequency*

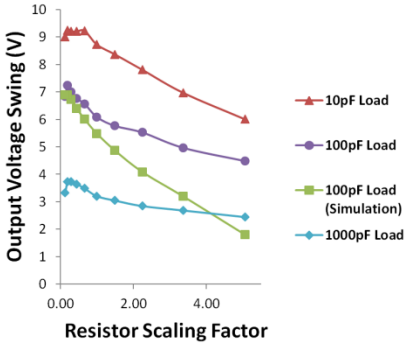


Fig. 9: Load scaling effect: *output swing*

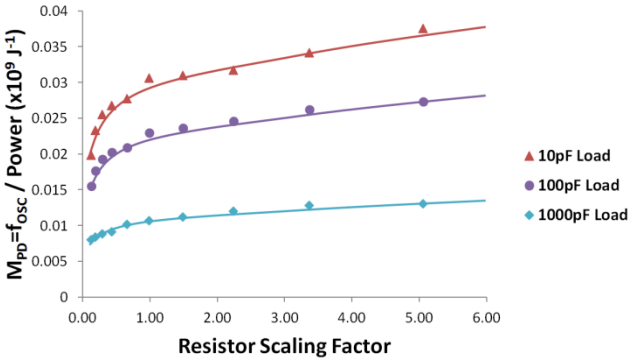


Fig. 10: Optimization of load parameters with (inverse) of conventional power-delay metric M_{PD}

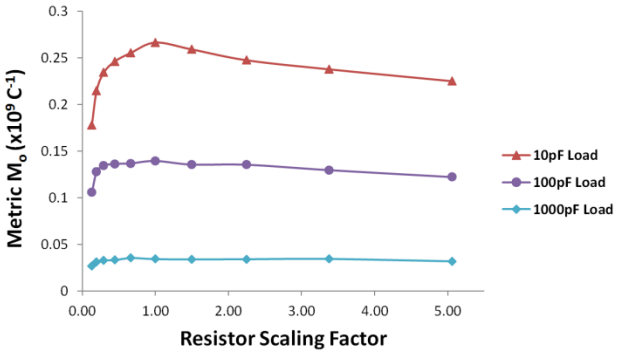


Fig. 11: Optimization of load parameters given proposed metric: $M_o = (f_{OSC} \times V_{SWING}) / (P_{SUPPLY})$

Short-Channel Enhancement-mode Planar GaAs Nanowire HEMTs through a Bottom-up method

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Bottom-up self-assembled planar nanowires (NWs) are of great interest for device application because they can be readily integrated using conventional processing technique. Planar GaAs NWs have been demonstrated to have great crystal quality (free from top-down dry etching damages) and high electron mobility. Considering NWs' 3D geometry, planar NW-FETs inherently benefit from the enhanced electron confinement and electrostatic gate control which are essential to suppress short channel effects and enable the down-scaling of modern transistors. We had fabricated multiple channel planar NW high electron mobility transistors (NW-HEMTs) with self-aligned intrinsic planar <110> GaAs NWs capped with Si doped $Al_xGa_{1-x}As$ thin film as the channel on semi-insulating (100) GaAs substrates and demonstrated the feasibility of wafer-scale electrical uniformity of bottom-up NW-FETs previously [1-4]. However, these prototype multiple channel planar NW-HEMTs were of 1.2μm gate length and ~250nm NW diameter in the channel.

To improve planar NW-HEMT performance, it is imperative to scale both the size of NWs and gate length. It is well-known that VLS grown NWs' size is determined by the size of Au seeds. However, scaling planar NWs purely by using Au seeds of smaller size were not successful due to more severe effect of parasitic NW sidewall deposition during VLS growth. We finally succeeded in growing high quality sub-100nm planar GaAs NWs using a two-temperature-stage growth. Basically, we start the planar NW growth at higher temperature to ensure high planar NW yield and then drop the growth temperature to a lower value to ensure planar NW quality. Figure 1 shows planar NWs grown from 100nm and 250 nm Au seeds in the inset and main frame at the same magnification (scale bar), respectively. Both sets of planar NWs are of great quality and with clear smooth top (100) and side (111A) facets developed.

Complete planar NW-HEMT structure was formed in one single epitaxial growth. After 100nm Au seeds dispersion, an intrinsic 150nm thick $Al_{0.33}Ga_{0.67}As$ back barrier was grown at 680°C temperature in order to improve carrier confinement. Au seeds under such growth condition simply elevated to the top surface and no NW growth took place. Then the reactor condition was adjusted to grow for 2 mins yielding 15μm long planar NWs via the Au-catalyzed vapor-solid-liquid mechanism. Finally, we switched back to thin film growth mode and grew 3nm thick intrinsic $Al_{0.33}Ga_{0.67}As$ spacer followed by 42nm Si-doped ($2\cdot10^{18}$ cm^{-3}) $Al_{0.33}Ga_{0.67}As$ and 30nm n^+ GaAs contact cap. Figure 2 shows the output characteristics of a single NW long channel (L_{ch}=1.2μm, source to drain = 5 μm) HEMT. Figure 3 plots the transfer characteristics of the same device scaled by W = 280nm (the total width of NW top and side facets). Note the threshold voltage of this device is 0.02V which does not match the $Al_{0.33}Ga_{0.67}As$ carrier supply layer growth parameter because of different thin film deposition rate thus thickness on different facets. This can be seen clearly in Figure 4 which shows a planar NW-HEMT cross-section with a 75nm Au nanoparticle seeded planar NW in channel. For these sub-100nm planar NW-HEMT structure, we fabricated short channel devices (L_{ch} = 120nm, source to drain = 3 μm) in order to demonstrate the advantages of our NW-HEMTs due to 3D carrier confinement and better gate control. The top view of a short channel NW-HEMT is shown in Figure 5. Figure 6 shows the output characteristics. Figure 7 plots the transfer characteristics in log scale from which we extract the I_{on}/I_{off} ratio ~10^4, SS = 160mV/dec and DIBL = 120mV/V. Figure 8 gives the scaled extrinsic G_m and drive current plots using W = 145nm at 1V drain bias. The peak extrinsic G_m is 500μS/μm and peak drive current is 384μA/μm, which are excellent values for AlGaAs/ GaAs HEMT system and even comparable to advanced InAlAs/ InGaAs HEMT system. Through more carrier-transfer efficient delta doping, uniform and thinner AlGaAs carrier supply layer, optimized back barrier with delta doping and smaller mesa isolation (rather than 20μm mesa for this prototype device), we are optimistic that our bottom-up grown planar NW-HEMTs can surpass its planar counterpart.

[1] Seth A. Fortuna and Xiuling Li, *IEEE Elec. Dev. Lett.* **6**, 593-595 (2009).

[2] Xin Miao and Xiuling Li, *IEEE DRC Digest,* 115-116 (2011).

[3] Xin Miao and Xiuling Li, *IEEE Elec. Dev. Lett.* **9**, 1227-1229 (2011).

[4] Seth A. Fortuna et al., *Nano Lett.* **8**, 4421-4427(2008).

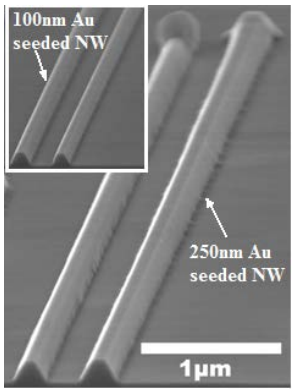

Fig. 1 Comparison between 250nm and 100nm Au seeded NWs

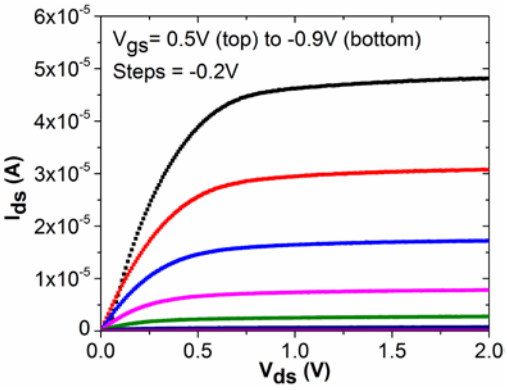

Fig. 2 Output characteristics of Long channel NW-HEMT

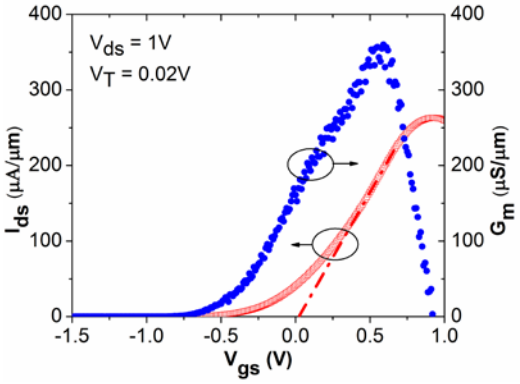

Fig. 3 Scaled transfer characteristics of Long channel NW-HEMT

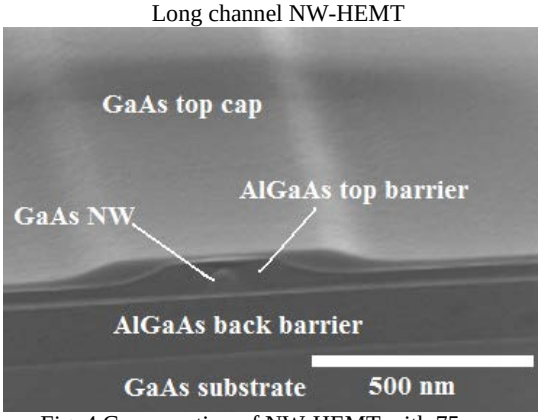

Fig. 4 Cross-section of NW-HEMT with 75nm Au seeded planar GaAs NW in channel

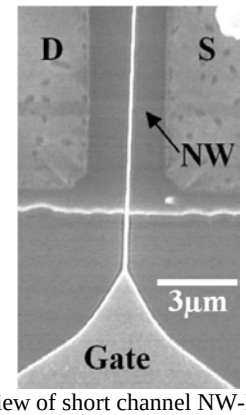

Fig. 5 Top view of short channel NW-HEMT with 120nm gate and 3µm source to drain seperation

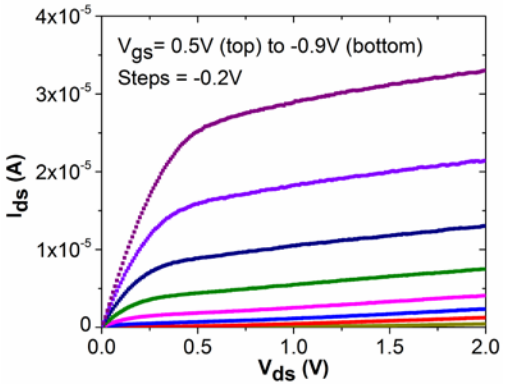

Fig. 6 Output characteristics of short channel NW-HEMT

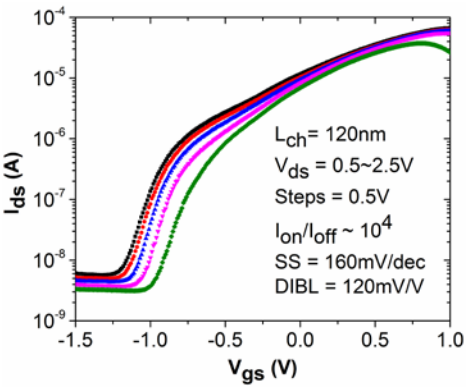

Fig. 7 Transfer characteristics of short channel NW-HEMT in log scale

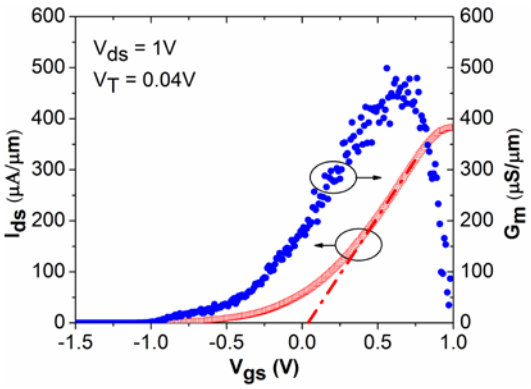

Fig. 8 Scaled G_m and drive current plots of short channel NW-HEMT

Electric Field Driven Domain Wall Transfer in Hybrid Structures

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Domain wall (DW) motion devices attracts much interest with their prospective logic and memory applications[1][2]. Present on-chip DW manipulations by a magnetic field of electric currents or electron spin torque raise the problem of high Ohmic energy losses. We show that such a difficulty can be avoided by applying an *exchange field* $\mathbf{H}_{\text{eff}}$ to the magnetic layer from the proximate graphene (Gr), instead of using an actual magnetic field. $\mathbf{H}_{\text{eff}}$ is shown to be dependent on carrier density gradient in Gr, which is easily manipulated with a gate voltage. A novel memory device implementing this concept is designed and modeled, demonstrating switching power well below femto-Joule while maintaining a switch time within 2 nanoseconds.

The quantitative analysis is based on a mean field approximation of the exchange energy between Gr electrons and the adjacent ferromagnetic insulator (FMI) layer with a 180° DW. In-plane variation of electrical potential generates electron density distribution (Fig.1) that pushes DW into the area with lowest local carrier concentration according to the linear dispersion relation in Gr. If a linear doping gradient is assumed to exist in Gr, the corresponding $\mathbf{H}_{\text{eff}}$ is shown in Fig. 3; the bias shifted fields drive the DW between the two stable points A and B where $\mathbf{H}_{\text{eff}}$ is neutralized by coercivity.

This analysis suggests the device prototype as shown in Fig.2, where two nanowire gates control the potential gradient electrostatically through a high dielectric insulator layer. Fig. 4 shows the typical $\mathbf{H}_{\text{eff}}$ profile with different dielectric layer thickness and dielectric constants; Fig. 6 indicates the minimum field at the middle of the two gates for different structural and operating conditions. Theoretical analysis of the DW dynamics was carried out by solving Landau-Lifshits-Gilbert equation adapted to dynamics of DW location (Fig. 5, insert). These results are supported by the numerical simulation of DW propagation with the Nmag software[3] (Figs 5, 8) which considers the interaction as an additional surface anisotropy term. These results confirm that the DW moves over 40 nm in 1~2 ns.

Additionally, longer-range DW transfers are feasibly achievable by cascading the unit structures (Fig. 7) and successively applying bias to gate 1 and 3, gate 2 and 4, etc. As the voltage is tuned to move the DW between the two active gates, individual control of DW inside each unit is possible. This also enables multi-DW control along the FMI stripline for memory and logic applications.

In conclusion, we proved for the first time the feasibility of the DW motion control by electric field using the exchange interaction between Gr electrons and the FMI layer. A device prototype is designed and modeled. It is shown an effective magnetic field at 10~100 Oe is generated upon the DW, which leads to a velocity around 30 m/s. 0.5~1 GHz operating frequency is expected in this condition as a bi-state memory. No active current is present and the equivalent circuit model is a set of capacitors. Therefore, low energy consumption is achieved, about 10^{-16} J/switch.

[1] S.S.P. Parkin, M. Hayashi, and L. Thomas, *Science* 320, 190 (2008).
[2] D.A. Allwood, et al, *Science* 309, 1688 (2005).
[3] Fischbacher et al, EEE Transactions on Magnetics, 43, 6, 2896-2898 (2007)

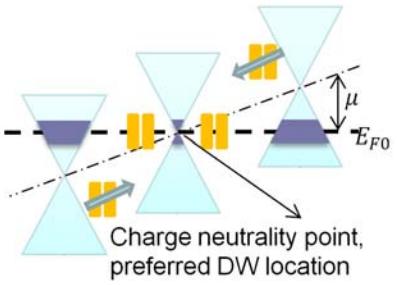

Fig. 1 DW moves towards the neutrality point with the presence of chemical potential gradient in Gr.

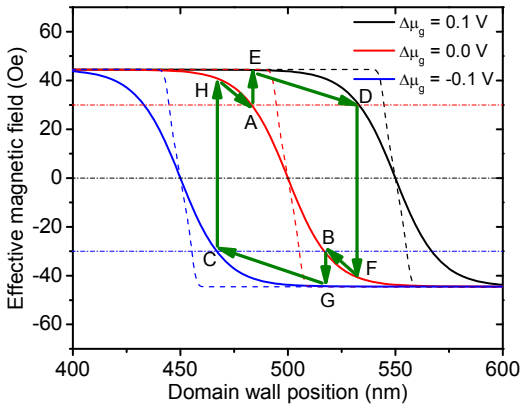

Fig. 3 Effective magnetic field as a function of DW position with a linear chemical potential gradient. The motion of DW is controlled by shifting the profile with gate bias. It follows the loop A-E-D-F-B-G-C-H-A which is determined by the coercivity.

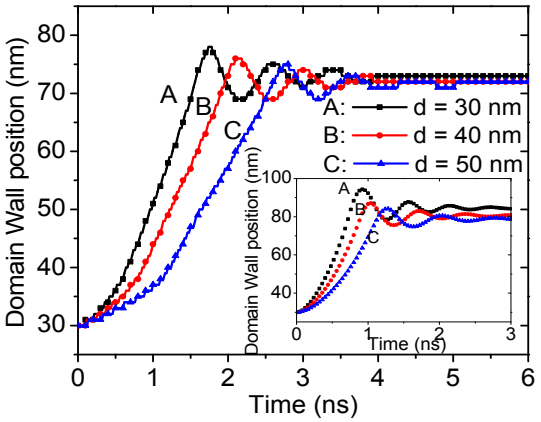

Fig. 5 DW position as a function of time with ±1 V bias from micromagnetic simulation (main figure) and theoretical modeling (inserted).

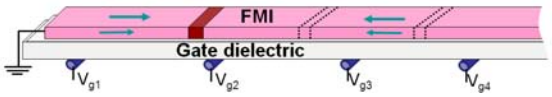

Fig. 7 The cascade structure to realize DW movement over a large range. Successive motion is induced by successively applied bias on gate 1 and 3, gate 2 and 4, etc.

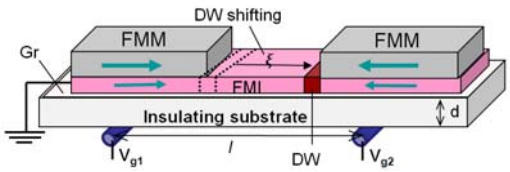

Fig. 2 Structure of the device prototype. Nanowire gates generate the moderate potential gradient.

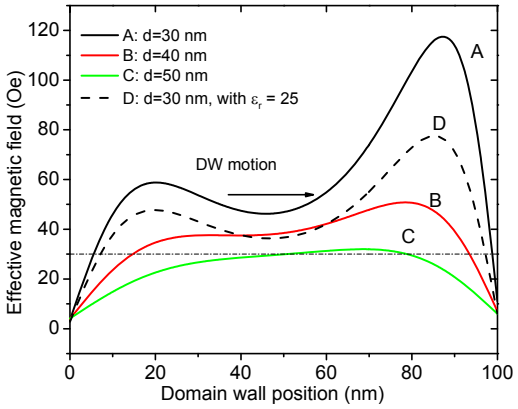

Fig. 4 Effective magnetic field as a function of position for the device prototype with different substrate properties.

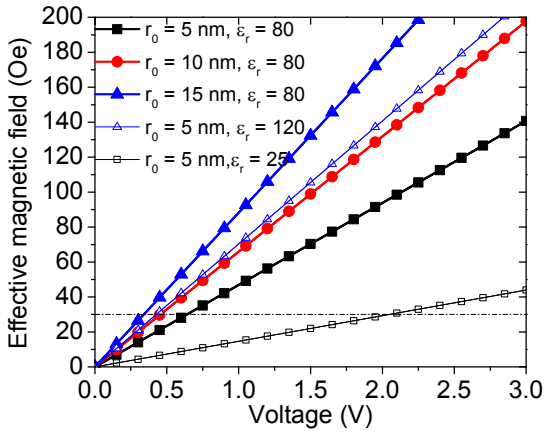

Fig. 6 Effective magnetic field at the middle position for different gate voltages, nanowire gate radius and insulating dielectric constant.

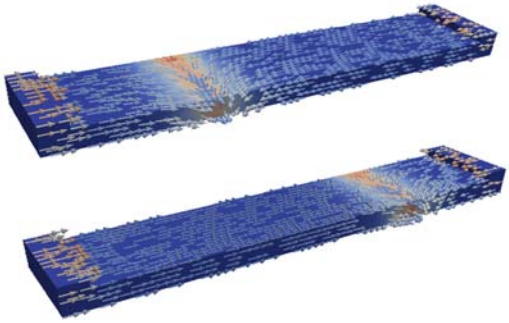

Fig. 8 Simulation of the DW motion with Nmag, colored by the exchange and demagnetization energy densities for the bulk and the arrows respectability.

Comparison of Graphene Nanoribbons With Cu and Al Interconnects

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We present a comparative study of graphene nanoribbon (GNR) interconnects (ICs) with sub-50 nm copper (Cu) and aluminum (Al) ICs. We extend existing models for all materials in order to understand the physical size effects that occur when the electron mean free path (λ_{MFP}) becomes comparable to the IC dimensions. We calibrate such models against the best publicly available data. We find that, depending on geometrical configuration, either Al or GNRs could hold advantages over Cu at linewidths <10 nm.

To treat the resistivity of Al and Cu with line edge roughness (LER), we implement the model of [1] with specularity $p(\theta)=\exp[-(4\pi h/\lambda_F)\cos^2\theta]$, where λ_F is the Fermi wavelength and h is the root-mean-square LER. (We note this represents a more physical approach than previous models which used fitting parameters for specularity p and reflectivity R [2].) We correlate this model with Ref. [2] and obtain specularity values $p_{Cu}=0.4$ and $p_{Al}=0.78$ for metal nanowires with LER. With other parameters in Table 1 and Fig. 1a, we plot the resistivity of sub-50 nm ICs in Fig. 1b. Interestingly, Al could suffer from less resistivity increase than Cu in scaled ICs due to a shorter λ_{MFP}, λ_F, and a fixed grain size [3] (see Table 1).

To treat GNR resistivity we utilize the theoretical work of [4] with experimental data of [5]. (This data set is the most comprehensive available, but such GNRs were not optimally doped; to lower resistivity for practical IC applications, graphene could be doped up to ~10^{14} cm^{-2} [6].) For the best fit to the data [5], we re-derive the Fuchs resistivity model [7] in 2-dimensions:

$$\frac{\rho_0}{\rho} = 1 - \left(\frac{2\lambda_{MFP}}{\pi W}\right)\int_0^{\pi} d\theta \sin^2\theta|\cos\theta|\left\{(1-p(\theta)) - \frac{(1-p(\theta))^2\exp\left(-W/\lambda_{MFP}|\cos\theta|\right)}{[1-p(\theta)\exp\left(-W/\lambda_{MFP}|\cos\theta|\right)]}\right\}$$

where ρ_0 is the bulk resistivity, W is the GNR width, and $p(\theta)$ is the angle-dependent specularity [1].

To examine the coupling capacitance of our ICs, we consider two basic horizontal and vertical configurations in Figs. 2a-b using COMSOL Multiphysics. For the vertical configuration, we assume that stacked GNRs can be treated as a single IC of width W. The various dimensions for each configuration are shown in Table 2 and the results of our capacitance calculations are shown in Fig. 3.

To calculate the RC time delay (τ) we multiply the resistance for 500 nm long ICs generated by our models with the capacitance results from COMSOL. The results of the horizontal configuration are shown in Fig. 4a, where the lower delay of Al at 5 nm < W < 20 nm is due to a lower resistivity. Below ~5 nm, GNRs should theoretically offer better performance as coupling capacitance dominates delay in metal ICs. However, the most relevant experimental data currently available [5] suggest that GNRs on SiO_2 could outperform only Cu but not Al below ~6 nm. (However, this observation is subject to change, when more experimental data on highly-doped GNRs becomes available.) The results of the vertical configuration are shown in Fig. 4b, where we find τ increases as $W \rightarrow 0$ nm due to size effects and as $W > 20$ nm due to coupling capacitance. The τ of Cu is superior for intermediate values of W due to a lower bulk resistivity value (Table 1). However, the resistivities of the vertical GNRs are independent of the IC width (LER only on top and bottom), allowing τ to remain lower than that of Cu and Al below ~8 nm.

In conclusion, we developed an updated Sambles-Steinhögl model [1,2] finding that Al may hold advantages over Cu for sub-10 nm ICs due to a shorter electron λ_{MFP} and larger grain size. COMSOL simulations show that horizontal GNRs can reduce coupling capacitance for sub-10 nm dimensions. Depending on horizontal or vertical configuration, RC time delays of Al and GNRs may be lower than those of Cu at linewidths below ~8 nm. This study offers a physical analysis of the scaling of such ICs, and results can be updated as more realistic LER, grain size, and GNR resistivity data become available.

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Table 1. Resistivity Model Parameters

	Aluminum	Copper
$\rho_{bulk,300K}$	2.8 μΩ·cm [8]	2.2 μΩ·cm [9]
λ_{MFP}	19.8 nm [8]	39 nm [9]
P	0.78	0.4
R	0.59 [8]	0.34
d_{Grain}	30 nm [10]	See Fig. 1
λ_F	0.36 nm [11]	0.46 nm [11]

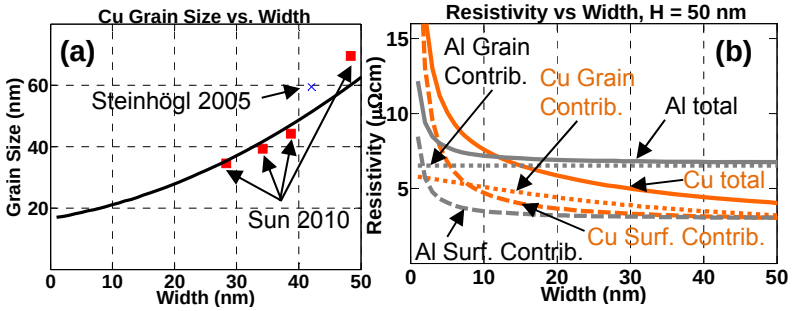

Fig. 1: (a) Copper grain size vs. width. Quadratic fit to data points from [1] and [9]. (b) Resistivity of rectangular Cu and Al nanowires as function of width. *Additional References*: [8] J. Lee et al., *Scripta Mat.* **63**, 1009 (2010). [9] T. Sun et al., *Phys. Rev. B.* **81**, 155454 (2010). [10] Z.N. Farhat et al., *Mat. Sci. and Eng.* **A206**, 302 (1996). [11] T. Kim et al., *Nano Lett.* **10**, 3096 (2010).

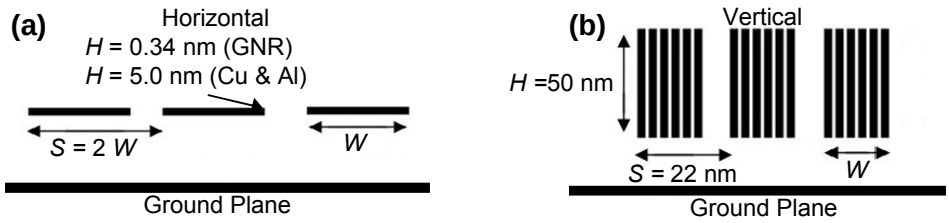

Fig. 2: (a) Horizontally oriented interconnects. (b) Vertically oriented interconnects. Note all GNR sheets in one block are at same potential and no capacitive coupling exists between sheets in one block. We therefore simulate a block with width *W* for the vertically oriented GNR stacks.

Table 2. COMSOL Simulation Parameters

Configuration	Material	Height (H)	Spacing (S)	Dielectric Constant	Ground Plane Distance
Horizontal	GNR	0.3 nm	S=2*W*	2.3 [ITRS 2007]	300 nm
Horizontal	Al, Cu	5 nm	S=2*W*	2.3	300 nm
Vertical	GNR, Al, Cu	50 nm	S=22 nm	2.3	30 nm

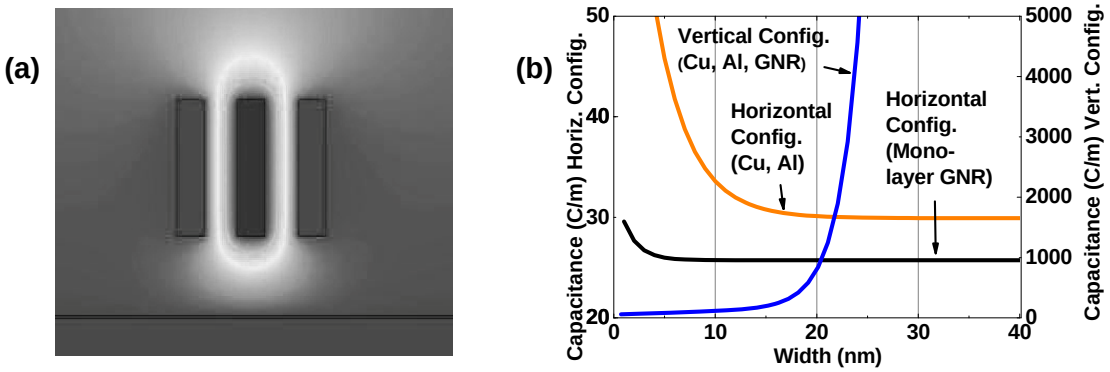

Fig. 3: (a) Resulting fringing field lines from COMSOL simulation for *W* = 10 nm, *H* = 50 nm. (b) Resulting capacitance as a function of width *W* from COMSOL simulations.

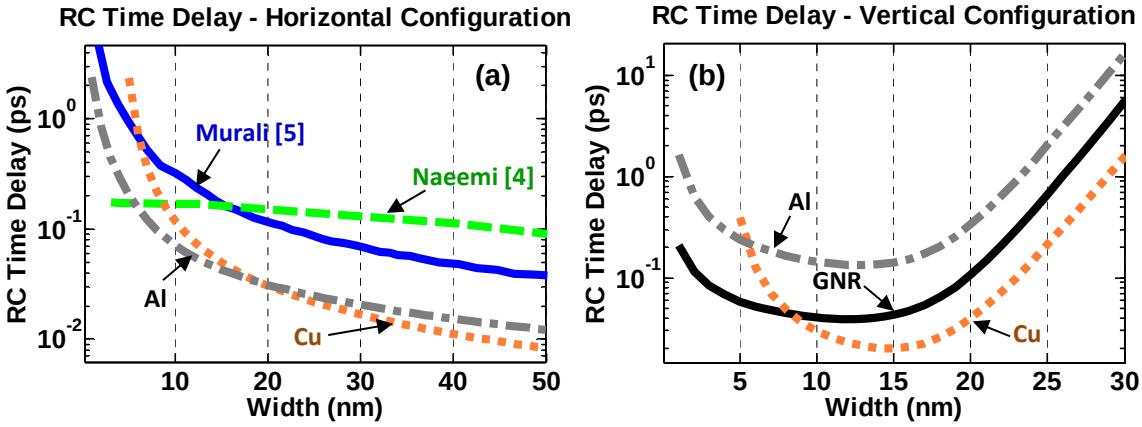

Fig. 4: a) Horizontal configuration. Al could have an advantage at widths < 20 nm due to a lower resistivity. b) Vertical configuration with GNR *S* = 22 nm. Cu is best for intermediate values of *W* due to low bulk resistivity, but GNRs could have lower delay below ~8 nm.

Electrical Control of Nuclear-Spin-Induced Hall Voltage in an Inverted InAs Heterostructure

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We have fabricated a nuclear spin manipulation device by spin injection from ferromagnetic (FM) electrode into an InAs channel and the operation was confirmed by Hall voltage near the FM/semiconductor interface. Injected electron spins are transferred to nuclear spin angular momentum by hyperfine interaction known as Overhauser effect. [1] Previously, it was reported that nuclear spin polarization in semiconductor by edge current in quantum Hall state [2] and nonlocal lateral spin valve configuration. [3] Compared with these samples working only in extreme conditions, we propose a nuclear spin device, which is electrically controllable at room temperature. Spin induced local magnetic field was estimated to be of the order of kGauss, resulting in a few tens of mV range in Hall voltage [4-5]. Electrical manipulation of local nuclear spin angular momentum would provide a new horizon on device applications of spintronics.

The fabricated Hall-bar is shown in Figure 1. It was formed on inverted InAs pseudomorphic HEMT structure grown on InP (001). The channel mobility was 17,000 $cm^2V^{-1}s^{-1}$ and 28,100 $cm^2V^{-1}s^{-1}$ at 300K and 4.2K, respectively. Mesa etching for the device isolation was conducted with conventional electron-beam lithography and wet chemical etching with phosphoric acid based etchant. Current source electrodes consist of ferromagnetic metal and non-ferromagnetic metal. As a ferromagnetic electrode, 15nm Fe was grown by MBE followed by 3nm Au protection layer. The Fe electrode extends across the source edge of the mesa so that the contact from side edge of the mesa staructure is made possible, while drain electrode was stacked from top of mesa or side with Au/Ge/Pd alloys or Pd. This ferromagnetic electrode is designed in such a way that the injected spins are polarized perpendicular to the substrate, whose spin states are transmitted to the nuclear spins near the source edge though Overhauser effect, resulting in perpendicular built-in magnetic field. When the current direction is opposite, spin non-polarized electrons are injected from non-ferromagnetic electrode, resulting in disappearance of the local magnetic field.

Hall effect measurement was conducted by running constant current from the FM terminal (electrons are injected from the non-FM terminal) under external magnetic field (Fig. 5). Then, Fe electrode was magnetized in-plane, parallel to the current direction and the steady spin current is supplied from the ferromagnetic electrode without external magnetic field so that the out-of-plane magnetization at the edge of the mesa step as shown in Fig. 4 and Fig.7. Then, Hall measurement was carried out in zero external magnetic field in two current directions. Substantial Hall voltage was observed as shown in Fig. 6 (solid curve) in the case of electron injection from ferromagnet and much reduced negative Hall voltage was observed (green) in the case of opposite current direction. The Hall voltage difference is too large to explain with the lithography pattern size variations between the relative Hall terminals. Possible explanation is nuclear magnetization near the spin injection edge (source) through spin exchange process between electron spin and the nuclear spin (mostly contribution from indium atoms). Spin injection from Fe into InAs channel was verified in the separate device as shown in Fig.3. The local magnetic field was calculated to be 0.2T(Fig.6) and 0.35T (Fig.8, Hall terminal at 2μm) and 1T(Fig.8, Hall terminal at 3μm) by comparing Hall voltage with Hall measurement results (Fig.5). In order to verify the spin transfer effect, spin non-polarized current was injected in the same sample. The dotted curves in Fig.6 and Fig.8 clearly show that the zero-field Hall voltage has disappeared. The reason why the dotted curve in Fig 6 did not completely disappear is not clear at the moment and finite Hall voltage increase in the current range of $I > 4\mu A$ in the terminal of 3μm distance from source edge needs to be explained with more investigation. It is evident that substantial Hall voltage can be generated by injecting spin polarized electrons near the injection interface and spin non-polarized electron injection can erase the Hall voltage. The distant Hall terminal, which was 8μm away, showed no Hall voltage, whereas terminals at 2μm and 3μm showed substantial voltage. The magnetic moment of the 30% of nuclear spin polarization near the FM terminal matches well with the local magnetic field estimated by (zero-field) Hall voltage and conventional Hall measurements (Fig.5). All these results suggest that these phenomena is caused by spin transfer to the nuclear spin near the ferromagnet/semiconductor interface. To our knowledge, this is the first result of electrical manipulation of nuclear spins and local magnetic field. This result may open up a new horizon of spintronics in ferromagnetic metal/semiconductor hybrid systems.

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[4] D. Paget et al, Phys. Rev. B 15 (1977) 5780.
[5] F. H. L. Koppens et al, Science 309 (2005) 1346.

InGaAs	10nm
$In_{0.52}Al_{0.48}As$	50nm
$In_{0.53}Ga_{0.47}As$	1.8nm
InAs	4.1nm
$In_{0.53}Ga_{0.47}As$	5.6nm
$In_{0.52}Al_{0.48}As$	50nm
Si δ-doping	$1.2 \times 10^{12}cm^{-2}$
$In_{0.52}Al_{0.48}As$	0.8μm
InP (100) substrate	

Fig. 1

Fig. 1. InAs HEMT (high electron mobility transistor) grown on InP (100).

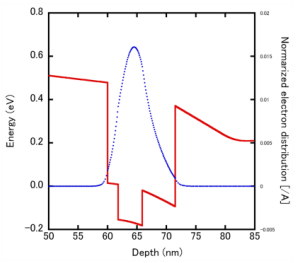

Fig. 2

Fig. 2. Band diagrams and carrier distribution.

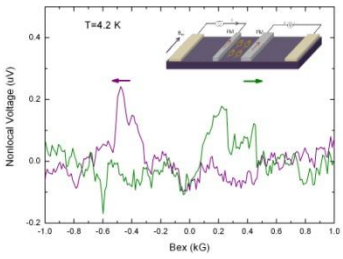

Fig. 3

Fig. 3. Nonlocal spin valve configuration.

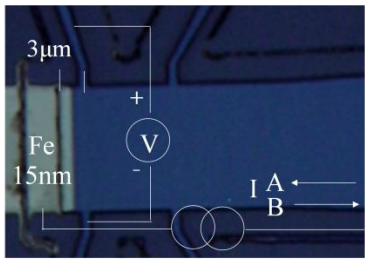

Fig. 4

Fig. 4. Optical microscopy of fabricated Hall-bar with ferromagnetic elctrode.

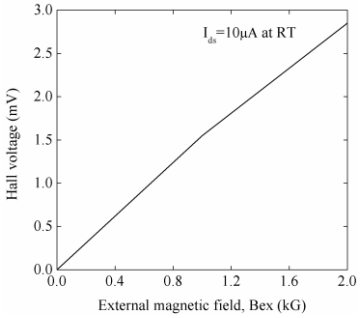

Fig. 5

Fig. 5. The conventional Hall effect of sample #1.

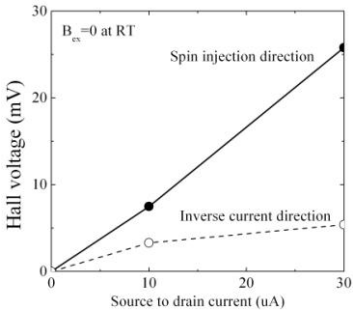

Fig. 6

Fig. 6. Source to drain current dependence of the anomalous Hall effects in zero magnetic field of sample #1 by spin injection.

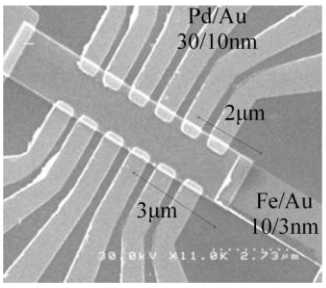

Fig. 7

Fig. 7. Scanning electron microscopy image of sample #2.

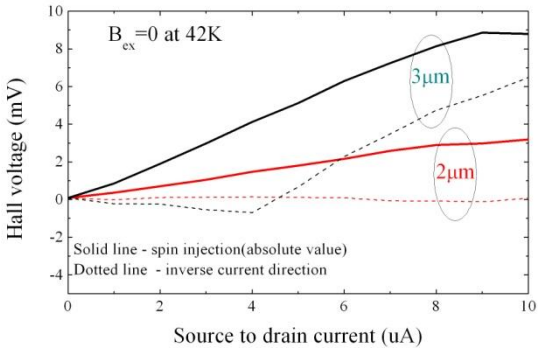

Fig. 8

Fig. 8. Distance from contact dependence of the anomalous Hall effects in zero magnetic field of sample #2.

Epitaxialy defined (ED) FinFET: to reduce V_T variability and enable multiple V_T

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Introduction – Device variability has become a major concern for CMOS technology [1]. Various sources of variability include Random Dopant Fluctuation (RDF), Gate Edge Roughness (GER) and Line Edge Roughness (LER) [2]. The introduction of FinFETs at 22nm node has two issues. Firstly, the effect of RDF is considerably reduced due to undoped fins [3]. But the aggressive fin width (Wfin) requirement (~ Lg/3 [4]) to reduce short channel effect aggravates the electrical impact of LER and makes it greatest contributor to patterning induced variability [2]. Moreover, the edge roughness does not scale with technology and remains independent of the type of lithography used [5]. Secondly, multiple threshold voltage (V_T) is achieved in planar technology by various patterned implant steps, which is unavailable for FinFET technology as the fin is undoped. Multiple V_T transistor technology is essential for power vs. performance optimization by circuit designers [6]. In this work, we propose an alternative to conventional FinFET structure which can (a) reduce overall variability by 4× reduction in sensitivity to LER and (b) enable multiple V_T by applying body bias dynamically without any costly patterned implant steps.

Description of Approach –The Sentaurus^{TM} TCAD simulation deck has been well calibrated with the experimental data (Fig. 1) [7]. A sensitivity analysis of the Wfin on the V_T of FinFET is done from 18 nm to 9 nm node for different magnitudes of LER (Fig. 2). It should be noted that the magnitude of LER implies 3σ variation of Wfin on either side i.e. if the nominal Wfin is 5nm, then with LER magnitude of 2nm the effective Wfin would be 1 or 9 (5 ± 2*2) nm. It can be seen that ΔV_T increases sharply as we scale down Wfin and becomes as large as about 250 mV which is confirmed in literature [2]. To reduce variability, we propose an Epitaxially-Defined-FinFET (EDFinFET) structure with the process flow described in Fig. 3(a). A heavy doped (1e20 cm^{-3}) fin (~12nm) is fabricated in the same way as the conventional fin and a low-doped channel is grown epitaxially all around it (junction abruptness ~1 nm/decade [8]). The excellent thickness uniformity control in epitaxial layer will define a uniform channel depletion-width. The heavy doped starting fin cannot be depleted and thus cannot contribute electrically to variability despite high LER. Similar planar structure has been already proposed [9].The gate is patterned next followed by spacer deposition and the etching of the epitaxial layer for subsequent epitaxial source/drain. The full structure as used in device simulations is shown in Fig. 3(b) for performance and variability evaluation. To compare EDFinFET and conventional FinFETs in terms of LER based variability, structures were generated by a Gaussian autocorrelation model [5] with the RMS amplitude 3σ =2 nm and correlation length Λ = 30 nm and is modeled by a sine function (e.g. LER=$3\sigma\ sin(2\pi x/\Lambda)\pm W/2$) where W is the Wfin (Fig. 3 (c)) [10]. To account for GER, a sensitivity analysis for gate length was done with RMS amplitude 3σ =2 nm. The FinFETs are RDF-immune due to undoped fins. In comparison, the EDFinFET includes bi-layer fin (low doped epi on heavily doped fin) and hence V_T shift due to RDF needs to be evaluated exhaustively. Same has been done by the impedance field method (IFM) [11] which calculates standard deviation in gate voltage due to RDF to maintain constant nominal current at nominal Vg. σVg is plotted vs Vg. σVg at V_T gives σV_T. $3*\sigma V_T$ is ΔV_T due to RDF (3σ fluctuation). Finally the effect of body bias on V_T in EDFinFET is demonstrated.

Evaluation of Results - Fig. 4 shows V_T obtained for different extents of LER. While FinFETs are strongly susceptible to LER in narrower than nominal Wfin cases because of quantum confinement (QC) effects, EDFinFET remains immune to such degradation due to (a) depletion width defined by uniform epitaxy (c.f. patterning dependent depletion width which is the Wfin FinFETs) (b) weaker well formation due to single dielectric interface. Fig. 5(a) shows comparison of V_T shift due to GER, where EDFinFET performs slightly worse than FinFETs. This can be ascribed to single gate control in EDFinFET. Fig 5(b) shows that the immunity of V_T fluctuation due to RDF in EDFinFET is comparable to FinFETs despite having high doping in fins because the depletion is limited to the lightly doped epi-grown channel while the heavy doped fin remains undepleted. Hence, any dopant fluctuation in the highly doped region is electrically screened out. Comparing the worst case ΔV_T due to variability sources individually and cumulatively shows that EDFinFET improves variability in LER by 4X and 2.2X overall (Fig. 6). IV characteristics are compared in Fig 7(a) to show higher on-current (shown on linear scale by Monte-Carlo Simulations without stress dependent mobility enhancement) for same off current even though the sub-threshold slope (SS) is poorer. The higher on-current in EDFinFET is expected because of lower effective EOT due to surface inversion compared to bulk inversion in FinFETs (Fig 7(b)). The poorer SS can be significantly improved by applying gate-bias to the body contact similar to Dynamic Threshold-voltage MOS (DTMOS) for planar MOSFETs [12]. We refer to this configuration as DTEDFinFET (Fig 7(a)). The large SS and I_{ON} improvement are due to better electrostatics from the body-bias assist to the gate control. Fig 8 shows I_{ON} for EDFinFET is 22% better for same variability. In Table 1, EDFinFET shows higher I_{ON} than FinFET while the SS is poorer. In the DTEDFinFET configuration, both I_{ON} and SS are strongly improved. Lastly, dc body bias effectively enables multiple V_T on-the-fly (Fig. 9). A body bias is ineffective in FinFETs to enable multiple V_T due to un-doped fins. Hence process integration based gate multi-work-function and gate-source/drain overlap engineering is proposed [6] which is technically very challenging and cannot provide post fabrication-V_T tuning. In summary, as shown in Table 2, EDFinFET provides attractive performance and variability resistance compared to FinFETs, along with desirable multiple V_T and dynamic V_T features.

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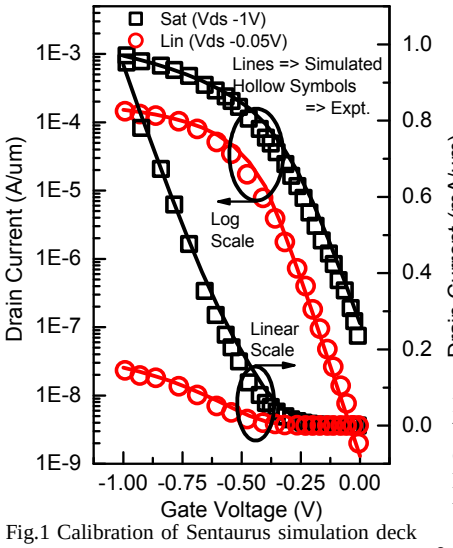


Fig.1 Calibration of Sentaurus simulation deck for quantum corrected drift-diffusion with FinFET experimental data for 25nm channel length [7]

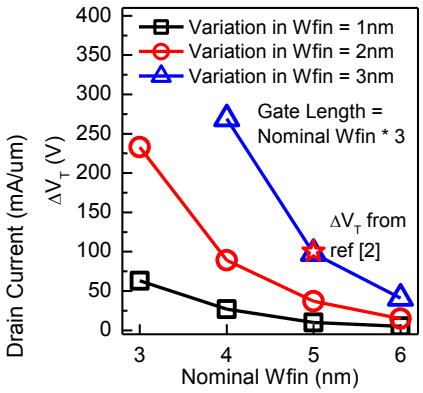


Fig.2 V_T shift for different gate lengths (L_G= Wfin*3) as fin width is reduced from nominal. Quantum Confinements (QC) increases ΔV_T largely as the fin widths get reduced due to un-scalable LER and needs to be addressed.

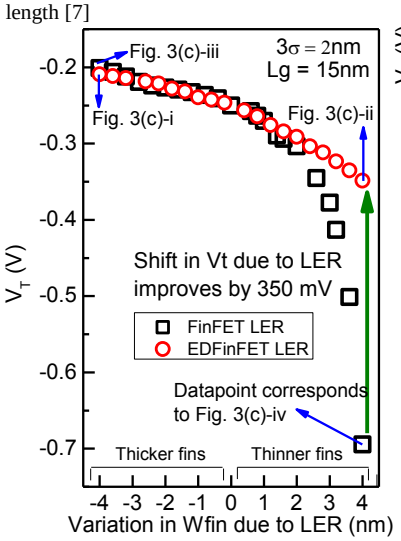
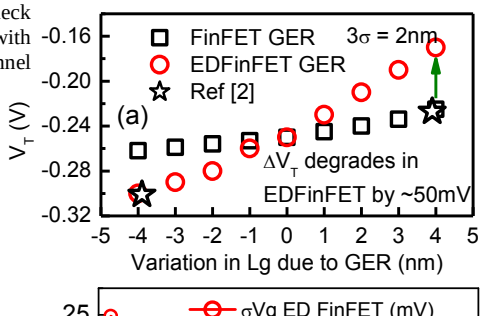


Fig. 4 Comparison of V_T shift due to LER at L_G=15 nm (FinFET Wfin=5nm). ED-FinFET gives ~350mV advantage compared to thinner FinFETs largely affected by QC.



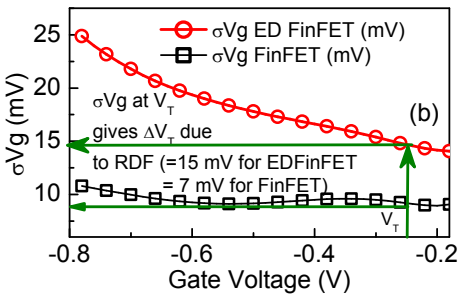


Fig. 5 (a) Comparison of ΔV_T due to GER. It degrades for EDFinFET due to single gate control (b) By Impedance Field Method (IFM) [11], the standard deviation in gate voltage (σVg) for a constant drain current at nominal Vg due to RDF is plotted as σVg vs. Vg. σVg is extracted at V_T to obtain ΔV_T

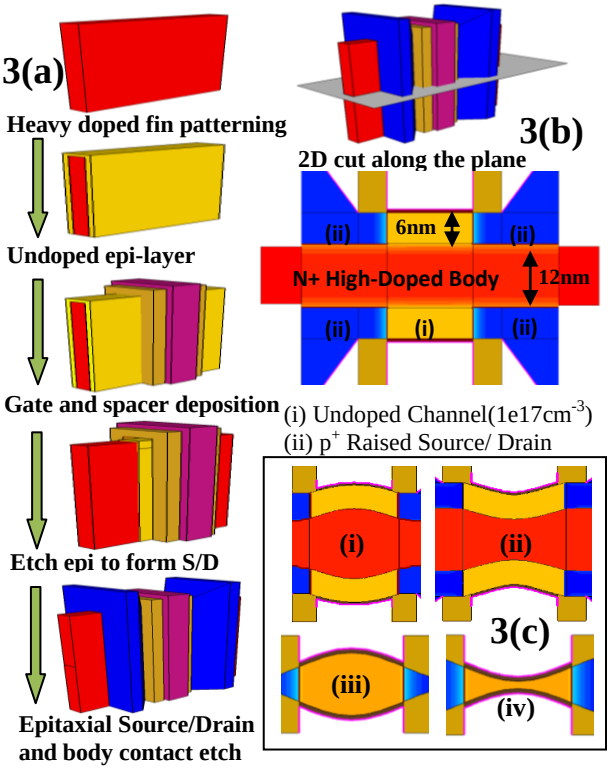


Fig. 3 (a) Process flow for Epitaxially Defined FinFET (EDFinFET) to reduce LER, (b) 2D cut of the device used in simulations (c) Structures generated for LER study using the Gaussian auto-correlation model, (i) Thick EDFinFET, (ii) Thin EDFinFET, (iii) Thick FinFET and (iv) Thin FinFET. Epitaxially defined channel ensures constant channel width (hence no QC induced V_T shift) despite LER in heavy doped body.

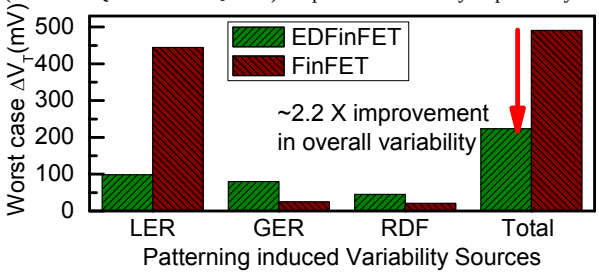


Fig. 6 Comparison of worst case ΔV_T for EDFinFET and FinFET. EDFinFET gives 2.2 X improvement in overall variability

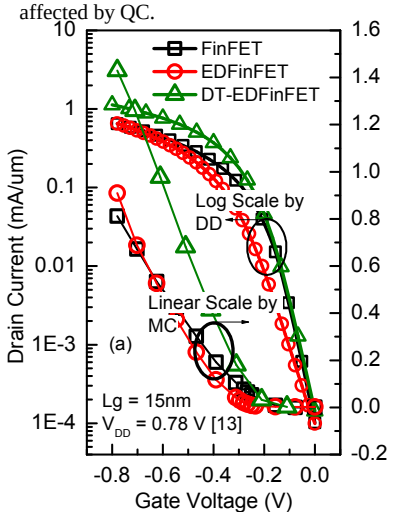


Fig. 7(a) I-V Comparison plot. EDFinFET shows slightly lower SS due to single gate control, however, can be significantly improved by dynamic V_T control; DTEDFinFET [12]. I_{ON} for EDFinFET is better as explained in 7(b). Higher I_{ON} is observed by Monte Carlo (MC) simulations (shown on right y axis in linear scale)

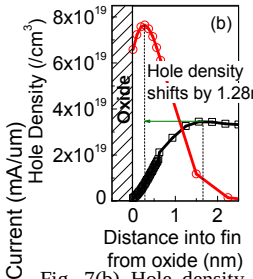


Fig. 7(b) Hole density plot from Oxide interface into the Silicon channel for FinFET and EDFinFET. Less QC in EDFinFET leads to lesser EOT and hence better Ion.

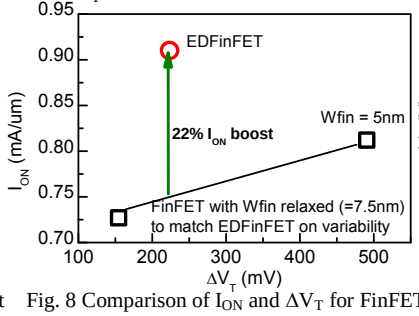


Fig. 8 Comparison of I_{ON} and ΔV_T for FinFET at Lg = 15 nm, Wfin = 5nm (LER prone) and 7.5nm (less prone to LER) and EDFinFET. For Wfin = 5nm, EDFinEFET outperforms FinFET in both I_{ON} and ΔV_T .Wfin = 7.5 nm gives similar ΔV_T but 25% lower I_{ON}.

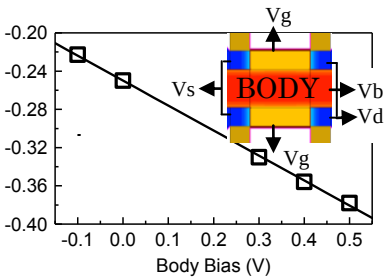


Fig. 9 Body bias can be utilized to change V_T of EDFinFET over a wide range and presents a considerable advantage over conventional FinFETs.

Table 1 I_{ON} (mA/um) and SS comparison at 15 and 10 nm node for same variability (FinFET Wfin = 7.5nm)

	15 nm node		10 nm node	
	Ion	SS	Ion	SS
FinFET	0.727	78	0.747	84
EDFinFET	0.910	99	1.04	101
DTEDFinFET	1.43	69	1.79	68

Table 2 Advantages and Disadvantages of EDFinFET

	FinFET	EDFinFET	DTEDFinFET
I_{ON} (mA/um)	0.812	0.91	1.43
Variability (mV)	490.63	223.6	137
SS (mV/decade)	69	99	69
Multiple V_T	No	Yes	No
Dynamic V_T Control	No	No	Yes

Power Reduction in Nanomagnetic Logic Clocking through High Permeability Dielectrics

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Nanomagnetic logic (NML) has emerged as a novel paradigm to realize non-volatile, nanometer scale, ultra-low energy digital logic [1]. Since there are large energy differences between magnetization states, an external stimulus is required for circuit re-evaluation. In our first experiments we applied an off-chip magnetic field along the hard (i.e., short) axis of a group of nanomagnets. Later, structures that generate fields on-chip were demonstrated [2]. These current-carrying copper wires clad with ferromagnetic material (Supermalloy, $Ni_{79}Fe_{16}Mo_5$), can provide local magnetic fields for NML circuits. However, the required current densities could be as high as ~10^7 A/cm^2 [2]. The ratio of flux density to magnetic field strength (μ = B/H) can be increased by surrounding the magnets with a material of high permeability. While we will need to ensure that the binary state of a magnet is not adversely affected, candidate materials do exist. Freescale demonstrated enhanced permeability dielectrics (EPDs) with embedded magnetic nano-particles to increase the field from a word or bit line in field MRAM without increasing current [3]. That EPD particle sizes are below the superparamagnetic limit helps to ensure that a magnet's state is not unduly influenced. With similar considerations, we have proposed a clocking structure where EPD films surround the nanomagnets, as shown in Fig. 1. With this new design, the magnetic flux can be confined within the EPD film area instead of leaking to the air. As such, the field intensity for switching the nanomagnets can be increased, and the required current density and power for clocking can be reduced (potenitially by μ_r^2 in the case of power). This work shows our efforts of integrating EPD films with nanomagnets for NML clocking.

The EPD is a dielectric matrix (in our case the dielectric material is MgO) with embedded nanometer-size CoFe particles. EPD samples with different CoFe layer thicknesses were deposited in a magnetic material sputtering system under a base pressure of 3×10^{-8} mbar. Fig. 2 shows in-plane SEM images of two of the samples with CoFe single layers of 1.5 nm and 2 nm thicknesses, respectively. The CoFe layer in each sample is composed of discrete particles. Fig. 3 shows the magnetization curves of EPD samples with nominal CoFe layer thicknesses of 1 nm, 1.5 nm and 2 nm. They all exhibit superparamagnetic characteristics. It can be seen that relative permeability (μ_r) and saturation magnetization (M_s) for the EPD sample with a higher CoFe layer thickness are correspondingly higher.

To study the effect of EPDs on the switching fields of nanomagnets, ~10^7 nominally identical Supermalloy ($Ni_{79}Fe_{16}Mo_5$) magnets with 60 nm × 120 nm × 20 nm footprints were fabricated with electron beam lithography and evaporation. This number of devices is enough to provide an adequate magnetic signal for vibrating sample magnetometry (VSM). The magnets are placed sufficiently far apart so that coupling field interactions are negligible. Fig. 4 (a) shows an SEM image of the nanomagnet sample. Fig. 4 (b) shows the easy-axis magnetization curve of the nanomagnets; because of lithographic shape variations and thermal fluctuations, the switching field distribution of the easy-axis hysteresis loop of the nanomagnets was broadened as compared to what would be expected by OOMMF simulations of an ideal single magnet [4].

Figure 5 (a) shows full magnetization curves of the nanomagnets only (same curve in Fig. 4 (b)), nanomagnets with a thin EPD (1 CoFe layer on top) and nanomagnets with a thicker EPD (4 CoFe layers on top). Fig. 5 (b) comes from the same measurement and shows a detailed view of the -1200 Oe to 1200 Oe, -30 μemu to 30 μemu region. Note that the remanence is unchanged for the three samples, since the EPD itself adds no additional remanence. The coercivity of the nanomagnet alone sample is 170 Oe, with the open region of the loop from -900 Oe to 900 Oe. With one CoFe layer on top of the nanomagnets, the coercivity changes to 91 Oe, and the open region ranges from -830 Oe to 830 Oe. With four CoFe layers on top of the nanomagnets, the coercivity becomes 30 Oe, (an 82% reduction compared with nanomagnets alone), and the open region is -650 Oe to 650 Oe. This reduced coercivity implies a decreased distribution in the switching fields over the array of magnets, which is beneficial to reducing switching fields and errors in NML. Moreover, the remanent magnetic moment is the same for these three curves, which means that EPDs do not change the states or properties of the nanomagnets, and the remanence is due to the nanomagnets alone. Notably, Fig. 6 shows a magnetization curve of the EPD sample that was deposited along with the nanomagnet sample, confirming its superparamagnetic characteristics.

In conclusion, we demonstrated an 82% reduction in the coercivity of the nanomagnets with EPD, as well as a decreased switching field distribution; this indicates a possibly significant reduction of power for clocking in NML circuits as desired B fields could be generated with less current. Measurement results also show that EPDs do not change the properties of the nanomagnets. Investigation of the effect of EPDs on coupling fields among the nanomagnets is in progress to demonstrate other EPD contributions to NML circuits.

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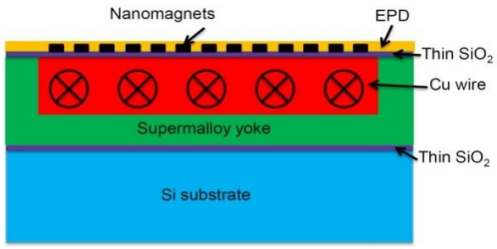


Fig. 1. Schematic of the proposed clocking structure with enhanced permeability dielectric film (top) surrounding the nanomagnets.

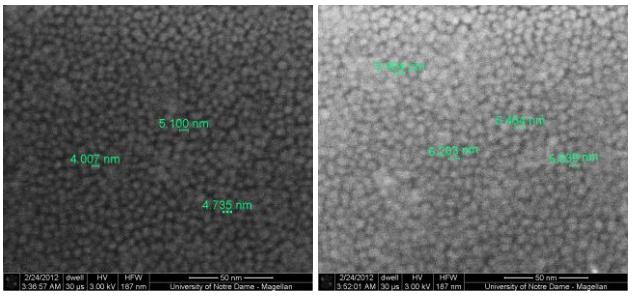


Fig. 2. In-plane SEM images of CoFe single layers with nominal thicknesses of 1.5 nm (left) and 2.0 nm (right).

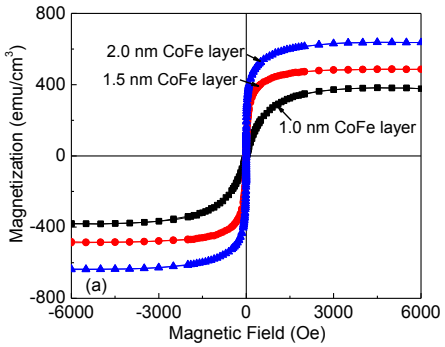


Fig. 3. Magnetization curves of EPD samples with three CoFe layer thicknesses.

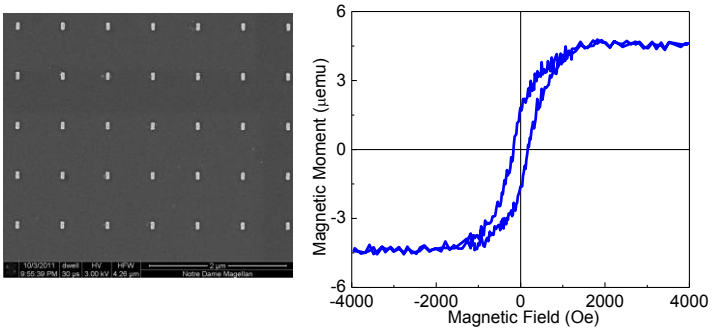
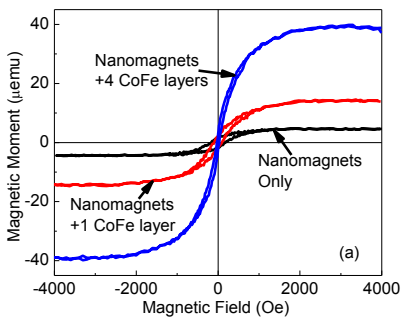


Fig. 4. (a) SEM image of the sample with nanomagnets of 60 nm × 120 nm × 20 nm. (b) Easy axis magnetization curve of the nanomagnets.



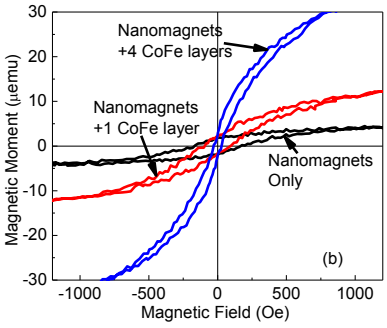


Fig. 5. Magnetization curve of the nanomagnets, nanomagnets with 1 CoFe layer on top and nanomagnets with 4 CoFe layers on top. (a) Full curves and (b) curves from -1200 Oe to 1200 Oe range.

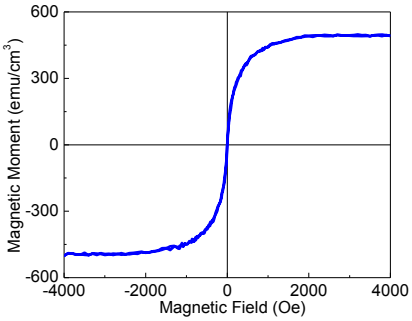


Fig. 6. Magnetization curve of the exact same EPD deposited at the same time for the nanomagnet sample.

New Tunnel-FET Architecture with Enhanced I_{ON} and Improved Miller Effect for Energy Efficient Switching

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Tunneling Field Effect Transistors (TFET) are promising devices to respond to the demanding requirements of future technology nodes. The benefits of the TFETs are linked to their sub-60mV/decade sub-threshold swing, a prerequisite for scaling the supply voltage well below 1V. Main research efforts are currently dedicated to improving the on current (I_{ON}) level in a TFET. However, from the circuit point of view the device capacitances are equally important. It is known that the drain-to-gate capacitance in a TFET is almost equal to the gate capacitance in moderate and strong inversion regimes. Due to enhanced Miller Effect [1], they are known to exhibit large over/undershoot in transient operation as compared to CMOS. Therefore, the effort on improving I_{ON} should be simultaneous to an effort of reducing the Miller capacitance (C_{MILLER}). This work proposes a new architecture which addresses both these issues.
In a TFET the gate modulation of the tunneling barrier is of primary importance. It is clear that in order to have a better gate modulation the tunneling direction should be aligned to the gate electric field. In this scenario, also known as "line tunneling", the source is substantially overlapped by the gate and band-to-band (B2B) tunneling takes place from a gate-field induced inversion layer to the source underneath. This design can have a much larger current due to the larger tunneling area. Line tunneling structure as proposed by [2] shows improved current levels, however also has higher gate capacitances, which slightly overshadows the advantage gained by the improved on current level.

The proposed new all-Silicon structure, as shown in the fig. 1 has an elevated source at an angle of 45°. The effective gate length (measured horizontally) is 50nm. The entire source is overlapped by the gate electrode which aligns the tunneling direction to the gate-electric field. An ultra-thin BOX of 10nm is used to reduce the coupling between source and drain. Fig.1 also shows the e- and hole B2B generation rates at V_G=0.8V.
The simulations were performed using Synopsys TCAD ver. 2010.12 which uses a non-local B2B tunneling model to dynamically determine the tunneling path [3]. Physical models like Shockley-Read-Hall recombination, doping and field dependent mobility and Fermi statistics were also included in the simulations. For quantization effects, the MLDA (Modified Local Density Approximation) model was used. However it should be noted that quantum confinement effects are only partially taken into account [4], as the quantization model is not fully coupled with the B2B tunneling model.

Fig. 2 shows the transfer and output characteristic of the proposed device: an average sub-threshold slope (SS) of 24mV/decade over 4 decades and high current levels are observed. Fig. 3 compares the SS and intrinsic delay of the proposed structure to those of a conventional SOI TFET at V_{DS}=0.8V; the reported figure of merits get even better at lower V_{DS}. Fig. 4 shows the propagation delay and switching energy per cycle for fan-out 1 inverters for three device technologies including hetero-structure (Ge-source n-type and InAs-source p-type) TFET like the ones simulated in [5] and SPICE simulated 65 nm low-V_t CMOS, all the cases have been normalized with respect to cell areas. It is interesting to note that the new structure can outperform CMOS as well as hetero-structure TFETs in terms of both propagation delay and switching energy for sub 0.25 V_{DD}.
In fig. 5, at V_{GS}=V_{DS}=0.2V a C_{dg} lower than both other technologies is observed in the new structure, due to the reduced gate-drain coupling in this structure. The higher C_{gg} of the new structure seen in fig. 4 is due to the higher actual gate length of 70nm ($L_{g,eff}$ = 50nm). This reduction in C_{dg} translates to the lowering of over/under shoot voltage of the new structure in a three-stage inverter configuration as can be seen from the transient behavior of the three technologies in fig. 6. Fig. 6 also shows lower rise and fall times for the new structure, confirming the results in fig. 4. Continuing the study at V_{DD}= 0.25 V, fig. 7 shows the voltage transfer characteristics of the three technologies in a single-stage inverter configuration. From the inset in fig. 7, it is evident that the new structure has the highest gain amongst the three. Clearly the advantages of the proposed new structure are more pronounced for low supply voltages, where TFETs are intrinsically optimized for.

In conclusion we have proposed and simulated a new device architecture which provides higher current as well as lower C_{MILLER} resulting in considerably faster operation, more so at lower V_{DD}. Circuit level performance is also remarkably good in low V_{DD} regime and even better than CMOS below V_{DD}= 0.2V.

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The research leading to these results has been funded by the European Community's Seventh Framework Program (FP7/2007-2013) under grant agreement n° 257267.

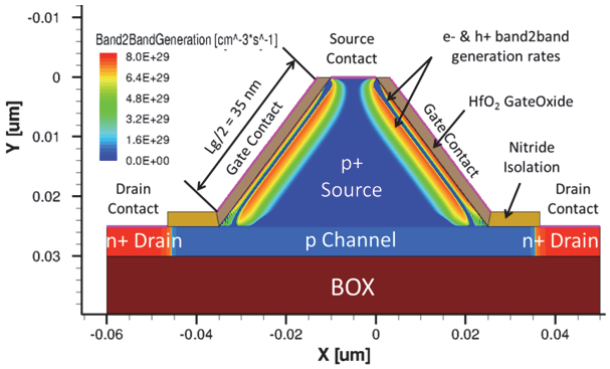

Figure 1. Proposed structure with T_{Si}= 5nm, effective Gate length $L_{g,eff}$ = 50 nm. Gate work-function is 3.9eV. $N_{A,source}$= $10^{20}cm^{-3}$; $N_{D,drain}$= $10^{20}cm^{-3}$ while $N_{A,channel}$ = $10^{18}cm^{-3}$. 2.5nm of HfO_2 are used as gateoxide; t_{BOX}=10nm; t_{bulk}=1µm. 15nm of Si_3N_4 are used as spacers.

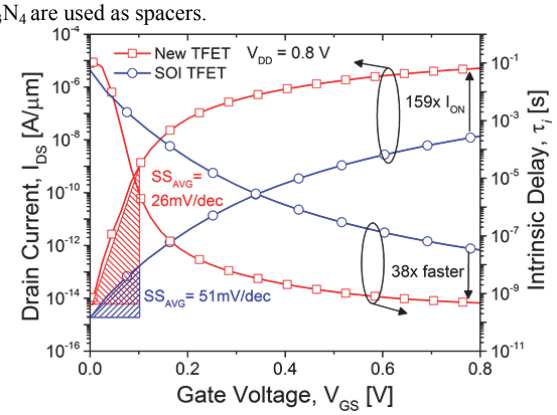

Figure 3. Transfer characteristics comparison of the proposed new structure with a SOI TFET at V_{DS}=0.8V. Improved I_{ON}, better SS and faster device speed (Intrinsic delay = CV/I) is observed.

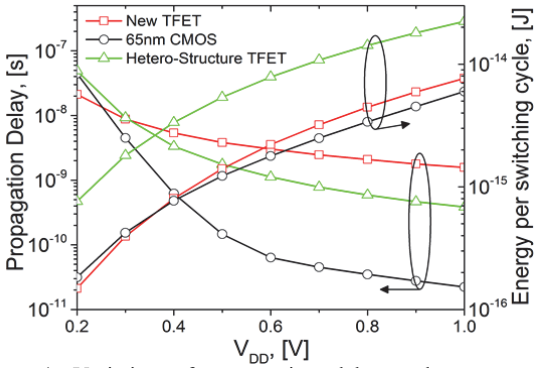

Figure 4. Variation of propagation delay and energy per switching cycle with supply voltage. The proposed TFET becomes comparable to CMOS at V_{DD} 0.3V and lower.

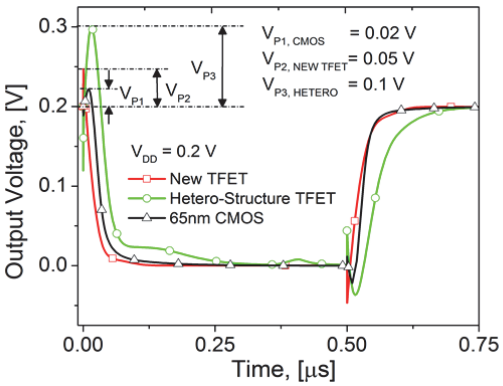

Figure 6. Transient response of the three technologies in a three-stage inverter configuration for an input period of 1µs. The overshoot voltages are also shown.

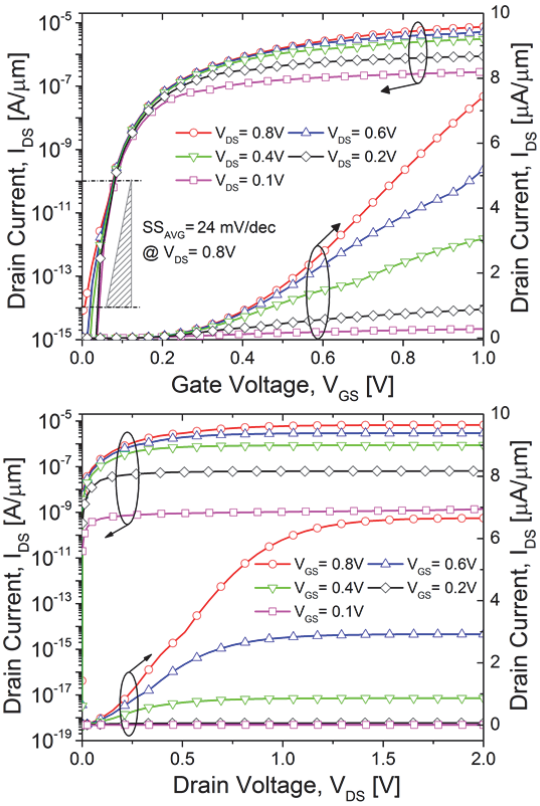

Figure 2. Transfer (top) and output (bottom) characteristics of the proposed new structure.

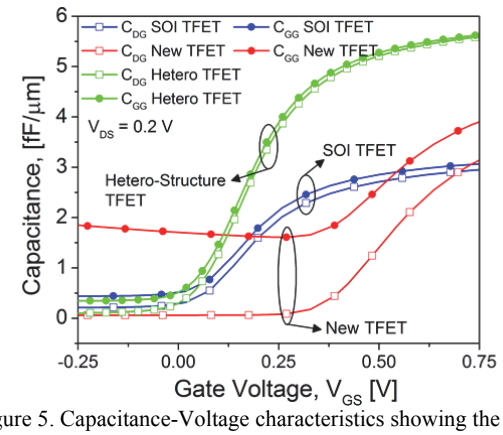

Figure 5. Capacitance-Voltage characteristics showing the drain-to-gate(C_{dg}) and gate(C_{gg}) capacitances as a function of V_{GS}.

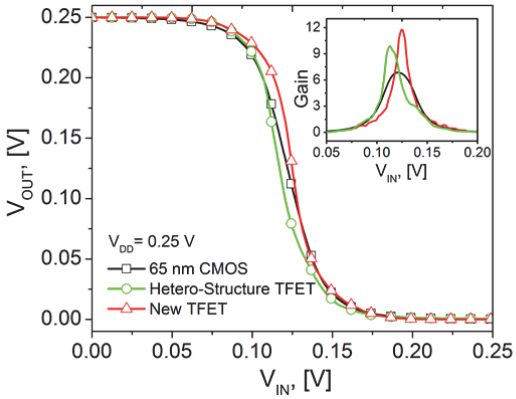

Figure 7. Voltage transfer characteristics of the three technologies reported in fig. 4 & 6. Inset shows the inverter Gain = dV_{OUT}/dV_{IN}.

Switching dynamics in ferroelectric-charge hybrid nonvolatile memory

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Abstract

A statistical model is proposed for ferroelectric (FE) polarization switching response during program and retention in FE-charge hybrid nonvolatile memory. During the program pulse, high fields first occur in the FE layer and then transfer to tunnel oxide after FE polarization, which leads to a two-step process: (a) rapid domain switching (~1ns – 100ns) and (b) electron injection into the floating gate (~10μs – 1ms). This device can be potentially used as a dual-mode memory with a fast low-retention mode (DRAM), and a slower high-retention mode (Flash).

Introduction

Integration of FE thin film in gate-injection flash memory was demonstrated to improve memory window as well as endurance and retention over comparable Flash and FE-FET (Fig. 1) [1], with charge injected from the control-gate complementing FE polarization. Organic PVDF with slow polarization switching had been used in the experimental demonstration of the hybrid device concept [1]. In this paper, we present the device characteristics with fast-polarization PZT and propose dual modes of DRAM-like and Flash-like operations.

Model

A part-by-part statistical switching model [2] is used for the time steps of FE domains with self-consistent electrostatics to include the effect of the depolarization field during program, erase and retention. The total field experienced by FE domains, $E_{tot}(t)$, is the sum of applied and depolarization fields. For FE with activation field α, infinite-field switching time t_∞, the average time for switching of the N+1[th] part out of a total of M_0 parts is given by:

$$\frac{M_0 - N - 1}{M_0 - N} = \exp\left(-\frac{t_{N+1}}{t_\infty}\exp\left(-\frac{\alpha}{E_{tot}(t_N)}\right)\right)$$

Simulations were calibrated with switching polarization measurements on PVDF and PZT [3] MFM capacitors at different applied program fields (Fig 2) with parameters in Table I.

Table I: Extracted parameters

Parameter	PVDF	PZT
α	7MV/cm	1.2MV/cm
t_∞	30ns	100ps

The hybrid FE-charge structure simulated (Fig. 1) consists of a top tunnel oxide (5 nm SiO_2), metallic floating gate, 150 nm FE layer and 10 nm SiO_2 bottom control dielectric grown on silicon substrate. The tunneling current through the top oxide was calculated by the Tsu-Esaki method [4]. FE parameters from [2] were used for retention and program simulations. Self read disturbance on charge and polarization is ignored.

Retention

Storing electrons on the floating gate increases the fraction of domains retaining their poled state (Fig. 3), because the depolarization field experienced at each switching decreases (Fig. 4). The injected charge behaves similar to image charges in MFM and screens out the depolarization field. This gives three direct advantages: 1) stabilization of FE polarization, 2) addition to the total memory window (Fig. 5a), and 3) field in tunnel oxide being reduced in retention and increased in program/erase. Initial memory window loss is dominated by polarization relaxation before charge leakage (Fig. 5b). A further improvement of polarization retention is to use a high-k bottom dielectric for better coupling ratio (Fig. 6). Charge loss from the floating gate could become more significant on cycling the device, especially when larger charge is stored in the floating gate.

Program and Erase

As opposed to an MFM capacitor, domains in the FE layer in the hybrid memory do not experience constant fields during program and erase, due to the potential drop in adjoining dielectrics. At the start of program, the randomized FE domains lead to higher voltage drop in the FE, which accelerates domain switching. For FE with higher saturation polarization while keeping all other parameters fixed, domain switching is faster, although complete poling is in danger of being close to the breakdown field in the top oxide (Fig. 7).

As the polarization increases, field in the top oxide is enhanced to initiate electron injection (Fig. 8). Charge tunneling through the top oxide becomes significant at time scales of ~10μs to 1ms. The threshold voltage V_T also reflects this two-time-constant process (Fig. 9). High figures of merits in retention/program time ratio t_{ret}/t_{prog} for a given memory window (6V) is desirable. t_{ret} is defined as the time required for 70% loss in the total memory window. The maximum occurs for low bottom dielectric thickness (Fig. 10).

Due to the clear difference in time scales for the two mechanisms, memory window gained through polarization switching at low time scales can be utilized for fast-write and fast-access applications, similar to a DRAM (Fig. 11), whereas electron injection can give a high retention, high V_T mode similar to Flash (Fig. 12).

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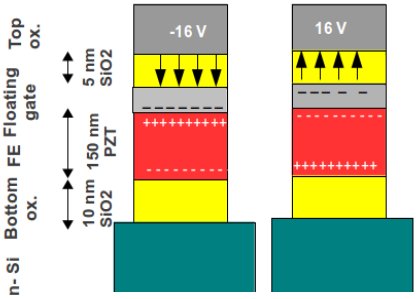

Fig. 1: The hybrid FE-charge memory device in program and erase operations.

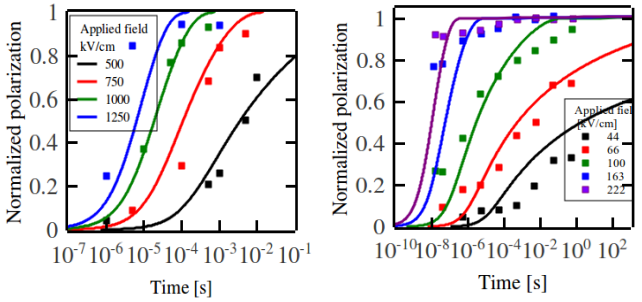

Fig. 2: Polarization switching measurements on MFM capacitors were used for model calibration of a) PVDF, and b) PZT [3].

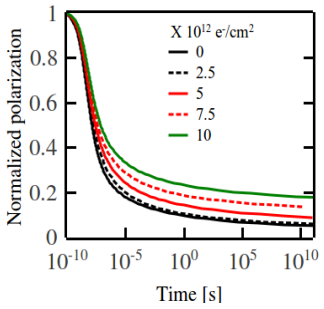

Fig. 3: Control gate injection of electrons into floating gate leads to larger fraction of domains retaining their poled state.

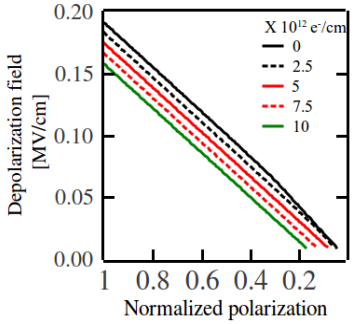

Fig. 4: With gate-injection charge on floating gate, each domain switching event occurs under a reduced depolarization field.

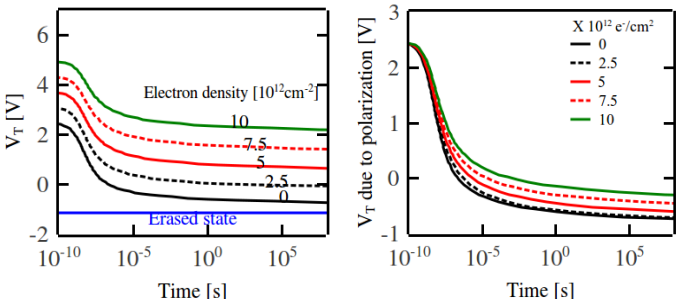

Fig. 5 a): Total memory window increases with gate-injected electrons. b) Significant part of the polarization is rapidly lost after the program pulse is removed.

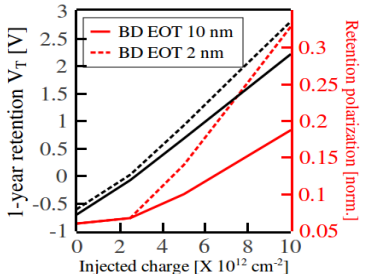

Fig. 6: Reducing the EOT of bottom dielectric with a high-k material improves the retained polarization and memory window

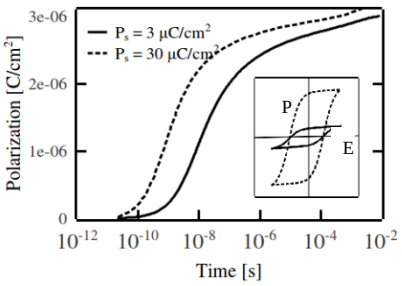

Fig. 7: For FE with higher saturation polarization, switching at (-16V program) occurs more rapidly, but poling is not 100% complete even after 10 ms.

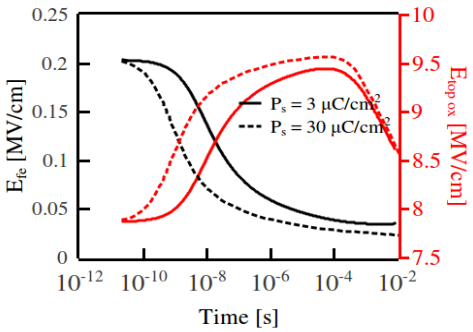

Fig. 8: At start of program (-16V), higher fraction of program voltage drops across FE and domain switching is accelerated. Gradually, field in FE reduces and field in the top-oxide increases, leading to electron injection from control gate.

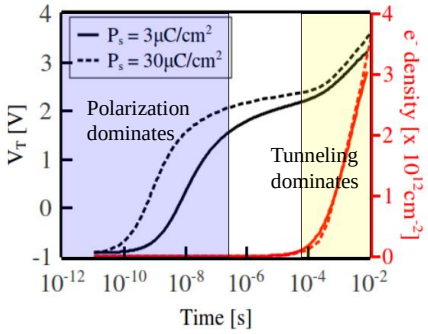

Fig. 9: V_T increases in the two-time-constant process with fast domain switching (~0.01 – 0.1μs), followed by slow electron injection (~0.1-1ms).

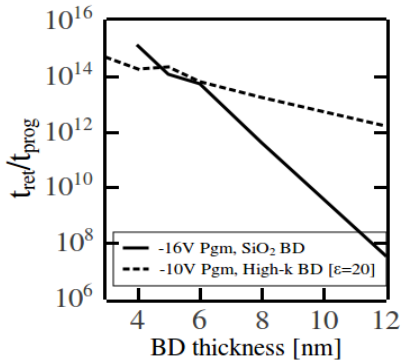

Fig. 10: t_{ret}/t_{prog} figures of merit as a function of bottom dielectric (BD) thickness. SiO_2 BD devices are programmed at -16V, while high-k BD devices were programmed at -10V.

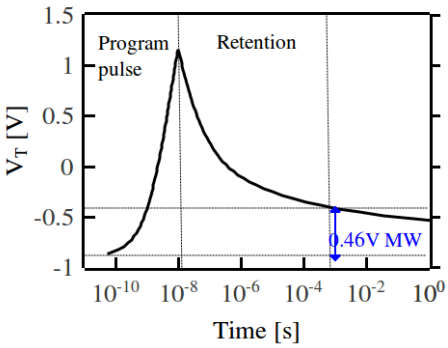

Fig. 11: The FE-charge hybrid memory in DRAM mode shows 1ms retention time and 10 ns program time at -16V for reaching 60% of polarization.

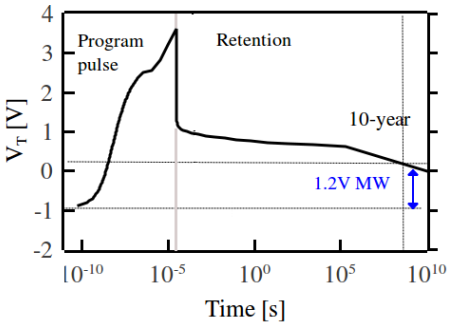

Fig. 12: The FE-charge hybrid memory in the Flash mode, shows 10-year retention time by applying a -16V gate pulse for 30 μs program.

Frequency Dependence of Amorphous Silicon Schottky Diodes for Large-Area Rectification Applications

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Schottky diodes can play a valuable role as rectifiers in Large-Area Electronics (LAE) systems and circuits. They can be used to recover a DC signal when an AC carrier is used to transmit signals between adjacent plastic electronic sheets through near-field wireless coupling [1], rectify DC power after AC transmission between sheets to provide power to sensors, and so forth. In this paper we describe: 1) the intrinsic frequency limits of Schottky diodes fabricated on hydrogenated amorphous silicon (a-Si:H); 2) circuit design strategies for using the diodes at frequencies far beyond their intrinsic limits; 3) and the application of these strategies to demonstrate, to the best of out knowledge, the first amorphous silicon (a-Si:H) full-wave rectifier, with an AC-to-DC power conversion efficiency (PCE) ranging from approximately 46% at 200 Hz to greater than 10 % at 1 MHz.

Schottky diodes were fabricated using PECVD at under 200°C, with a 100nm chrome back contact, 30 nm n+ a-Si:H, 200 to 1000 nm intrinsic a-Si:H, and a 100 nm chrome front contact (Fig .1). For low-forward voltages they have an exponential type current-voltage behavior (Fig. 2), associated with transport over the semiconductor/metal interface. At intermediate voltages they show a power-law relationship ($I \propto V^m$) suggesting that diode current density is restricted by space-charge-limited current (SCLC) in the presence of an exponential trap distribution [2]. Reducing the thickness of the intrinsic layer diminishes the effect of SCLC and allowed us to obtain higher current densities. A lower intrinsic layer thickness caused the capacitance (Fig. 3) to increase, due to the diode's specific capacitance C obeying $C = \varepsilon/d$ where d is the thickness of the intrinsic layer and ε is the dielectric permittivity [3].

In large-signal applications, the intrinsic frequency of a Schottky diode is limited by its internal RC time constant, where R is the effective series resistance given by $\sim V_{applied}/I_{forward}$ and C is the capacitance of the diode. R is large due to the low mobility of amorphous silicon and SCLC. It can be reduced by operating at high current densities, enabled by decreasing the thickness of intrinsic layer, which allows smaller device area and lower capacitance. Decreasing the intrinsic layer results in increased specific capacitance, but overall still significantly reduces the RC time constant (Fig. 4).

When a Schottky diode is used in a half-wave rectifier (Fig. 5(a)) it is limited by its RC time constant. For example, in Fig. 5(c), the power conversion efficiency for a half-wave rectifier using a $1mm^2$ diode drops to 3.2 % at 20 kHz. However, in a full-wave rectifier circuit, undesired capacitive currents in opposite directions through connected diodes can cancel out, and allow the circuit to operate at higher frequencies. For example, in the full-wave rectifier shown in Fig. 5(b) the inputs (V_{inp} and V_{inm}) oscillate in counter phase, so for node V_{outp} the undesired capacitive current through D1 is cancelled by an opposite current though D2. This concept was experimentally demonstrated using four integrated $1mm^2$ Schottky diodes with a conservative 1000 nm thick intrinsic layer to reduce reverse leakage. It enabled the full-wave rectifier to operate with far greater power conversion efficiency than the half-wave rectifier, as demonstrated in Fig. 5(c).

In summary, reducing the thickness of the intrinsic layer of an amorphous silicon Schottky diode decreases its internal RC time constant and raises its intrinsic frequency. Further improvements can be obtained by designing symmetric diode-based circuits, such as a full-wave bridge rectifier, which we have experimentally demonstrated can function at frequencies far beyond the intrinsic limit.

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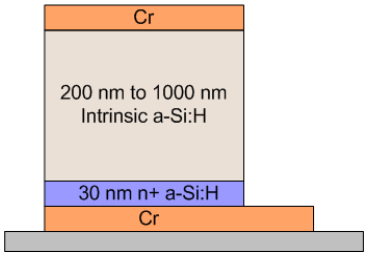

Fig. 1. Structure of a-Si:H Schottky diode.

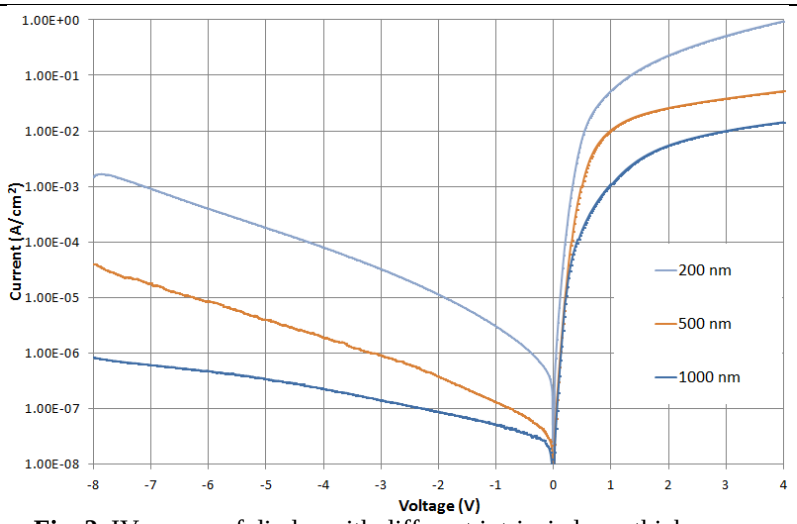

Fig. 2. IV curves of diodes with different intrinsic layer thicknesses.

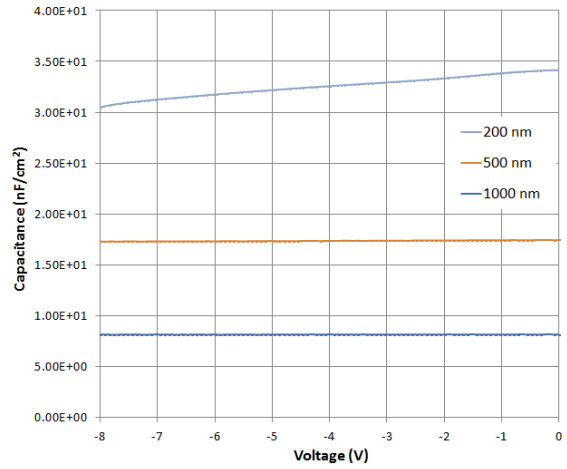

Fig. 3. CV curves for diodes with different intrinsic layer thicknesses

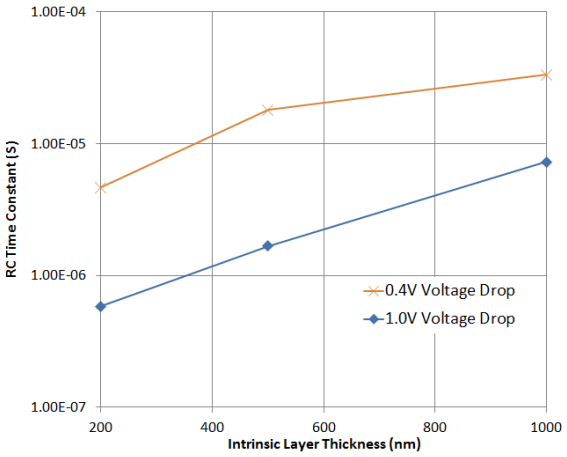

Fig. 4. RC time constant for diodes with different intrinsic layer thicknesses.

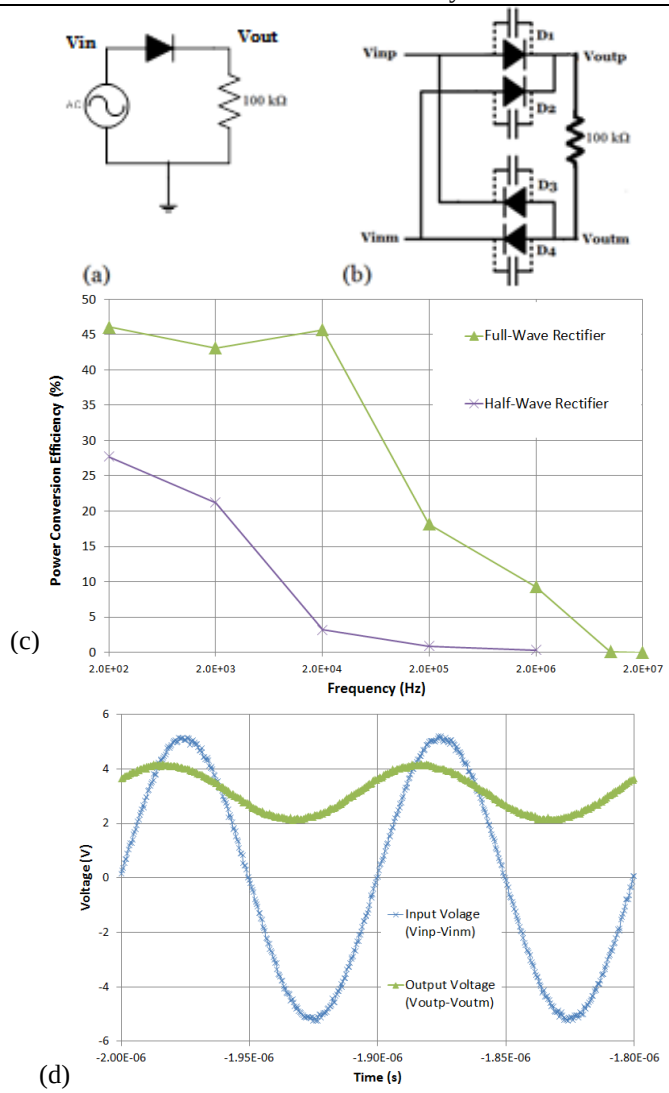

Fig. 5. (a) Half-wave rectifier (b) Full-wave bridge rectifier (c) Power conversion efficiency of full and half-wave rectifier (d) Full-wave rectifier at 10 MHz. The load in (c) and (d) is 100kΩ.

Reliability Improvement Achieved by N_2O Radical Treatment for AlGaN/GaN Heterojunction Field-Effect Transistors

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Recently, O_2 or N_2O plasma treatment has been extensively investigated about the passivation effect of AlGaN/GaN HFETs [1-3]. However, the effect was not consistent. Due to ion bombardment on the sample surface, the devices might be significantly degraded [2,3], suggesting that it might be difficult to suppress the plasma damage. On the other hand, Tapajna et al. [4] have reported the reliability issue of such oxidation process. In this work, a method called N_2O radical treatment will be introduced. With this method, we suppressed the current collapse of AlGaN/GaN HFETs by ~40%. And the reliability was also improved by ~60%.

Figure 1 shows the schematic illustration of the radical generator. After plasma generation, a DC bias was applied to the plasma beam to trap the ions. Only high reactive radicals are left to diffuse to the sample surface. Thus, a thin layer of "native" oxide can be formed on the AlGaN surface without high temperature process and ion bombardment.

Figure 2 shows the cross section of the AlGaN/GaN HFETs with and without the N_2O radical treatment. Both devices are passivated by 10 nm of Al_2O_3. Figure 3 shows the output characteristics of the devices and the drain currents were increased by the N_2O radical treatment. Figure 4 shows the transfer characteristics. The threshold voltage was shifted to the negative direction by ~0.5V and g_m was not degraded. With C-V measurement of Schottky diodes, it was confirmed that ~1.5nm of insulator layer has been formed on the surface and the electron density was slightly increased, as shown in Fig. 5. Figure 6 shows the two-terminal breakdown characteristics of the devices with 0.5 μm of L_{GD}. The gate leakage current was suppressed by the N_2O radical treatment by near two orders. The breakdown voltage was increased accordingly.

Under off-state, with increase of drain bias, the depletion region will extend towards the drain due to the trapping effect at the drain side of the gate edge[5]. As shown in Fig. 7, the potential in the channel can be monitored through a 2DEG-sensing bar (2DEG: two dimensional electron gas). In the beginning, the depletion region doesn't get to the 2DEG sensing bar. Then the 2DEG sensing bar was electrically connected to the drain through the channel. As a result, the sensing voltage will follow the drain bias. When the depletion just went across the 2DEG sensing bar, the sensing voltage will become fixed, because extra drain bias will be applied to the depletion region extended over the 2DEG sensing bar. If the trapping effect was suppressed, the turning point will appear at higher drain bias. We actually observed that the devices with N2O radical treatment have a turning point at higher drain bias. This phenomenon proved that the N2O radical treatment reduced the surface traps [5].

Figure 8 shows the off-stress induced on-resistance (R_{ON}) variation as a function of off-stress drain bias. The stress time was 10 s. The N_2O radical treatment suppressed the current collapse by ~40%. The reliability of the devices was investigated by 30 min of high-voltage off-stress (V_{GS}=-6V, V_{DS}=65V). This degradation stress generated more traps and cause enhanced trapping. However, with N_2O radical treatment, the enhanced trapping was suppressed by ~60%.

The surface chemical composition was investigated by XPS measurements. To specially investigate the surface, the escape angle (the angle between the detector and the sample surface) was set at 15°. Figure 9 shows the Ga3d and Al2p signals. For the N_2O radical treatment, oxidation of Ga and Al can be confirmed with the extension of the signals. Compared to Ga3d signals, Al2p signals have more extension to the high energy side, suggesting that Al has stronger oxidation. However, for O_2 plasma treatment, it has been reported that the oxidation of Ga was severer [1]. Therefore, N_2O radical treatment must have a different passivation mechanism with that of O_2 plasma treatment. Figure 10 shows the ratios of integrated XPS intensities. It was confirmed that the N_2O radical treatment formed a surface oxidation layer rich of oxidized Al. However, for the control sample, the oxidation of Ga is stronger. Therefore, the stronger Al-O bond might be responsible for the improved reliability achieved by the N_2O radical treatment.

About long term reliability, more results will be presented during the conference. Both HFETs and MOS-HFETs have been investigated.

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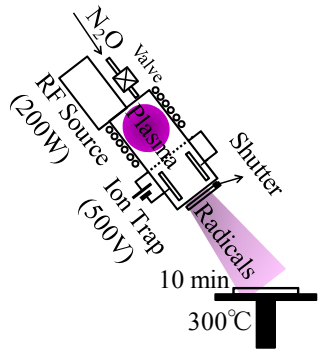


Fig. 1 N_2O radical treatment

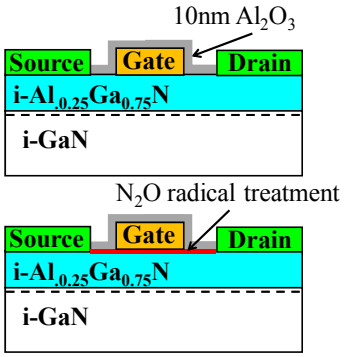


Fig. 2 Sample structures

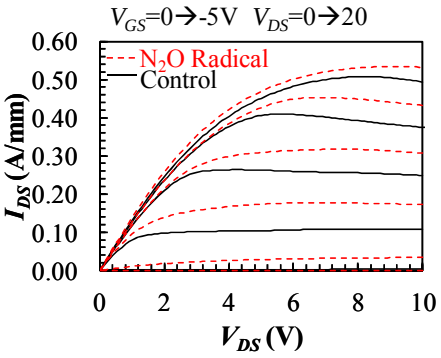


Fig. 3 Output characteristics

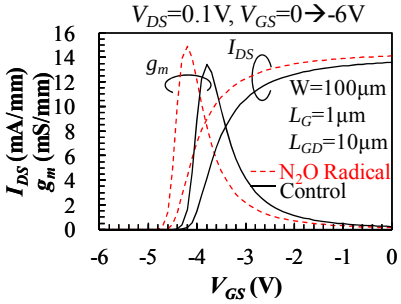


Fig. 4 Transfer characteristics

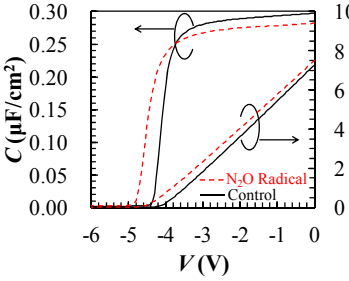


Fig. 5 C-V curves of SBD

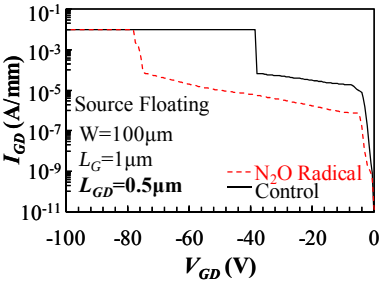
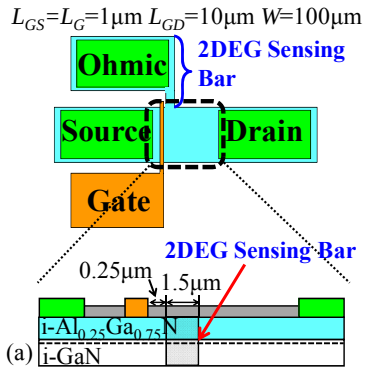


Fig. 6 Breakdown characteristics



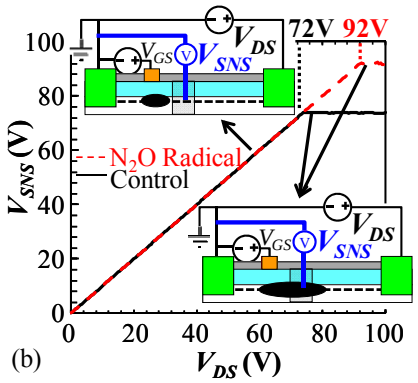


Fig. 7 Measurement of gate depletion (V_{GS}=-6 V, V_{DS}=0→100 V)
(a): Device structure; (b): Sensing voltage VS Drain bias

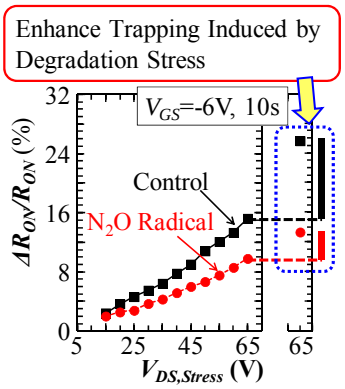


Fig. 8 On-resistance variation induced by off-stress

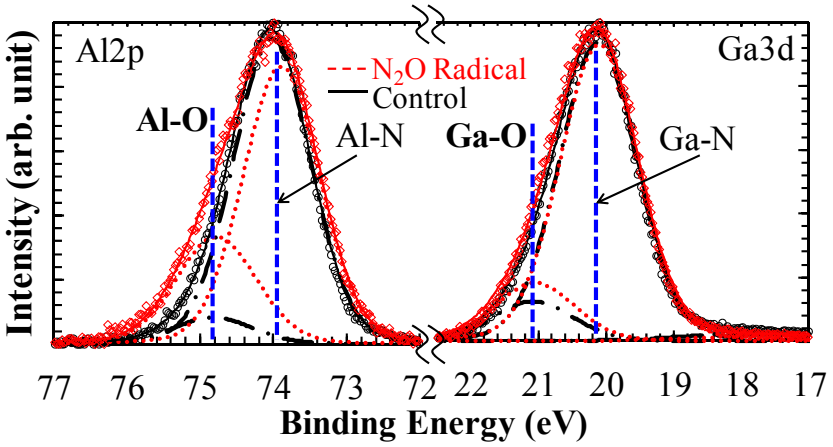


Fig. 9 Normalized XPS signals of Al2p and Ga3d (15° escape angle)

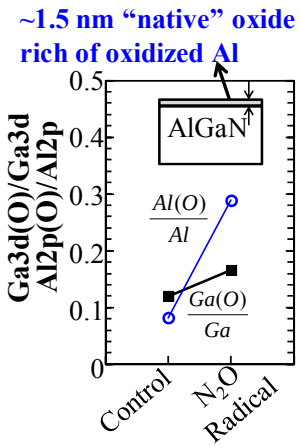


Fig. 10 Ratios of integrated XPS intensities

Exploring Variability and Reliability of Multi-Level STT-MRAM Cells

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Multi-level spin-transfer torque magnetoresistive random access memory (STT-MRAM) has been proposed to improve bit-density, power consumption and speed of standard STT-MRAM. The traditional STT-MRAM bit-cell consists of one access transistor and one magnetic tunnel junction (MTJ) (1T-1R) [1] whereas multi-level STT-MRAM has two stacked MTJs with one access transistor (1T-2R, see **Fig. 1**) as proposed in [2]. However, variability and reliability issues can degrade the benefits associated with multi-level STT-MRAM. The variability issues in 1T-2R are attributed to the process variations in both the access transistor and the MTJs [3]. The primary reliability concern in 1T-2R is the time-dependent dielectric breakdown (TDDB) of the tunnel junction (MgO) in the MTJ [4]. TDDB lowers lifetime and can further degrade the performance of the MTJ cell with MgO thickness scaling [4]. Hence, in this paper we present in-depth study of variability and reliability of multi-level STT-MRAM cells. We also propose device/circuit optimization techniques for design space analysis of 1T-2R cell.

Reading and writing the 1T-2R cell: Reading a 1T-2R cell requires sensing of different resistance states that represent the data stored in the cell. A nondestructive self-reference sensing (NSRS) scheme was proposed in [6] to mitigate sensing failures that arise when using a single global reference. NSRS leverages the fact that the slope of MTJ resistance versus current depends on the state of the MTJ. Hence, the same scheme can be used to read the 1T-2R in two steps. In the first step, a fixed current (I_0) is pumped through the 1T-2R cell generating a bit-line voltage. This voltage is then stored on a capacitor connected to one input of a differential sensing amplifier (DSA). In the next step, a different current, I_1, is pumped through the 1T-2R cell to generate a bit-line voltage that drives the other input of DSA. The amplifier output has four analog voltage levels; each one corresponds to a different resistance state of the 1T-2R cell. Finally, a decoder converts the analog voltage into digital data. Note that distinction between "01" and "10" states is achieved by using unequal resistances for the MTJs. **Writing** data into 1T-2R cell also takes two steps unlike the 1T-1R cell. Note that the device in 1T-2R consists of two MTJs in which one has a larger critical current (I_C) than the other. In our convention, the MTJ with larger I_C stores the most significant bit (MSB) and the other stores the least significant bit (LSB). Since the MTJ's are series connected in the bit-cell, both MSB and LSB are first "programmed" during write, namely, during the first write step the MTJs store '00' if the MSB to be stored is '0', and '11' if the MSB to be stored is '1'. In the second step, the LSB is "programmed". Since the I_C of the MSB device is larger than I_C of the LSB device, MSB data is intact after the second write step.

Simulation Technique: We use a self-consistent hybrid MTJ/CMOS framework based on SPICE to perform all the simulations [5]. In this model the device dimensions of each MTJ such as the MgO thickness and the cell area as well as physical parameters are user defined. By tuning these parameters we have calibrated our model (**Table 1**) to match the experimental data presented in [1]. The switching characteristics of each individual MTJ and their series connection are shown in **Fig. 2**. Moreover, the effect of process variations on the performance of multi-cell STT-MRAM was investigated using, one million Monte Carlo runs within our simulation framework. The MTJ process variations are introduced as variations in the effective T_{ox} and effective area of MTJ reported in [2].

Study of Variations and Design space exploration of 1T-2R cell: Two types of read failures can occur in 1T-2R cell: (a) disturb failure and sensing failure. **Disturb failure** occurs when data is accidentally written into the cell during read when the read current exceeds the critical current of one of the MTJs. **Sensing failure** occurs when DSA senses the resistance state of the cell incorrectly. For example, the cell may have stored '10' but the sensing circuitry detects the state as '11'. For sensing the cell properly, large enough resistance difference is needed between different states for the DSA to sense the differential currents. **Fig. 4** shows that under process variations, the difference in bit-cell read current between states may fall below that required for DSA to sense. Also, write failures may occur due to write currents falling below I_C as shown in **Fig. 5**. During write, '00' or '11' is first written into the cell depending on the value of MSB. Driving currents larger than I_{00} or I_{11} in order to mitigate write failures can degrade the oxide reliability as we show later. Note, after writing the MSB, the LSB is written. Hence, drive currents larger than I_{10} or I_{01} might result in flipping of the MSB, which has been written in the previous cycle. Therefore, 1T-2R cell must be optimized to reduce such failures in the presence of process variations. **Figs. 6, 7** depict read and write iso-failure contours for different magnitudes of process variations -- 2% in T_{ox} and 5% in area leads to 100 parts per million (100ppm) failure rate. Furthermore, sweeping the area-resistance product of each MTJ and tuning the limit of DSA, we get the design points for read as shown in **Fig.8**. In **Fig. 9** a composite plot for read and write is drawn for yield=99.9%. The non-shaded region is the design space with the feasible points. Note, all the design points in this region have RA_2>RA_1 for non-destructive read, but RA_2 cannot be much larger than RA_1 since it will lead to write failures.

Reliability Analysis: Since the main operation of the STT-MRAM memory is based on the tunneling current passing through the oxide, reliability analysis (mainly TDDB) and design for reliability is important. The design parameter that can be tuned to trade off lifetime and yield is T_{ox}. In **Fig. 10** we sweep T_{ox} and plot in the same graph the average lifetime of MgO and read/write parametric failures. Decreasing T_{ox} leads to both lifetime and read failure degradation but write failures are improved. Hence, an optimal point for T_{ox} has to be chosen. If the optimal T_{ox} achieved by considering only parametric failures (0.95nm is our study) does not meet the lifetime specifications then thicker T_{ox} has to be chosen at the expense of increased failures. Note that choosing thinner T_{ox} (<0.95nm) improves write failures but leads to lifetime degradation.

Conclusion: In this paper we have presented a comprehensive analysis of multi-valued STT-MRAM and their benefits and drawbacks. Results shows that in order to reduce read failures in scaled geometries, self-reference reading scheme is necessary. We have also shown that by choosing appropriate RA_1 and RA_2 (we define the feasible RA_1-RA_2 region in the design space), one can reduce both read and write failures. However, in order to achieve higher reliability, a thicker T_{ox} is needed, which can further constrain the RA_1-RA_2 design space of multi-valued STT-MRAMs.

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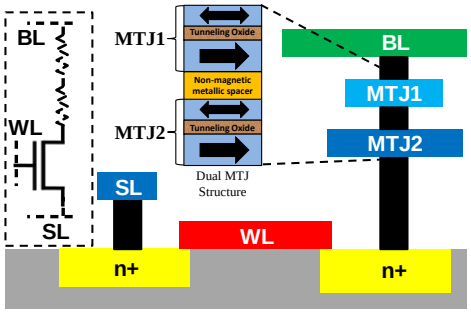


Fig. 1: Illustration showing the CMOS access transistor with two MTJs stacked (MLC) in (a) the metal stack and circuit schematic diagram.

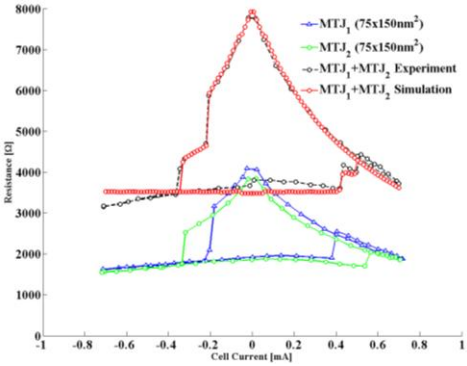


Fig. 2: Resistance-Current characteristics for the series 2MTJ STT-MRAM using model [2] and comparison with experimental data.

	MTJ_1	MTJ_2
Area (WxL) [nm²]	140x70	150x75
$T_{ox,1}=T_{ox,2}$ [nm]	0.8	0.8
$Polarization_{plus}$	0.31	0.25
$Polarization_{minus}$	0.61	0.45
Magnetization M_s [emu/cm²]	800	800
TMR	130	130
R_PA [Ω-μm²]	20	20
K_{u2} [erg/cm²]	$2.6x10^5$	$2.6x10^5$
α (LLG coefficient)	0.01	0.01

Table 1: Model parameters used to calibrate our physics-based SPICE MTJ sub-circuit in order to simulate both MTJ_1 and MTJ_2.

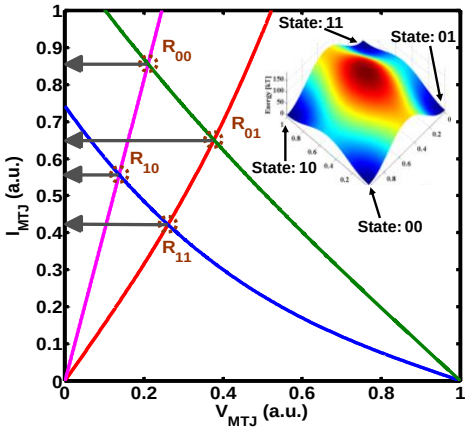


Fig. 3: Load line and energy landscape for the MLC showing the four stable operating points.

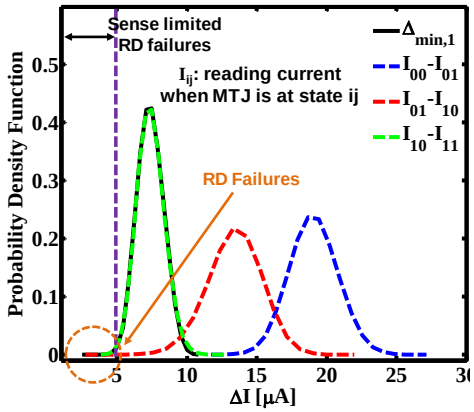
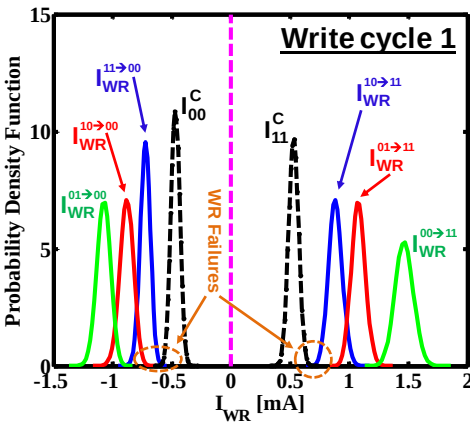


Fig. 4: PDF of ΔRD current for a default Mont Carlo run showing the different failure modes Δ_{min}=2% of Tox and 5% of S.



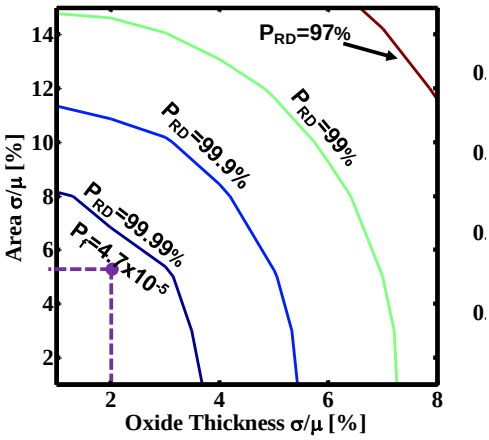


Fig. 6: Read failure iso-yield variations in oxide thickness and area of both MTJ_1 and MTJ_2. Tox_1=Tox_2 and $Area_1$=2x$Area_2$.

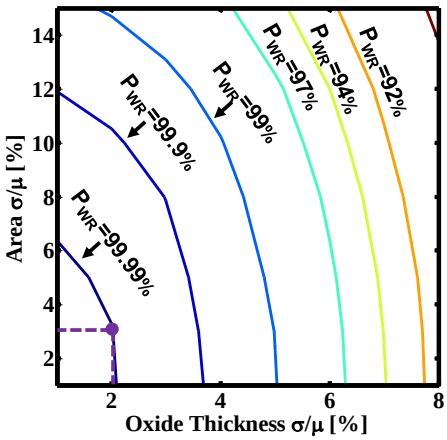


Fig. 7: Write failure iso-yield variations in oxide thickness and area of both MTJ_1 and MTJ_2.

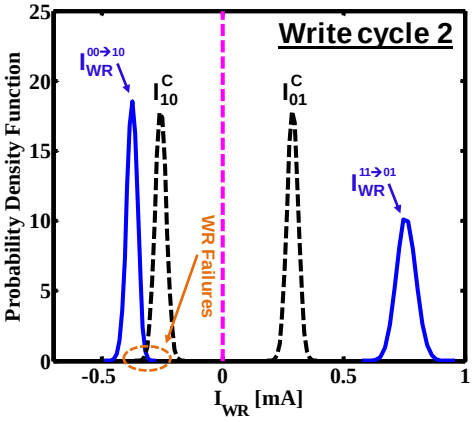


Fig. 5: PDF of WR current for a default Monte Carlo run showing the WR failure modes. The two cycle scheme leads to failures in either first cycle or the second one.

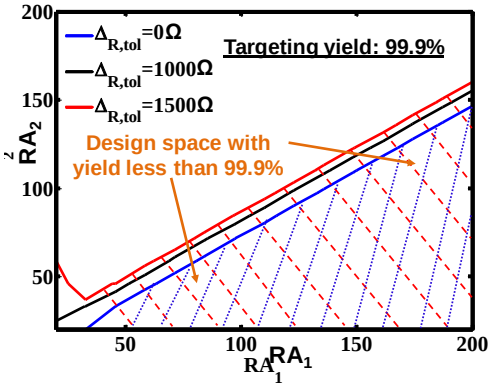


Fig. 8: Design space exploration for RD by sweeping the RA product of each MTJ transistor in the stack.

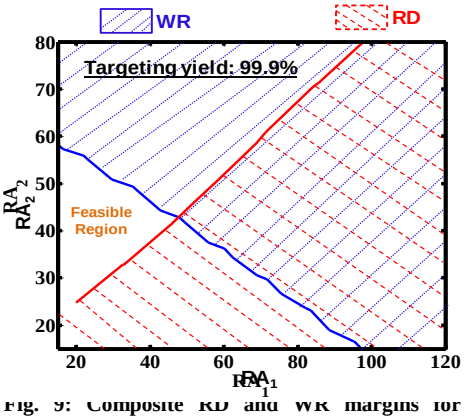


Fig. 9: Composite RD and WR margins for yield=99.9%.The shaded regions are the non-readable and writable sections.

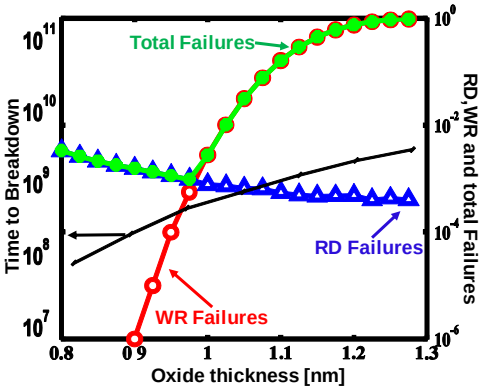


Fig. 10: Reliability analysis where the trade-off between parametric failures and lifetime determine T_{ox}. Lifetime (T_{BD}) prediction is based on the MTJ with the smallest area since larger current density passes through it.

Comparative Study of LEDs conformally overgrown on multi-facet GaN NWs vs. conventional c-plane LEDs

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Over the last decade, considerable efforts have gone into researching techniques to improve the efficiency of light emitting diodes (LEDs) based on the III-nitride material system. These efforts can be classified into two main approaches : improving the internal quantum efficiency (IQE) and increasing the light extraction efficiency of the LED devices. In the work outlined below, we demonstrate a unique LED structure that has a significantly enhanced light output intensity compared to c-plane LEDs by tackling both approaches simultaneously.

Using the embedded voids approach (EVA)[1], we demonstrated the conformal overgrowth of a LED structure on GaN nanowires[2]. The n-type GaN nanowires (NWs) were formed using a maskless ICP-RIE technique on MOCVD grown n-type GaN templates. One half of the sample was not etched to provide a reference area for growing a conventional c-plane LED for a comparative study. Overgrowth on the nanowires was then employed by growth of the active MQW structure along the non-polar and semi-polar facets of the nanowires. During the overgrowth, a non-complete lateral coalescence between the NWs resulted in void formation. Finally, p-type GaN was overgrown until a planar coalescent top surface was achieved. The LEDs were then fabricated as mesas (400μm x 400μm) with a ring-shaped p-contact.

Transmission electron microscopy (TEM) studies revealed that the MQWs were oriented along both lower order semi-polar planes [1-101] and [11-22] and the higher order semi-polar planes. In the lower parts of the NW, the MQW orientation was observed to be along the non-polar a- and m-planes. The spacing between embedded voids was determined to be of about 0.5-1 μm and the void density to be of about 10^8 cm^{-2}. Electroluminescence (EL) was carried out on the fabricated LEDs and light was captured from the back surface of the sapphire substrate. The light output intensity was found to be three times greater for the NWs LED, and a considerably reduced peak wavelength shift was observed as compared to the c-plane LED over the same range of current densities. The greater light output intensity in the NWs based LED was attributed to four main factors: (i) a lower dislocation density in the overgrown film as result of dislocation sinking in the voids; (ii) reduced quantum confined Stark effect (QCSE) due to nonpolar and semipolar alignment of the MQW region; (iii) an increased QW area for a given planar area in the NWs LED as compared to similarly sized c-plane LEDs and (iv) void-assisted wave-guiding of the light to help photons impinge the GaN/sapphire interface with a lesser probability of being totally internally reflected and thus improving light extraction. In addition, we investigated the ratio of light output intensity of the NWs LED vs the c-plane LED as a function of current density. At lower current densities, the lower QCSE in NWs LED is responsible for a large ratio. This reduces with increasing current density as carrier screening of the polarization field in the c-plane LED negates the QCSE effect. The ratio saturates at higher current densities where the mechanism for higher light output is dominated by the light extraction efficiency that depends only on the device geometry and is independent of the current density in the NWs LED.

1. P. Frajtag, N.A. El-Masry, N. Nepal, S.M. Bedair, Appl. Phys. Lett. **98** (2011) 023115
2. P. Frajtag, A.M. Hosalli, G.K. Bradshaw, N. Nepal, N.A. El-Masry, S.M. Bedair, Appl. Phys. Lett. **98** (2011) 143104

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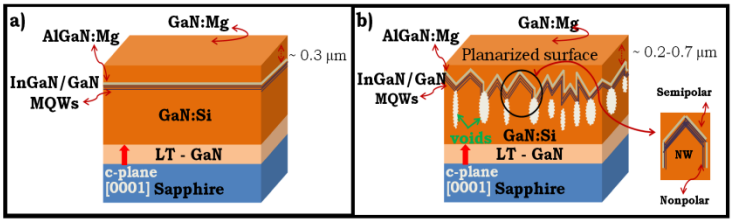


Fig. 1: (a) 3D schematic of the LED structure grown on the unetched n-GaN template. $In_xGa_{1-x}N$/GaN MQWs deposition is on polar (0001) c-plane. (b) 3D schematic of the LED structure grown on the etched n-GaN NWs template.

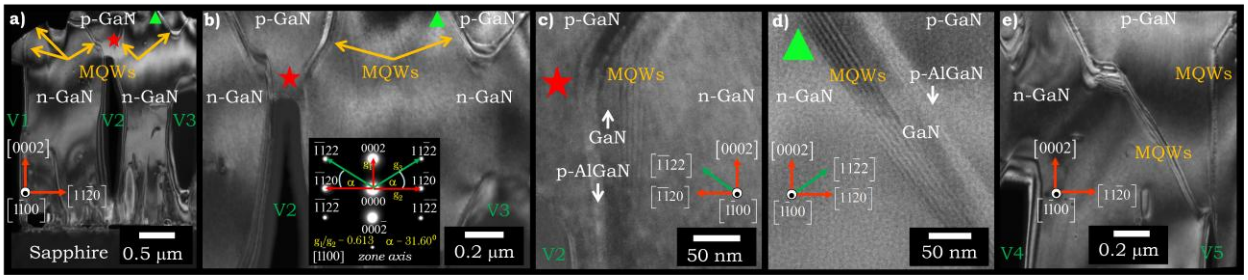


Fig. 2: DF TEM data in [m-zone] views: (a) the LED structure grown on NWs showing conformally grown MQWs on the semipolar and nonpolar crystallographic planes above the embedded voids network with the p-GaN filling the space between the NWs' tips, (b) the MQWs on the NWs' semipolar plane facets exhibit an increase in the surface area, (c) a detailed view of the conformally grown MQWs on the NWs' non-polar plane facet, (d) a detailed view of the conformally grown MQWs on the NWs' low-order semipolar plane facet, and (e) the MQWs on the NWs' are grown conformally on semipolar and non-polar plane facets depending on the stage of the coalescence process.

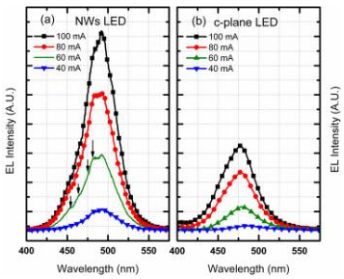
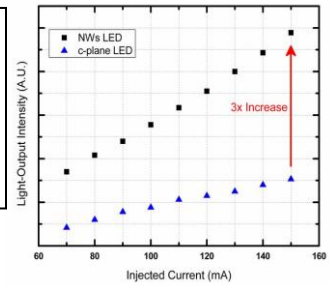


Fig. 3 : Electro-luminescence spectra of (a) c-plane LED and (b) NWs LED at different applied currents.

Fig. 4 : Integrated light-output intensity of the c-plane and NWs LEDs vs. injected current.



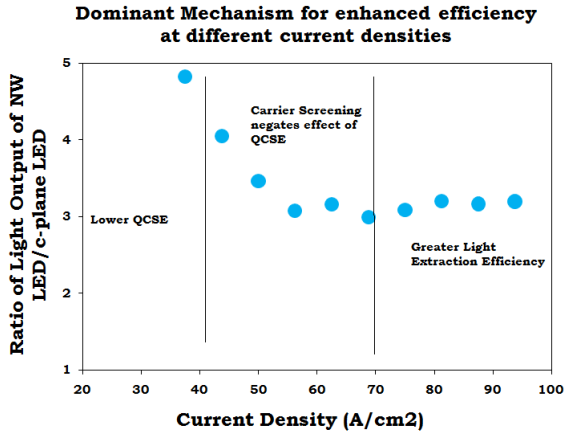


Fig. 5 : Ratio of light output of NWs-based LED/c-plane LED vs. Injected Current Density. The dominant mechanism that determines the trend of this ratio is indicated for different regions of current density.

Inkjet-printed SWCNT films for stretchable electrode and strain sensor applications

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Stretchable electronics is one of the most attractive research areas for next-generation electronics application, where most parts of devices need to show stable and good mechanical properties under flexible and bendable deformation conditions. In order to implement stretchable electrodes, "soft metal" such as gold, silver, and copper has been widely used, but they showed relatively poor mechanical properties, especially in highly stretched cases. Therefore, metallic carbon nano tube (CNT) based materials have been considered the most adequate candidate in such conditions due to their excellent mechanical properties. In addition, relative easiness of controlling sensitivity of resistance change with applied strain is another advantage of the CNT based materials because their characteristics can be changed by various chemical treatment and structural changes. When the sensitivity is controlled to be large, the CNT films can be used as strain sensors.

Inkjet printing method has many advantages such as low process cost, high process speed and easy pattern control in comparison with conventional vacuum-based processes. In order to control mechanical and electrical properties of the inkjet-printed and patterned CNT films, architectural control and/or post treatment with nitric acid can be performed. This type of chemical treatment is known to improve electrical properties of the CNT electrodes via chemical doping [1] while we found that untreated CNT films showed poor properties and higher sensitivity of resistance change with strain, which is required for strain sensor applications. Therefore, in this paper, we report these advantageous properties of the CNT films, which are formed by using inkjet-printing process and home-made metallic single walled CNT (SWCNT) ink.

A schematic diagram of inkjet-printed devices is shown in Fig. 1. After SWCNT ink with aqueous surfactant is made, it is inkjet-printed on polydimethylsiloxane (PDMS) substrate. The printed film is washed by drop-casting deionized (DI) water with a syringe. In order to control its characteristics, two different processes are used. Chemical doping is performed by drop-casting nitric acid with a syringe, resulting in much reduced resistance of the SWCNT film and decreased sensitivity of resistance change with strain. Therefore, chemical doping is utilized for implementation of stretchable electrodes. Trade-off between resistance and transparency can be also controlled via number of printing times, which is shown in Fig. 2. When patterned SWCNT layer is additionally printed, architectural changes of the printed film occur, leading to increased sensitivity of resistance with strain. We use these inkjet-printed SWCNT films with higher sensitivity as strain sensors.

The cycle tests of SWCNT electrodes at low (1 mm/min) and high (100 mm/min) speeds are shown in Fig.3 and Fig.4, respectively. All of the samples have been tested for strains up to 50%. They showed irreversible resistance increase at first cycle but they showed reversible and much smaller variation in resistance after the second cycle. It was reported that this type of irreversible increase at first cycle was caused by loss of connection between each CNT [2]. Resistance change of SWCNT films which has architectural control is shown in Fig. 5. They showed high sensitivity to strain. Strain sensitivity is typically defined by a gauge factor represented by $(dR/R)/(dL/L)$. The gauge factor can be controlled by architectural control pattern etc.

By using inkjet-printing method and SWCNT ink, we can control resistance sensitivity to strain and thus, easily define areas where strain sensor or stretchable electrode needs to be fabricated. When array of the strain sensors is formed with the stretchable electrodes, motion or movement detection of specific area can be more accurately detected. Therefore, we believe that the inkjet- printed SWCNT films are simple, cost-effective and scale-controllable approaches for stretchable electronics applications.

[1] H.Geng, K. Kim, K. So, Y. Lee, Y. Chang, and Y. Lee, *J. AM. CHEM. SOC.*, **129**, 7758. (2007)
[2] Y. Zhang, C.J. Sheehan, J. Zhai, G. Zou, H. Luo, J. Xiong, Y.T. Zhu, and Q.X. Jia, *Adv. Mater.*, **22**, 3027. (2010)

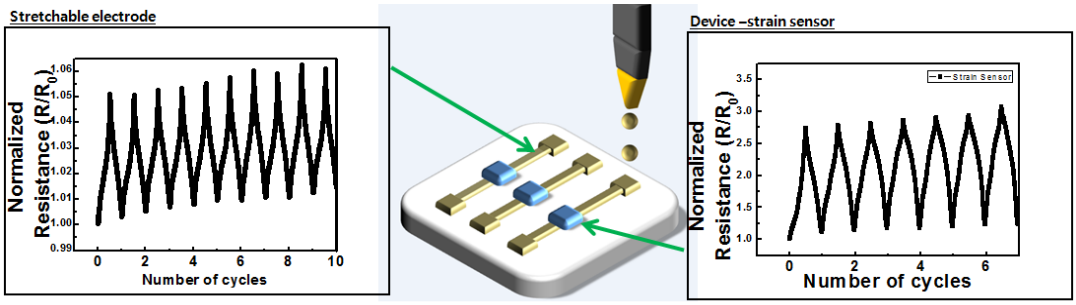

Fig. 1. A schematic diagram of SWCNT films. Two components are fabricated by inkjet printing of water-based SWCNT ink. Stretchable electrodes are treated by chemical doping which helps to decrease resistance of the films. Strain sensors are treated by architectural control which causes increasing resistance of the SWCNT films.

Fig. 2. Inkjet-printed CNT films on PDMS substrate. When 1 printing is performed on PDMS substrate, it has about 79 % of transmittance in visible range. As printing times increase, the transmittances of CNT film decrease.

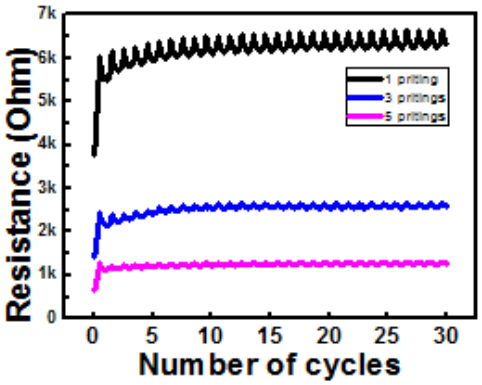

Fig. 3. Cycle test results of 1, 3, 5- time inkjet-printed SWCNT films which are treated by chemical doping at low strain speed (1 mm/min). All of the samples are tested for strains up to 50%. They have irreversible resistance increases at first cycle.

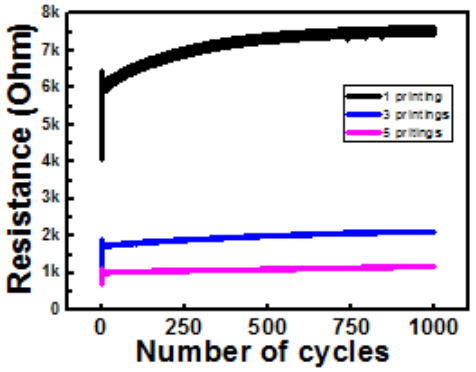

Fig. 4. Cycle test results of 1, 3, 5-time inkjet-printed SWCNT films which are treated by chemical doping at high strain speed (100 mm/min). All of the samples are tested for strains up to 50%. They have irreversible resistance increases at first cycles. The resistance variations are small at large cycle number.

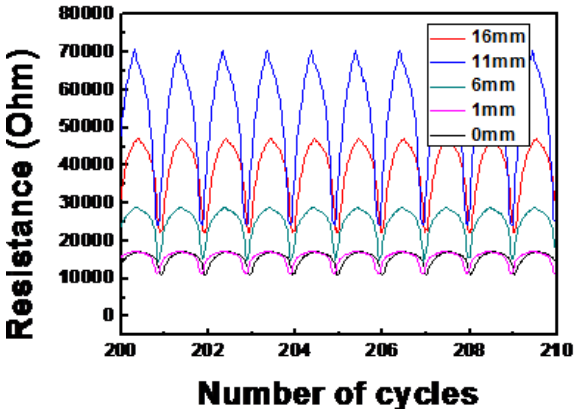

Fig. 5. Strain sensitivity of resistance of SWCNT films which contains architectural control layer at high strain speed (100 mm/min). All of the samples are tested for strains up to 50%. Unlike the CNT films which are treated by chemical doping, it has large resistance chance during one cycle. It is showed that pattern length which is one of architectural control can affect sensitivity to strain.

Comparison of Instantaneous Crystallization and Metastable Models in Phase Change Memory Cells

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Phase change memory (PCM) is a possible competitor for future generation non-volatile storage class memory due to its fast writing speed and aggressively scaled packing density [1]. In PCM cells current is confined through narrow conductive paths to create high current densities in a chalcogenide material ($Ge_2Sb_2Te_5$ or GST is most commonly used). The resulting heat allows the material to switch between crystalline (set) and amorphous (reset) states, changing the cell's resistance by ~10-10^4 times [2] depending on the cell dimensions. Less energy is required for melting smaller regions, therefore aggressive cell scaling results in reduced power and increased packing density. The properties of GST change by orders of magnitude as a function of temperature, and thus understanding its thermal dependency is crucial to accurately model phase change memory cell operation.

Electrical and thermal conductivities of GST have been reported as a function of temperature (Fig. 1) based on slow measurements (~1K/minute) [3]. In nanometer scale memory cells, GST traverses the entire temperature range from room temperature to melting in nanoseconds and is expected to retain a metastable phase until melting during reset operation. The electrical and thermal conductivities of GST change with variations in carrier concentration and mobility as a function of temperature. Therefore models based on constant values or materials properties extracted from slow-measurements are expected to differ significantly from actual cell operation. In this study we model cell operation by using extrapolations for electrical and thermal conductivity functions assuming that GST remains in fcc phase until melting and compare it to models based on slow measurements.

COMSOL Multiphysics was used to simulate the mushroom cell (Fig. 2a) with 2D rotational symmetry in series with an nFET (L x W = 22 x 200 nm, V_t = 0.32 V). The joule heating and electric current modules were coupled such that the current continuity (1) and heat transport (2) equations are solved self-consistently.

$$\nabla \cdot J = -\nabla \cdot (\sigma(T,E)(\nabla V + S\nabla T)) = 0 \quad (1) \qquad d_{GST} \cdot C_P(T)\frac{dT}{dt} - \nabla \cdot (\kappa(T)\nabla T) = \frac{J \cdot J}{\sigma(T,E)} - TJ \cdot \nabla S \quad (2)$$

where J is the current density, V is the electric potential, S is the Seebeck coefficient, and d_{GST} is the mass density. Thermoelectric effects are accounted for in this system of equations [4]. Thermal boundary resistance (TBR) was included with a 1 nm thick virtual layer assigned a thermal boundary conductance (TBC). Room temperature TBC between GST and TiN has been reported as ~0.05 $GW \cdot m^{-2} \cdot K^{-1}$ [5]. This value is applied between TiN and SiO_2, while TBC functions (Fig. 1b) have been included for GST boundaries to capture the change in TBR upon melting. The heat capacity of GST (Fig. 1e) is included as a constant value of 202 $J \cdot kg^{-1} \cdot K^{-1}$ with a 10 K wide plateau of 14.8 x 10^3 $J \cdot kg^{-1} \cdot K^{-1}$ starting at melting temperature (873 K) [6] to account for the latent heat of fusion (L_f). The more realistic electrical resistivity (metastable fcc phase) (Fig. 1c) function was generated by extrapolating the exponential behavior near room temperature to melting. The corresponding thermal conductivity function (Fig. 1d) was calculated by adding the contribution from phonons (estimated based on room temperature value and assumed to be zero upon melting) and electrons (using the Weidemann-Franz law) as a function of temperature.

Simulation results show more heating but similar molten volume using the instantaneous crystallization model for 10 nm heater diameter (Fig. 3). However, for heater diameters of ~20 nm, the metastable model shows a filament formation at the beginning of the pulse which relaxes into a mushroom shape by the end of the 100 ns (Fig. 3). The filament retains its shape without collapsing into a mushroom throughout the entire reset operation for larger diameters (~40 nm). The read (V_{GATE} = 1.75 V, V_{DD} = 15 mV) current contrast is 24 for the instantaneous crystallization model and 15 for the metastable model for the 20 nm cells for the reset operation shown in Fig. 4.

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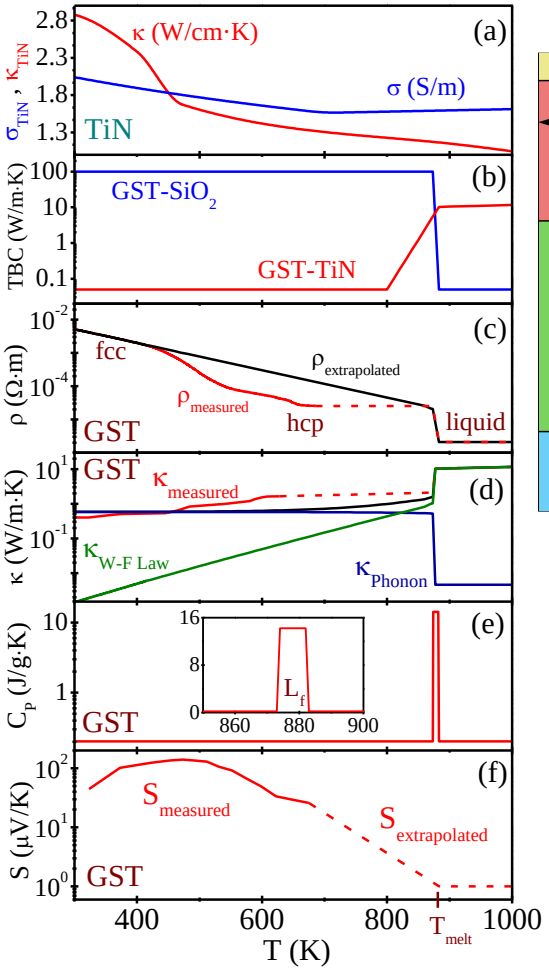

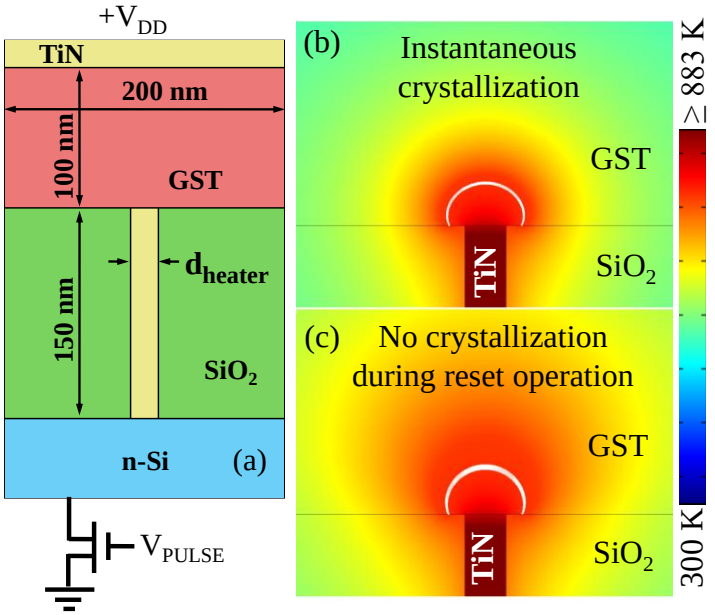

Figure 2. (a) Schematic of a phase change memory (PCM) cell used for simulations. Thermal profile of PCM cells with 10 nm heater diameter at the end of a reset pulse (b) using electrical and thermal conductivity values based on slow measurements and (c) based on exponential extrapolation of electrical resistivity and calculated thermal conductivity (assuming crystallization time >> pulse duration). GST melts as a mushroom in both cases. White lines indicate T_{melt} for GST.

Figure 1. (a) Temperature dependent thermal and electrical conductivities for TiN, (b) thermal boundary conductances, and (c) electrical resistivity (based on slow measurements and exponential extrapolation), (d) thermal conductivity (based on slow measurements and calculated electronic and estimated phonon contributions) , (e) heat capacity accounting for latent heat of fusion (L_f) , and (f) Seebeck coefficient for $Ge_2Sb_2Te_5$. Dashed lines indicate extrapolations. Seebeck coefficient used for TiN is 1 μV/K.

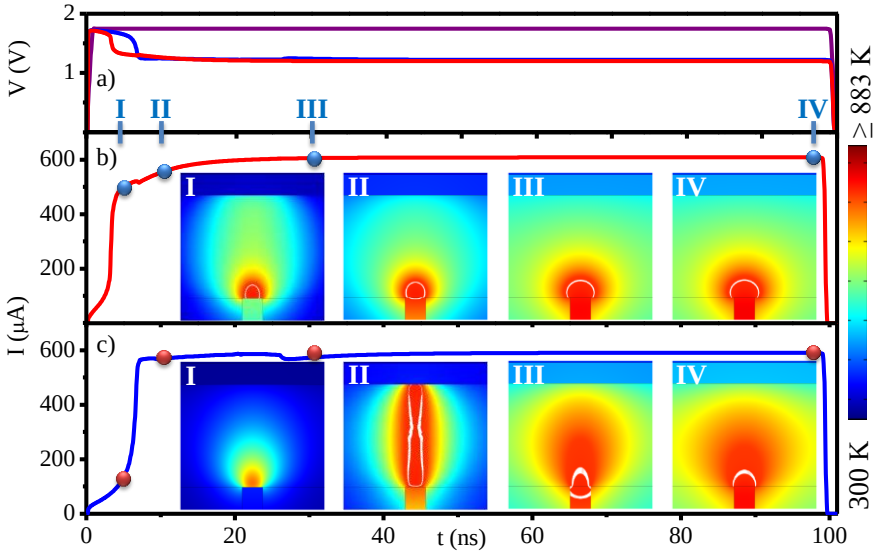

Figure 3. Reset operation for a 20 nm heater diameter PCM cell for instantaneous crystallization and metastable models (100 ns gate pulse). (a) Applied voltage (V_{DD} = 1.75 V) and voltage across the cell. Current through the cell and thermal profiles for the instantaneous crystallization model leading to a molten mushroom (b) and the metastable model, initially melting a filament and finally forming a mushroom during the pulse (c). Time snapshots I, II, III, and IV are taken at 5, 10, 30, and 99 ns respectively.

A Surface-Potential Based Compact Model for GaN HEMTs Incorporating Polarization Charges

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High electron mobility transistors (HEMTs) based on III-nitride semiconductor heterostructures are being actively pursued for high-voltage and high-speed microwave applications [1]. As discrete GaN transistors move towards integration in circuits, a compact model for device operation is highly desirable to aid systematic design. GaN HEMTs differ from Silicon and other III-V FETs through the presence of high density polarization-induced sheet charges at heterostructure interfaces. Till date, no clear method exists to incorporate such polarization charges into compact modeling of HEMTs. We introduce a method for incorporating polarization sheet charges into compact modeling in transistors. The Poisson equation is solved directly with a Dirac-delta function sheet charge at the heterojunction to obtain an analytical equation for the surface potential. This surface potential is then used to calculate the HEMT characteristics. Thus, the results of this work for the first time make an explicit connection between the material properties of the HEMT heterostructure with a surface potential based compact model through the polarization sheet charge. Furthermore, we have extended the intrinsic model by including field-dependent mobility and velocity saturation. The developed model should prove helpful in designing of devices and circuits.

Fig. 1(a) depicts the cross section of a GaN HEMT with a gate barrier of thickness t_b, an unintentionally doped GaN layer of thickness t_{GaN} of doping N_d sitting on a semiinsulating substrate, and source and drain contact regions. The self-aligned device structure has a gate length (= source-drain separation) of L. The regions of interest in the compact model include the GaN and the barrier layers. We denote the local potential in this region as $\psi(x, y)$ with the axes shown in Fig. 1(a). The potential variation along the x direction is retained, and the y direction variation is parameterized in terms of the boundary conditions $\psi(x,0) = 0$ and $\psi(x,L) = V_{ds}$. The local potential is then governed by the Poisson equation,

$$\frac{\partial^2\psi(x)}{\partial x^2} = -\frac{q}{\epsilon_s}\left[p(x) - n(x) + N_d^+ + \sigma_\pi\delta(x - x_0)\right], \quad (1)$$

Where all symbols have their usual meanings. The polarization sheet charge σ_π is explicitly included in the form of a Dirac-delta function located at $x = x_0$, which is precisely the location of the heterojunction. The charge-diagram and the resulting potential are shown schematically in Fig. 1(b) and (c). The potential at the heterojunciton $\psi(x_0) = \psi_s$ is thesurface potential. We note the relation $\sigma_\pi \int_{x_0-\delta}^{\infty}(d\psi/dx)\delta(x - x_0)dx = \sigma_\pi \times d\psi/dx|_{x_0-\delta}$. Here δ is chosen infinitesimally close to the heterojunction, but on the barrier side to include the polarization sheet charge. The potential at the metal gate is $\psi_G = V_{gs}$-V_p $=V_{gp}$, where V_p is the pinch-off voltage. Since there are no charges in the barrier, $d\psi/dx|_{x_0-\delta} = (\psi_s - V_{gp})/t_b$, and Eq.1 may be solved to the closed form,

$$\frac{1}{2}\left(\frac{V_{gp} - \psi_s}{t_b}\right)^2 + \frac{q\sigma_\pi}{\epsilon_s}\left(\frac{V_{gp} - \psi_s}{t_b}\right) + \frac{q}{\epsilon_s}\left[\psi_s N_d + v_t p_0(1 - e^{-\frac{\psi_s}{v_t}}) - v_t N_d e^{-\frac{V}{v_t}}(e^{\frac{\psi_s}{v_t}} - 1)\right] = 0. \quad (2)$$

Eq. 2 is the main result of this work. It is a closed formequation for the surface potential in GaN HEMTs with an explicit appearance of the polarization charge σ_π. The surface potential ψ_s of Eq. 2 depends on the localpotential V, which assumes values $V = 0$ at the source end, and $V = V_{ds}$ at the drain end of the HEMT. To illustrate the dependence of ψ_s on the gate and drain biases in a HEMT, we choose a representative polarization charge $\sigma_\pi = 10^{13}/\text{cm}^2$ at the heterojunction, $N_d = 10^{16}/\text{cm}^3$, t_b = 12 nm, $\epsilon_s = 9\epsilon_0$, and T = 300 K fixes the intrinsic carrier concentration n_i. The resulting surface potential is plotted in Fig. 2(a) as a function of the gate voltage for various values of V. The on- and off-state drain currents are easily obtained with knowledge of the surface potential [4]. Using mobility degradation due to normal electric field and velocity saturation due to high lateral field in the channel, the I-V characteristics can be written into following expression [3], $I_d = I_d^{acc/dep}/(G_{avg}/2).[\sqrt{1+\Gamma^2} + \ln(\Gamma + \sqrt{1+\Gamma^2})/\Gamma]$,where $\Gamma = (\mu_0.\Delta\psi_s)/(v_{sat}.L.G_{avg})$ and $G_{avg} = 1 + a.F_{avg}^2 + b.F_{avg}^{1/3}$ with $F_{avg} = (1/2).[c_b.(V_{gp} - \psi_{savg}) + qN_d t_{GaN}]/\epsilon_s$ and $\psi_{savg} = (\psi_{sS} + \psi_{sD})/2$.

Using the model, we first calculate the intrinsic device characteristics of Al(Ga,In)N/GaN HEMT with constant mobility and without velocity saturation effects as shown in Fig. 2(b). Then we calculate device characteristics with mobility degradation and velocity saturation effects as shown in Fig. 2(c). Fig. 3(a) plots the transfer curves of intrinsic model with constant mobility and with field dependent mobility for drain bias of 4V. The magnitude of current density becomes lower due to mobility reduction and velocity saturation of electrons as compared to intrinsic model. The intrinsic transconductance $g_m = \partial I_d/\partial V_{gs}$ at different V_{gs} are calculated and shown in Fig. 3(b). Note the sharp drop in g_m beyond the peak, and the sub-linear increase of the drain current with gate bias. The model captures most observed properties in GaN HEMTs.

In summary, a compact model for GaN HEMTs that explicitly captures the effect of polarization charges at heterojunctions has been developed. The model should be useful for both microwave as well as digital devices.

[1] Mishra et al, Proc. IEEE, 90, 1022 (2002), [2] Taur et al, Fundamentals of Modern VLSI Devices, 2nd ed. (2009),
[3] Langevelde et al., Physical background of MOS model 11, 2003/00239, [4] Nassar et al., IEEE Trans. on Electron Dev., 56, 1974 (2009).

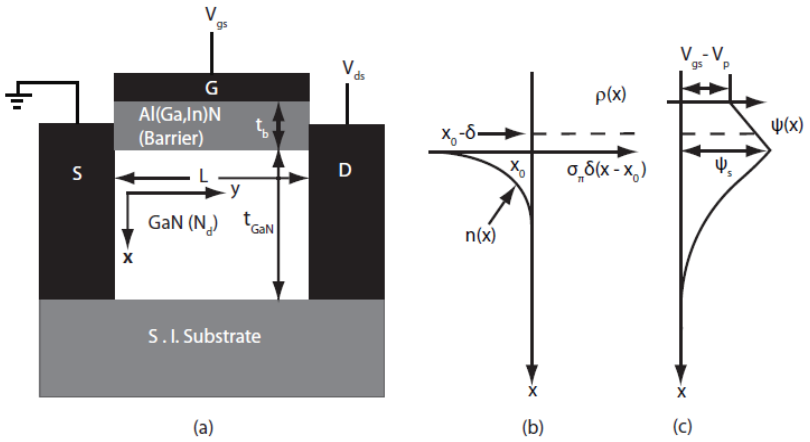


Fig. 1: (a) Al(Ga,In)N/GaN HEMT cross section with relevant parameters. (b) Charge distribution $\rho(x)$ with polarization sheet charge σ_π at the heterojunction and mobile charge $n(x)$. (c) The potential distribution $\psi(x)$. Thepotential at the heterojunction is the surface potential ψ_s

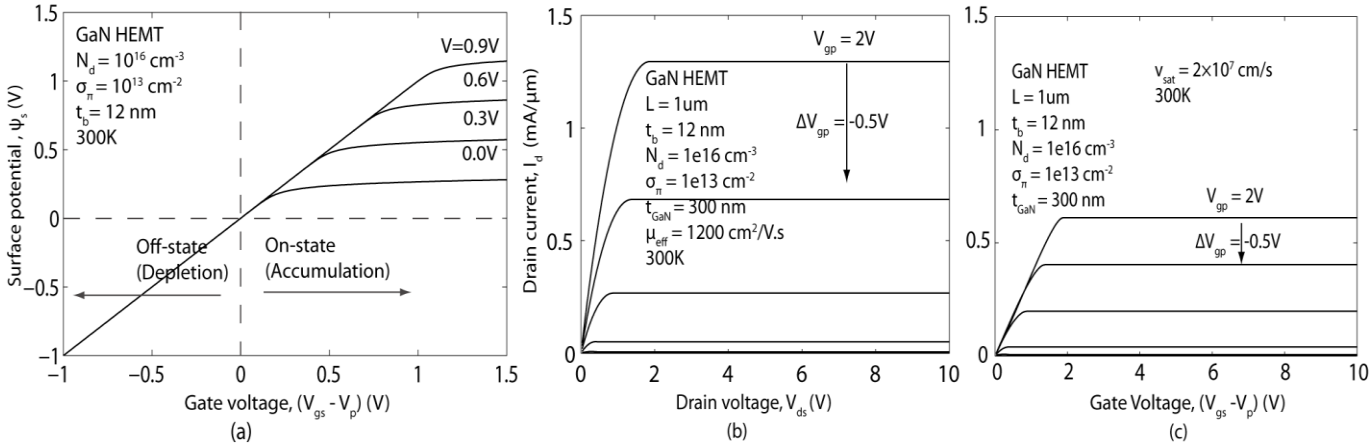


Fig. 2:(a) The surface potential ψ_s as a function of gate voltage for differentlocal channel potentials V depicting the depletion and the accumulation regions, (b) The calculated drain current I_d versus drain voltage V_{ds} for different effective gate voltages $(V_{gs} - V_p)$ for a GaN HEMT without velocity saturation effect, (c) Output characteristics (I_d-V_{ds}) show the degradation of saturation current due to mobility reduction and velocity saturation effects of mobile electrons in the channel.

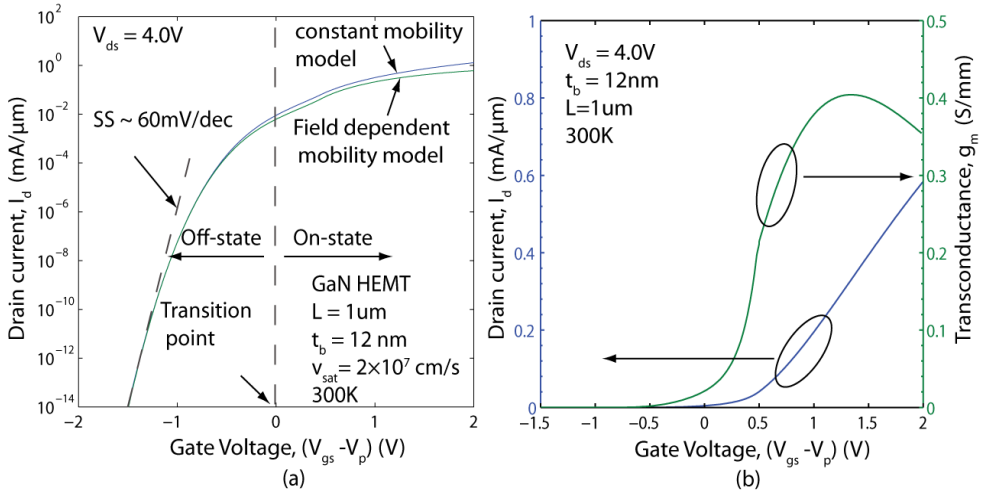


Fig. 3: (a) Calculated transfer curves depicting the drain current versus effective gate voltage, V_{gs} - V_p for drain biases V_{ds} = 4.0V with constant mobility and field dependent mobility of electrons in the channel. Field dependent mobility model shows the drain current reduction than the constant mobility model, (b) The net drain current and transconductance g_m versus V_{gs}-V_p. Transconductance decreases from peak value due to mobility reduction with normal electric field and velocity saturation of electron due to high drain bias is shown based on this model.

Session IV.A (Dean's Hall I)

Wide Bandgap/High Speed Devices

Tuesday AM, June 19th, 2012

Session Chair(s): Dan Green, ONR and Debdeep Jena, University of Notre Dame

8:20 AM IV.A-1
N-polar GaN/InAlN MIS-HEMT with 400-GHz fmax
D. Denninghoff, J. Lu, M. Laurent, E. Ahmadi, S. Keller and U. K. Mishra, Department of Electrical and Computer Engineering, University of California, Santa Barbara, California, USA

8:40 AM IV.A-2
Ultra-thin Body GaN-on-Insulator nFETs and pFETs: Towards III-Nitride Complementary Logic
G. Li, R. Wang, J. Verma, H. Xing, and D. Jena, Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA

9:00 AM IV.A-3
Improved GaN-based HEMT Performance by Nanocrystalline Diamond Capping
T. J. Anderson[1], K. D. Hobart[1], M. J. Tadjer[2], T. I. Feygelson[3], E. A. Imhoff[1], D. J. Meyer[1], D. S. Katzer[1], J. K. Hite[1], F. J. Kub[1], B. B. Pate[1], S. C. Binari[1], and C. R. Eddy, Jr.[1], [1] Naval Research Laboratory, Washington District of Columbia, USA, [2] Universidad Politécnica de Madrid, Madrid, SPAIN and [3] SAIC, Inc., Washington, District of Columbia, USA

9:20 AM IV.A-4
Record low tunnel junction specific resistivity (< 3X10-4 Ocm2) in GaN inter-band tunnel junctions
S. Krishnamoorthy[1], F. Akyol[1], J. Yang[2], P. S. Park[1], R. C. Myers[2,1], and S. Rajan[1,2], [1]Department of Electrical & Computer Engineering, The Ohio State University, Columbus, Ohio, USA and [2]Department of Material Science & Engineering, The Ohio State University, Columbus, Ohio, USA

9:40 AM IV.A-5
Ga_2O_3 Schottky barrier diodes fabricated on single-crystal ß-Ga_2O_3 substrates
K. Sasaki[1,2], M. Higashiwaki[2,3], A. Kuramata[1], T. Masui[4], and S. Yamakoshi[1], [1]Tamura Corporation, Sayama, Saitama, JAPAN, [2]National Institute of Information and Communications Technology, Koganei, Tokyo, JAPAN, [3]PRESTO, Japan Science and Technology Agency, Chiyoda, Tokyo, JAPAN, and [4]Koha Co., Ltd., Nerima, Tokyo, JAPAN

10:00 AM Break

10:20 AM IV.A-6
Quaternary nitride enhancement mode HFET with 260 mS/mm and a threshold voltage of +0.5 V
N. Ketteniss[1], B. Reuters[1], B. Holländer[2], H. Hahn[1], H. Kalisch[1], and A. Vescan[1], [1]GaN Device Technology, RWTH Aachen University, Aachen, GERMANY
and [2]Forschungszentrum Juelich GmbH, Juelich, GERMANY

10:40 AM IV.A-7
Methods for Attaining High Interband Tunneling Current in III-Nitrides
T. A. Growden, S. Krishnamoorthy, D. N. Nath, A. Ramesh, S. Rajan, and P. R. Berger, Department of Electrical and Computer Engineering, The Ohio State University, Columbus, Ohio, USA

11:00 AM IV.A-8
Experimental Demonstration of a Wafer-Bonded Heterostructure based Unipolar Transistor with In0.53Ga0.47As Channel and III-N Drain
S. Lal[1], J. Lu[1], B. Thibeault[1], S. P. Denbaars[2], and U. K. Mishra[1], [1]Department of Electrical and Computer Engineering and [2]Materials Department, University of California, Santa Barbara, California, USA

11:20 AM IV.A-9
Electrical Evidence of Disorder at the SiO2/4H-SiC MOS Interface and its Effect on Electron Transport
S. Swandono, A. Penumatcha, and J. A. Cooper, School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana, USA

11:20 AM IV.A-10
Asymmetric Dual-Grating Gate InGaAs/InAlAs/InP HEMTs for Ultrafast and Ultrahigh Sensitive Terahertz Detection
S. Boubanga-Tombet[1], Y. Tanimoto[1], T. Watanabe[1], T. Suemitsu[1], W. Yuye[2], H. Minamidev[2], H. Ito[2], V. Popov[3], and T. Otsuji[1], [1]Research Institute of Electrical Communication, Tohoku University, Aoba-Ku, Sendai , JAPAN, [2]RIKEN Sendai, Aoba-ku, Sendai, JAPAN, and [3]Institute of Radio Engineering and Electronics (Saratov Branch), Saratov, RUSSIA

N-polar GaN/InAlN MIS-HEMT with 400-GHz f_{max}

D. Denninghoff, J. Lu, M. Laurent, E. Ahmadi, S. Keller and U. K. Mishra
Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106 USA
Tel: (805) 893-8956, Fax: (805) 893-8714, Email: denninghoff@ece.ucsb.edu

This paper reports 400-GHz f_{max} using a tall-stem T-gate on an N-polar GaN/InAlN MIS-HEMT grown by MOCVD. This is the highest reported f_{max} value to date for an N-polar GaN HEMT and is among the highest values for all GaN HEMTs.

GaN-based HEMTs have tremendous potential for high-frequency operation due to the high electron velocity and high sheet charge density. The high-frequency performance of both N-polar and Ga-polar HEMTs has increased rapidly as the device gate length, source-drain spacing, and gate-channel spacing have decreased [1]-[4]. Nitrogen-polar HEMTs have advantages over Ga-polar HEMTs including a built-in back barrier for improved electron confinement, extremely low contact resistance [5], and greater flexibility in scaling the gate-channel distance as the 2DEG charge is determined by the back barrier instead of the top barrier.

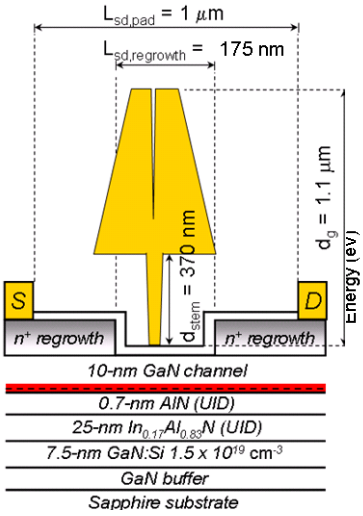
Many high-frequency performance results recently reported in the literature were obtained with extremely small rectangular gates [2]-[4]. These breakthrough f_T results have demonstrated that GaN-based HEMTs are capable of achieving frequency performance beyond what has been theorized. However, due to the high gate resistance of these rectangular-gate devices, the f_{max} performance is nearly an order of magnitude lower than f_T. A less-resistive and more process-intensive T-gate [1], [6] is required for the high f_{max} that is essential for many applications. A properly designed T-gate minimizes gate resistance (R_g) and parasitic gate-drain capacitance (C_{gd}), both of which would otherwise degrade f_{max}. The devices in this work were fabricated using the tall-stem T-gate process reported in Ref. 6.

The epitaxial structure of the devices reported in this work is given in Fig. 1, including a 10-nm GaN channel with an InAlN back barrier and 4.5-nm high-temperature MOCVD SiN gate dielectric. The growth details are similar to those already reported [7]. As InAlN can be grown lattice-matched to GaN, it provides a strain-free barrier layer, and the higher polarization charge of InAlN relative to AlGaN allows higher 2DEG sheet densities. The sheet resistance as measured by TLM structures for the devices in this work is 280 Ohm/sq, which resulted in a device on-resistance (R_{on}) of 0.29 Ohm-mm for L_g = 100 nm and 175-nm source-drain spacing. This R_{on} is the lowest reported for a non-self-aligned GaN HEMT and matches the lowest reported R_{on} for a self-aligned GaN HEMT [1]. The saturated drain current at V_{gs} = 0 V is 1.9 A/mm as shown in Fig. 2 with excellent saturation and pinch-off characteristics. The transfer curves show an extrinsic dc transconductance of 323 mS/mm at V_{ds} = 3 V and extremely low 28.9 mV/V drain-induced barrier lowering (DIBL)—defined as change in threshold voltage per drain bias.

As shown in Fig. 3a, the device with W_g = 2x12.5 µm and L_g = 100 nm obtained a peak f_T of 144 GHz at V_{ds} = 8 V and V_{gs} = -4.5 V, and the dc and RF g_m for this bias was 480 and 600 mS/mm, respectively. The small-signal S-parameters of this device were measured at biases up to V_{ds} = 8 V and V_{gs} = -4.5 V without breaking down. Thus, the gate-drain distance of ~50 nm supported a voltage of ~12.5 V. Fig. 3a also shows the f_{max} values of 377, 384, and 400 GHz for V_{gs} = -4.5, -4.25, and -4 V, respectively, at V_{ds} = 8 V. An additional device with W_g = 2x75 µm and L_g = 90 nm (L_g verified by SEM) achieved a peak f_T of 176 GHz, which results in an excellent f_T*L_g product of 15.8 GHz*µm. The lower f_{max} of 277 GHz for this device is caused by the higher gate resistance due to the longer gate width.

Fig. 5 shows that peak f_T and f_{max} both increase with increasing drain bias. To understand this dependence, RF g_m, C_{gs}, and C_{gd} were extracted from S-parameter measurements for each bias point. Fig. 5 shows that RF g_m increases with increasing drain bias while C_{gs} and C_{gd} decrease. This implies an increase in electron velocity as drain bias increases. Further improvement in f_T is expected on future devices as L_g is reduced. In addition to the challenge of yielding sub-100-nm gates, a properly designed T-gate at these dimensions is a significant challenge and is currently under development.

Funding from DARPA NEXT program (Dr. John Albrecht) and ONR (Dr. Paul Maki) is gratefully acknowledged. A portion of this work was performed in the UCSB Nanofabrication Facility, a member of the NSF-funded NNIN.
[1] K. Shinohara *et al. IEDM Tech. Dig.*, pp. 453-6, Dec. 2011. [2] Nidhi *et al., IEEE DRC Tech. Dig.*, p. 141-2, June 2011. [3] D. Lee *et al. IEDM Tech. Dig.*, pp. 457-60, Dec. 2011. [4] R. Wang *et al. IEEE EDL* vol. 32, no. 7, July 2011. [5] S. Dasgupta *et al., Applied Physics Letters*, vol. 96, no. 14 (143504), 5 Apr. 2010. [6] D. Denninghoff *et al. IEEE DRC Tech. Dig.*, p. 269-70, June 2011. [7] D. Brown *et al. IEEE EDL* vol. 31, no. 8, Aug. 2010.



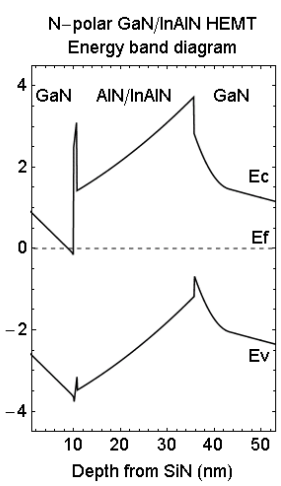
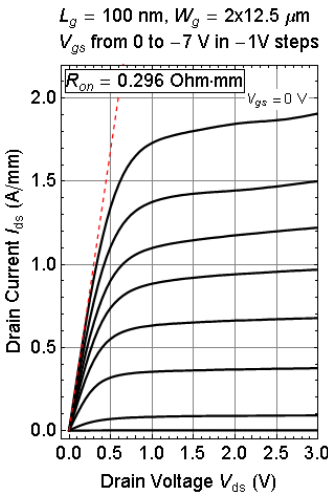


Fig. 1. Epitaxial structure and energy band diagram for N-polar GaN/InAlN MIS-HEMT grown by MOCVD on an off-axis sapphire substrate. The GaN channel is 10 nm and the MOCVD SiN gate dielectric is 4.5 nm. The gate is centered between highly doped ohmic regions formed by selective-area MBE regrowth. The sheet resistance of the GaN channel is 280 Ohm/sq as measured by TLM structures.



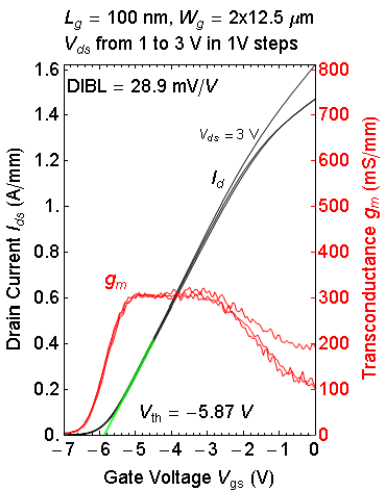


Fig. 2. Output and transfer characteristics for the tall-stem N-polar GaN/InAlN MIS-HEMT with 175-nm source-drain spacing and 100-nm gate length. 1.9 A/mm I_{dss} (at V_{gs} = 0 V) and 0.29 Ohm-mm on-resistance and excellent saturation and pinch-off characteristics are demonstrated. 323 mS/mm peak extrnsic g_m at V_{ds} = 3 V and near-zero drain-induced barrier lowering.

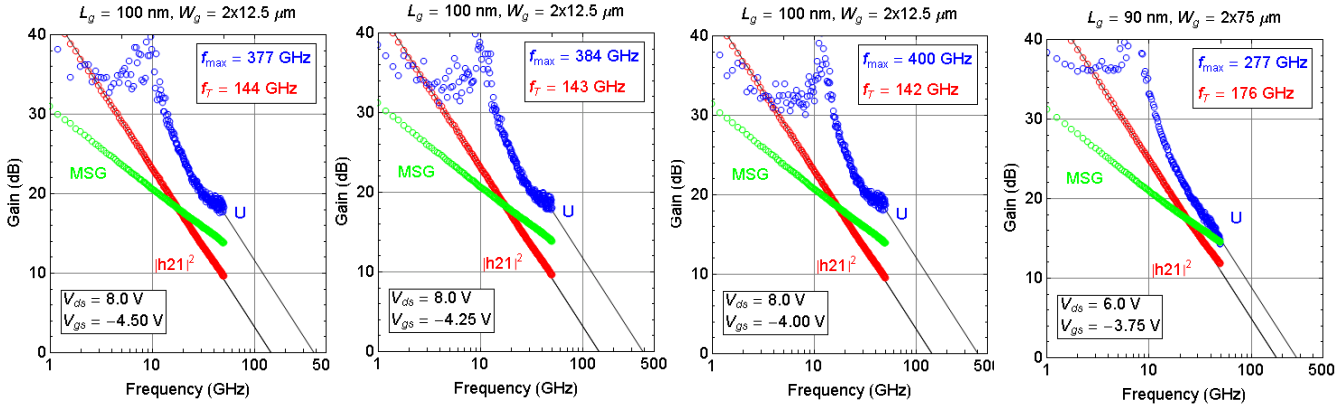


Fig. 3a. Small-signal RF gains for 2x12.5 μm device with L_g = 100 nm at V_{ds} = 8 V as a function of gate bias. The peak f_T is 144 GHz and the peak f_{max} is 400 GHz. This f_{max} is the highest reported to date for an N-polar GaN HEMT and among the highest for all GaN HEMTs.

Fig. 3b. Small-signal RF gain of 2x75 μm device with f_T*L_g product of 15.8 GHz μm

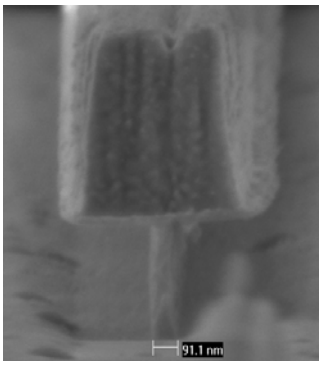


Fig. 4. SEM image of the L_g = 90 nm T-gate with a 370-nm-tall stem and 1.1 μm total gate height. The tall stem reduces the T-top parasitic capacitance.

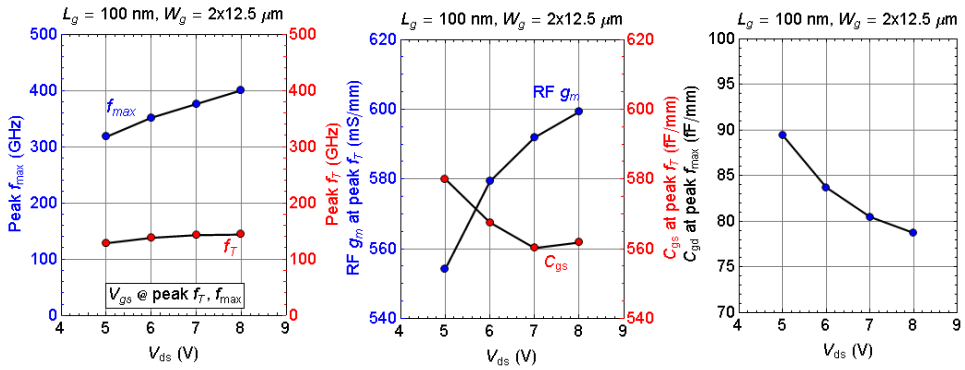


Fig. 5. Peak f_T and f_{max} for the 2x12.5-μm-wide device as a function of drain bias. Both f_T and f_{max} increase as drain bias increases. This increase is due to the increase in RF g_m and the decrease in C_{gs} and C_{gd} as drain bias increases. Further improvement in f_T is expected for L_g < 90 nm.

Ultra-thin Body GaN-on-Insulator nFETs and pFETs: Towards III-Nitride Complementary Logic

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Ultra-thin body (UTB) devices with tight electrostatic and quantum confinement of charge carriers have been well developed in highly scaled silicon CMOS technology. For adopting such advanced methods, III-nitrides can benefit immensely from epitaxial AlN as the substrate platform, in contrast to conventional GaN-based substrate platform. With its large polarization charge, wide bandgap and large band offsets, AlN induces the maximal carrier densities while providing the best confinement for nitride channels of all compositions. Such devices stand also to benefit from the symmetry of electronic polarization: high density *hole gases* can be generated in much the same way as the high density 2DEG in GaN HEMTs, thus enabling p-channel FETs on the same material platform in a logical manner. The AlN/GaN heterojunctions where mobile carriers are located are epitaxial, and excellent transport properties are expected as opposed to the rougher oxide-semiconductor interfaces. Furthermore, AlN is an excellent electrical insulator but simultaneously an excellent thermal conductor, which makes it highly attractive to act as back-barrier and to lower junction temperatures in high power devices by efficient heat dissipation. There have been reports on relaxed GaN n-channel FETs (nFETs) on AlN [1, 2] and III-nitride based p-channel field effect transistors (pFETs) [3, 4]. All the prior work uses relaxed GaN as the channel, and strained GaN channels on AlN have not been explored before. In this work we demonstrate UTB GaN nFETs [5] and pFETs on AlN grown by molecular beam epitaxy (MBE) as the first step towards complementary logic and high power applications.

Fig.1 shows the schematic heterostructures and band diagrams of (a) conventional AlN/GaN HEMTs, (b) AlN/GaN/AlN nFETs and (c) GaN/AlN pFETs. The wide bandgap AlN serves as back barrier. The nFETs consist of strained GaN channels sandwiched in strain-free AlN barriers, and pFETs are derived from nFETs by simply removing the top AlN barrier. At this stage, Mg doping is used in the channel for holes, a step that can be dispensed of in the future.

High-resolution X-ray diffraction measurements on the nFET sample shown in Fig.2 (a) clearly show the strained GaN channel peak, and the inset AFM image shows smooth surface morphology. Abrupt binary GaN/AlN heterojunction of the pFET sample is observed in Z-contrast scanning TEM image in Fig.2 (b). The schematic device structure is shown in Fig.3 for (a) nFETs and (b) pFETs. MBE regrowth of heavily Si-doped n^+-GaN has been used for ohmic contacts for nFETs. The pFET employ Schottky gates of Ni/Au directly deposited on the p-type GaN channel without annealing. In the pFET heterostructure, we measure by Hall effect mobile hole gas density of $\sim 5 \times 10^{13}$ cm^{-2}, enable by polarization. This is the highest hole gas density measured in *all* semiconductor heterostructures to date.

Complementary device performance of a 2.1-μm-long nFET and a 2.4-μm-long pFET is shown in Fig. 4. In these preliminary demonstrations, the nFETs show ~3 order of magnitude of current modulation, but due to leakage at Schottky gate and high hole density, the pFET is not completely pinched off at V_{GS} = +2 V as shown in Fig.4 (a). The transfer characteristics are shown in (b) linear scale and (c) semi-log scale. The capacitance-voltage (C-V) curves measured at 1 MHz are shown in Fig. 5. For nFET heterostructures a circular Schottky diode is measured while for pFET heterostructures the gate-to-source capacitor of a 2.6-μm-long pFET is used. This first demonstration of polarization-induced complementary FET behavior, in spite of its current shortcomings, paves the way for vast improvement by scaling and gate stack advances. Temperature dependent family IVs of a 2.6-μm-long pFET are plotted in Fig. 5 for (a) T = 77 K, (b) T = 300 K and (c) T = 400 K. The drain is biased up to 50 V with L_{sd} = 5.2 μm. The drive current and transconductance increase as temperature is lowered, as signatures of polarization-induced p-type doping.

In conclusion, we report novel complementary UTB strained GaN nFETs and pFETs on an AlN substrate platform. The symmetry of polarization fields is exploited to create high-density mobile electron and hole gases in strained channels on the same substrate. Low hole mobilities lead to asymmetric device characteristics, a problem that can be addressed effectively by exploiting the epitaxial strain. The device results provide promising ways for scaling in vertical direction (i.e. perpendicular to channel direction) for III-nitride heterostructures, and a compelling case for complementary logic applications.

This work was supported in part by the DARPA (Dr. J. Albrecht, the NEXT program, HR0011-10-C-0015), by AFOSR (Drs. K. Reinhardt and J. Hwang) and by ONR (Dr. P. Maki).

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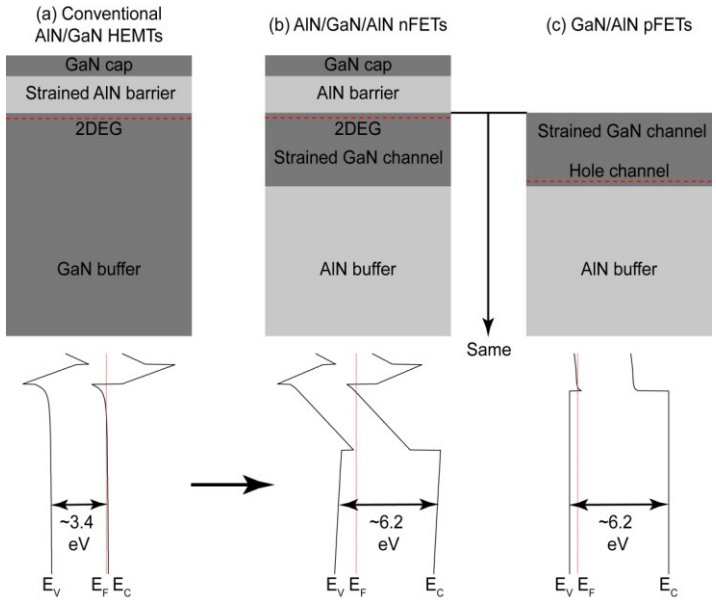

Fig.1 Schematic heterostructures and band diagrams of (a) conventional AlN/GaN HEMTs, (b) AlN/GaN/AlN nFETs and (c) GaN/AlN pFETs.

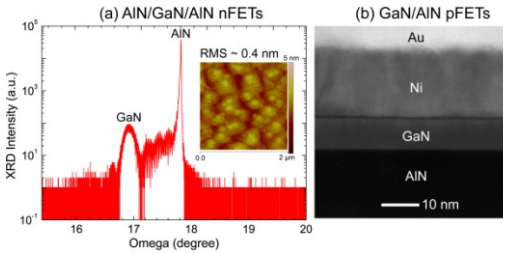

Fig.2 (a) High-resolution XRD and AFM (inset) scans on nFETs; (b) Z-contrast STEM image of pFETs under the gate.

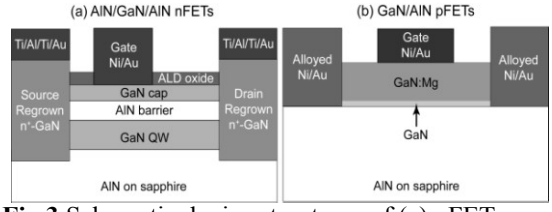

Fig.3 Schematic device structures of (a) nFETs and (b) pFETs.

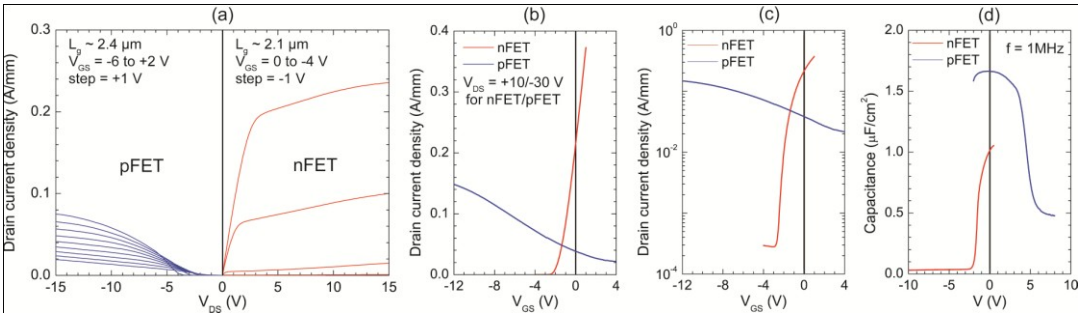

Fig.4 (a) Output characteristics; (b) linear plots of transfer curves; (c) semi-log plots of transfer curves; (d) C-V plots of a circular Schottky diode for n-channel, and gate-to-source capacitor of a pFET for p-channel.

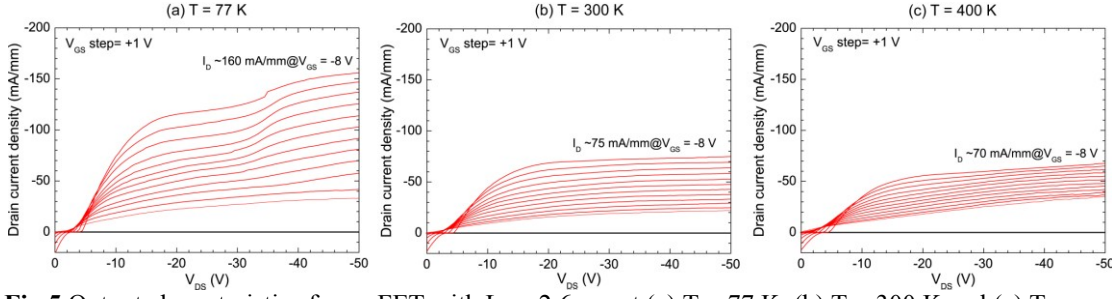

Fig.5 Output characteristics for a pFET with L_g = 2.6 µm at (a) T = 77 K, (b) T = 300 K and (c) T = 400 K.

Improved GaN-based HEMT Performance by Nanocrystalline Diamond Capping

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As a wide-bandgap semiconductor, gallium nitride (GaN) is an attractive material for next-generation power devices. To date, the capabilities of GaN-based high electron mobility transistors (HEMTs) have been limited by self-heating effects (drain current decreases due to phonon scattering-induced carrier velocity reductions at high drain fields). Despite awareness of this, attempts to mitigate thermal impairment have been limited due to the difficulties involved with placing high thermal conductivity materials close to heat sources in the device. Heat spreading schemes have involved growth of AlGaN/GaN on single crystal or CVD diamond, or capping of fully-processed HEMTs using nanocrystalline diamond (NCD). All approaches have suffered from reduced HEMT performance or limited substrate size. Recently, a "gate after diamond" approach, shown in Figure 1, has been successfully demonstrated to improve the thermal budget of the process by depositing NCD before the thermally sensitive Schottky gate and also to enable large-area diamond implementation [1].

The "gate after diamond" approach employs the deposition of the diamond heat spreading layer on either the bare AlGaN surface or a thin nucleation dielectric/passivation layer (eg. 10 nm PECVD SiN_X) after completion of the mesa and ohmic processes, but before the gate metal step. An O_2-based plasma etch is used to recess etch the diamond in the gate region before metal deposition. A reference HEMT was fabricated from the same wafer, and was passivated with 100nm PECVD SiN_X in the same process sequence as the NCD-capped device ("gate after nitride"). Hall measurements on van der Pauw structures were used to monitor the 2DEG throughout the fabrication processes to ensure that NCD deposition and processing were not damaging the device. The results are summarized in Table I, with the "covered" and "etched" terminology referring to the van der Pauw patterns that either remained coated with NCD (or SiN_X) or were exposed to the gate recess etch. Based on these results, it is clear that both the diamond deposition and gate recess processes had minimal impact on the 2DEG. The data shown are from AlGaN/GaN HEMT structures on SiC substrates, though the process is currently being extended to InAlN/GaN heterostructures.

Electrical characterization of a NCD-capped device has yielded device performance that is comparable to the non-capped reference device, as shown in Figure 2(a) and (b). The diamond-capped device appeared to demonstrate improved DC I-V characteristics in most key performance areas, as indicated in Table II. Of particular importance are the improved on-resistance, saturation current, and transconductance, and reduced off-state current and gate leakage, which are significant performance metrics for power switches. Furthermore, diamond-capped devices demonstrated improved forward blocking characteristics, manifested by the reduced off-state leakage current and a nearly 200V improvement in breakdown voltage in forward blocking mode, as shown in Figure 2(c). RF devices with 3 μm source-drain spacing were also fabricated, which yielded small signal f_T = 6 GHz and f_{MAX} = 23 GHz for a 1.5 μm gate length device

Electroluminescence (EL) imaging, shown in Figure 3, was used to gain some insight into the breakdown performance of these devices. At low bias conditions, a more intense emission was observed in NCD-capped devices despite the lower gate and drain leakage currents were lower. Experiments are in-progress to quantify the nature of this emission, however this result implies that the emission is related to the heat or field-spreading effects of the diamond layer. This work was supported by NRL and ONR (P. Maki).

[1] M.J. Tadjer, T.J. Anderson, K.D. Hobart, T.I. Feygelson, J.D. Caldwell, C.R. Eddy, Jr, F.J. Kub, J.E. Butler, B.B. Pate, J. Melngailis, 'Reduced self-heating in AlGaN/GaN HEMTs Using Nanocrystalline Diamond Heat Spreading Films." *IEEE Electron Dev. Lett.* Vol. 33, No. 1, 23-25 (2012)

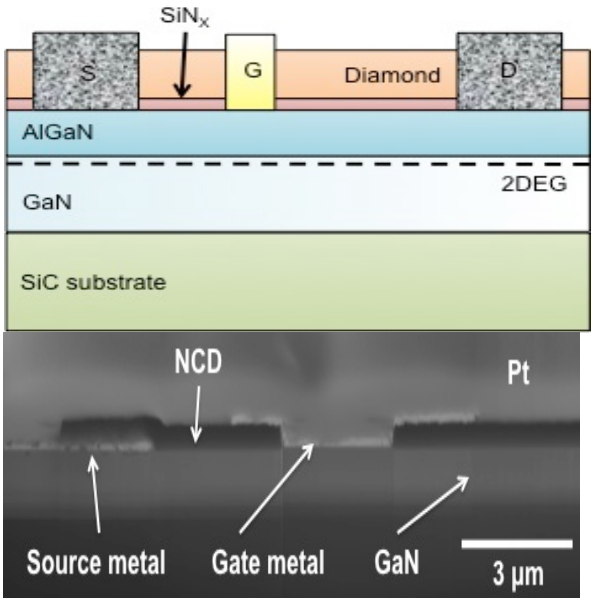

Figure 1. Schematic and FIB cross section of diamond-capped AlGaN/GaN HEMT. Pt was deposited in the FIB to protect the surface during ion milling.

Table I: Hall data for reference and diamond-capped HEMTs

		R_{SH} (Ω/□)	μ (cm²/V-s)	N_{SH} (cm⁻²)
NCD before gate HEMT	covered	488	1260	1.02×10^{13}
	etched	478	1280	1.02×10^{13}
Reference HEMT	covered	574	1270	9.22×10^{12}
	etched	533	1220	8.92×10^{12}

Table II: Device performance metrics for reference and diamond-capped HEMTs

	R_{ON} (Ω-mm)	I_{SAT} (A/mm)	I_{OFF} (A/mm)	V_T	$g_{m\,max}$ (S/mm)
NCD before gate HEMT	11.9	0.445	1.0×10^{-5}	-3.36	0.127
Reference HEMT	14.6	0.380	9.5×10^{-5}	-3.07	0.114

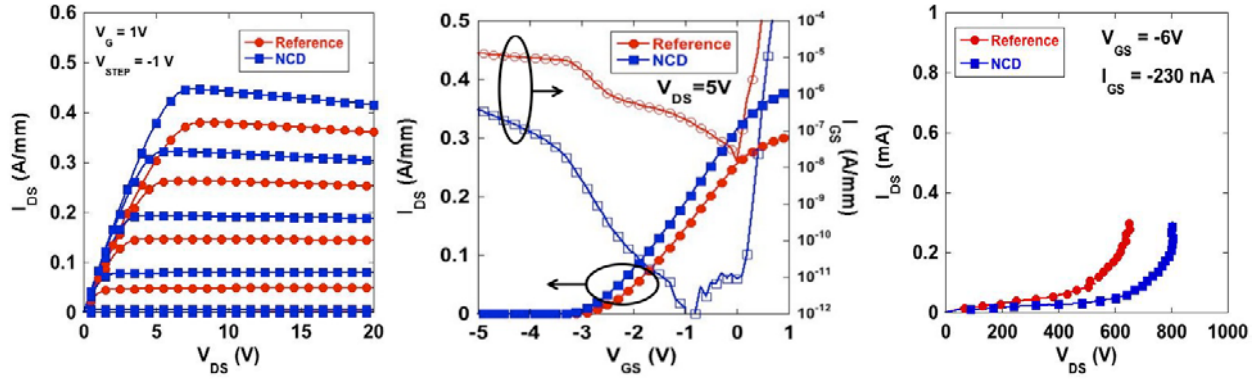

Figure 2. a) V_G-I_{DS} curves, b) V_{DS}-I_{DS} curves, and c) forward blocking characteristics for reference and diamond-capped devices

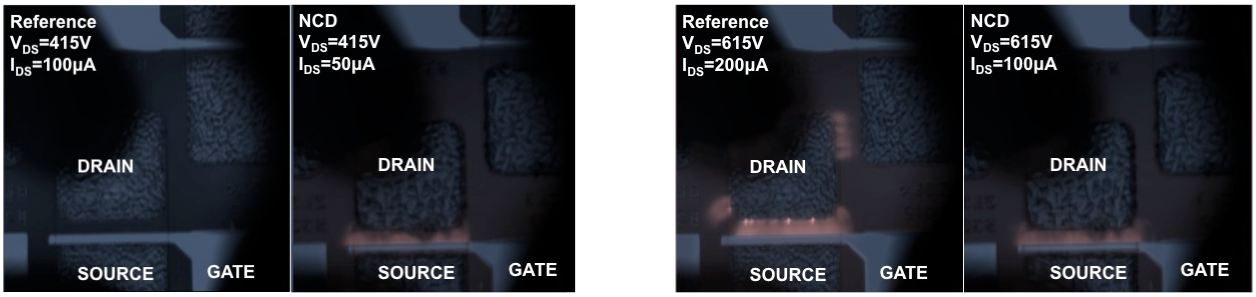

Figure 3. False-color EL images of reference and diamond-capped devices at V_{DS} = 415V and 615V. V_{GS} = -6V in all images.

Record low tunnel junction specific resistivity (< $3X10^{-4}$ Ωcm^2) in GaN inter-band tunnel junctions

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Introduction: We report on the design, fabrication, and characterization of record high efficiency inter-band tunnel junctions in GaN. We have achieved tunnel junction specific resistivity values as low as 3 $X10^{-4}$ Ωcm^2 by using polarization engineered GaN/InGaN/GaN tunnel junctions. An alternate approach of using rare earth nitride (GdN) nano-islands embedded in degenerately doped GaN p n junction has resulted in tunnel junction specific resistivity of $2.7X10^{-3}$ Ωcm^2. This is the first report of mid gap states assisted tunneling in GaN.

Efficient tunnel junctions can enable a wide range of electronic and optoelectronic devices, especially in III Nitrides material system, which is ubiquitous for blue, green light emitters and also solid state UV emitters. Polarization in this material system has been engineered to create huge band bending over smaller distances in nitride heterostructures by utilizing the high field due to the polarization charges that are induced at the polar heterointerfaces [1, 2]. A p-GaN/InGaN/n-GaN backward diode demonstrated earlier showed record high current density of 118 A/ cm^2 at a reverse bias of 1 V by utilizing a thin high indium composition InGaN barrier sandwiched between degenerately doped GaN p n junction[3]. Forward tunneling has also been demonstrated by appropriate design of the GaN/InGaN tunnel junctions and the first observation of NDR at room temperature has also been reported [4].

Polarization enhanced tunneling: In this work, a polarization engineered GaN/InGaN/GaN tunnel junction has been incorporated in a p-GaN down N- polar GaN p n junction to replace the p type material with more conductive n type material. 4 nm of 25% InGaN inserted between degenerately doped GaN aligns the conduction and valence bands of GaN, owing to the high polarization charge dipole at the GaN/InGaN interface, resulting in a high current density even close to zero bias across the tunnel junction. As the p n junction is forward biased, the GaN/InGaN tunnel junction is reversing biased. Electrons from the valence band of p GaN tunnel into n GaN, leaving a hole behind as shown in Fig.3. This is equivalent to tunnel injection of holes from a n type GaN contact into the p type material. Hole injected into the p type material diffuses to the n type GaN region when the p n junction is forward biased. The forward turn on voltage (Fig. 4) of this device is the sum of the voltage drop across the p n junction and that of the reverse biased tunnel junction. The forward turn on of this tunnel junction incorporated device indicates negligible voltage drop across the reverse biased tunnel junction as desired. The overall resistance of the device in forward bias is found by fitting the forward characteristics, to be 7 X 10^{-4} Ωcm^2. This overall resistance extracted includes the contact resistance, series resistance in the p GaN and n GaN regions, and the tunnel junction resistance. The top contact resistance is measured separately using TLM method, and is found to be 4 X 10^{-4} Ωcm^2. yielding the specific tunnel junction resistivity to be as low as < 3 X 10^{-4} Ωcm^2.

GdN nano-islands enhanced tunneling: The second approach to enhance tunneling in III nitrides is to introduce mid gap states in a GaN p^+ n^+ junction. GdN nano-islands embedded in GaN p n junctions with high doping density were grown along N face and Ga face orientations (Fig. 5) using Plasma Assisted Molecular Beam Epitaxy (PAMBE). Both N face and Ga face devices with GdN inserts showed increased current density as compared to standard p+/n+ junction, suggestive of enhanced recombination tunneling due to GdN nano-islands. At a reverse bias of 1 V, the Ga polar GaN/GdN/GaN carried 72.3 A/cm^2, while similar structure along the N polar orientation had a comparable current density of 75 A/cm^2, showing a weak dependence on polarity, as shown in Fig.6. Tunnel injection of holes from a n type GaN top contact into the p type material has been achieved using GaN/GdN TJ (Fig. 7). Negligible voltage drop across the tunnel junction is observed during the forward bias operation of the p n junction as shown in Fig.8. In comparison, the structure without GdN, which relies on tunneling across degenerately doped p n junction (conventional approach), a 2 V drop across the tunnel junction is required to inject holes into the p n junction. Tunnel junction specific contact resistivity of GdN based tunnel junction has been de-embedded from the overall device resistance to be 3 X 10^{-3} Ω cm^2.

In summary, ultra low tunneling specific resistances (3 $X10^{-4}$ Ωcm^2) have been obtained in GaN, inspite of the large band gap, by two different approaches, resulting in state-of-the-art III Nitride tunnel junctions. This is also the first report of efficient tunnel injection of holes in III- Nitrides. Such low resistance tunnel junctions achieved, demonstrates the potential of tunnel junction incorporation a variety of electronic and optoelectronic applications, in specific, for tunnel injection of holes to alleviate the problems with p type material in III- Nitrides.

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[2] J. Simon et.al., Phys. Rev. Lett. 103, (2009).
[3] S. Krishnamoorthy et.al., Appl. Phys. Lett.,97,203502 (2010).
[4] S. Krishnamoorthy et.al., Appl. Phys. Lett.,99,233504 (2011).

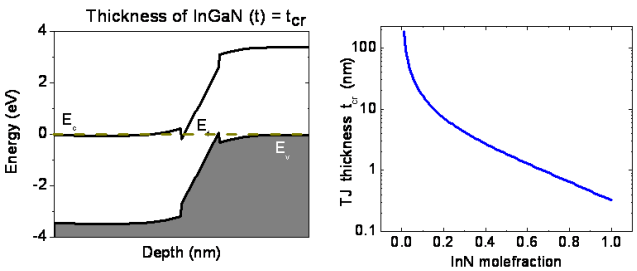

Figure 1 : (a) Band diagram of a GaN/InGaN/GaN tunnel junction with thickness of InGaN t = t_{cr} to align the valence and conduction bands , and (b) Calculation of t_{cr} for different InGaN compositions.

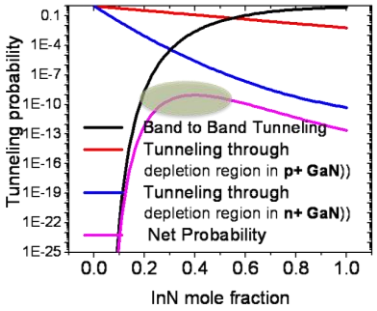

Figure 2: Net Tunneling probability evaluated for the tunnel junction with the maximum tunneling probability region encircled.

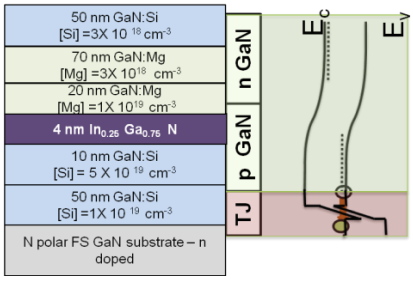

Figure 3: Epitaxial stack of a TJ incorporated p n junction along N polar orientation and the band diagram showing tunnel injection of holes.

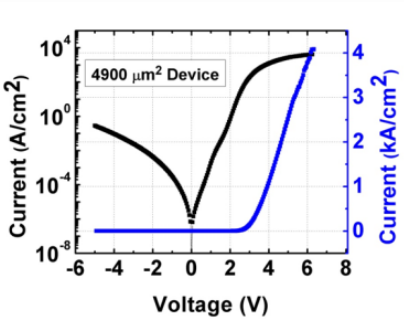

Figure 4 : The IV characteristics of the stack shown in Fig. 3. The voltage drop across the TJ is negligible, and the specific contact resistivity (< 3 X 10^{-4} Ωcm^2) can be evaluated from the forward characteristics by subtracting the contact and series resistances.

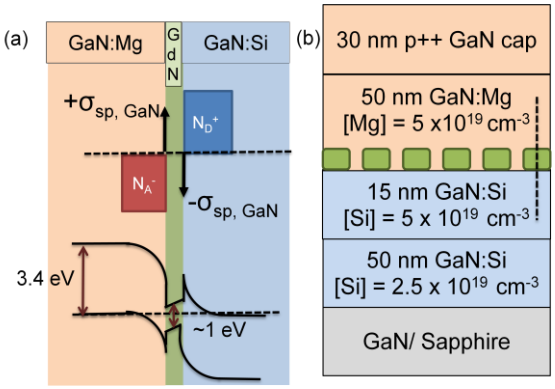

Figure 5: Band diagram of tunnel junctions with GdN nano-island inserts. In Ga polar orientation, the field in GdN is against the depletion field. However, with very high doping, this effect is not significant. Both N polar and Ga polar structures have similar depletion width, and hence similar current density is expected.

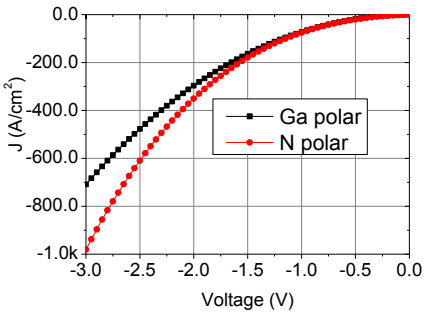

Figure 6: Comparasion of reverse characteristics of GaN/GdN TJ along Ga polar and N polar orientation. Similar reverse current density is observed close to zero bias.

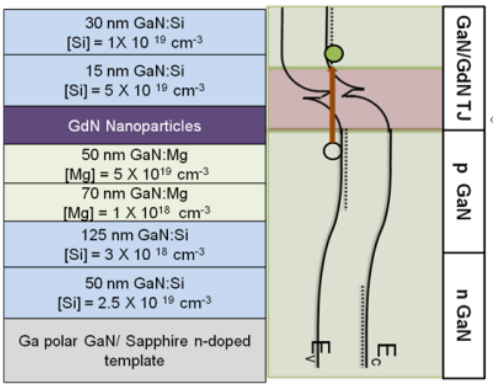

Figure 7: Epitaxial stack of a GdN/GaN TJ incorporated p n junction along Ga polar orientation and the band diagram showing tunnel injection of holes.

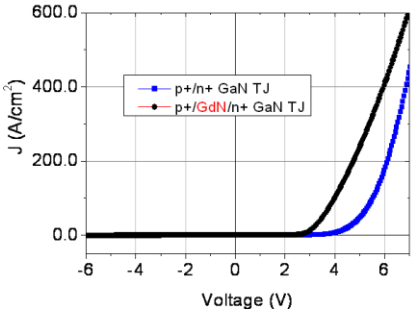

Figure8: The IV characteristics of the stack shown in Fig. 7. The voltage drop across the TJ is negligible, and the specific contact resistivity (< 3 X 10^{-3} Ωcm^2) is extracted.

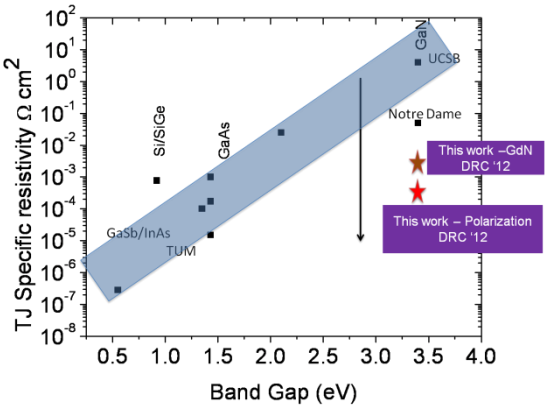

Figure 9: Plot of TJ specific resistivity obtained in different material systems. Stars show the **record low resistivity (< 3 X 10^{-4} Ωcm^2)** obtained in this work, in spite of the large band gap of GaN.

Ga_2O_3 Schottky barrier diodes fabricated on single-crystal β-Ga_2O_3 substrates

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β-Ga_2O_3 has an extremely large bandgap of 4.8-4.9 eV and excellent material properties for power device applications, as summarized in Tab. 1. The breakdown field of β-Ga_2O_3 is estimated to be 8 MV/cm, from the relation between the band gaps and breakdown fields of other major semiconductors. Another important feature is that large single-crystal β-Ga_2O_3 substrates can be fabricated with melt-growth methods such as floating-zone (FZ) and edge-defined film-fed growth (EFG). Figure 1 shows a photograph of a 2-inch-diameter single-crystal β-Ga_2O_3 wafer fabricated by the EFG method. The wafer size depends on the production machine size. Therefore, we consider that Ga_2O_3 is a very attractive new semiconductor for power device applications because of its material properties and ease of mass production. However, it has not been studied to any extent up to now.

We have been working on a new project to develop Ga_2O_3 power devices and recently succeeded in fabricating Ga_2O_3 transistors on single-crystal Ga_2O_3 substrates for the first time [1,2]. The devices exhibited good characteristics such as high breakdown voltage (V_{BR}) (~250 V), low off-state drain leakage current (5 μA/mm), and high on/off ratio (~10^4), even though they had a simple circular MESFET structure. These characteristics clearly indicate the potential of Ga_2O_3 power devices. In this study, we fabricated and characterized Ga_2O_3 Schottky barrier diodes (SBDs) on single-crystal β-Ga_2O_3 substrates made from melt; these devices will be key components in power electronics.

We used unintentionally-doped β-Ga_2O_3 substrates prepared from bulk grown by the FZ method. The bulk crystal was cut along the (010) plane. The substrate thickness was 600 μm. The surface of the substrate was atomically flat after chemical mechanical polishing with a root-mean-square surface roughness of 0.11 nm. The crystal quality of the substrate was excellent, as represented by a narrow XRD rocking curve peak with an FWHM of 30 arcsec and low dislocation density of less than 1×10^4 cm^{-2}. The substrate showed *n*-type conductivity due to unintentionally-doped Si, which was incorporated in the Ga_2O_3 powder source (5N). The electron density (*n*) was uniform in the depth direction, but a little distributed in a range of 3×10^{16}-1×10^{17} cm^{-3} in the plane, as evaluated by the capacitance-voltage measurement.

Figure 2 shows a cross-sectional schematic illustration of the β-Ga_2O_3 SBD structure fabricated on the single-crystal β-Ga_2O_3 substrate. First, circular Schottky contacts with a diameter of 100 μm were fabricated on the front side of the substrate as anode electrodes by standard photolithography patterning, Pt/Ti/Au evaporation, and lift off. Next, a reactive ion etching (RIE) treatment using a mixture gas of BCl_3 and Ar was performed on the back side, followed by cathode metal evaporation (Ti/Au). We found that the RIE treatment changes the electrode property from Schottky to ohmic and significantly decreases the contact resistance [1].

Figures 3(a) and (b) show the forward current density-voltage (*J-V*) characteristics of two different Ga_2O_3 SBDs with $n=3\times10^{16}$ and 5×10^{16} cm^{-3}, which were at different places on the same substrate. They showed excellent ideal factors of 1.04-1.06, indicating the high crystal quality of the Ga_2O_3 substrate and good Schottky interface property. On-resistances (R_{on}) were high, 7.85 and 4.30 mΩcm^2, and they were larger than those of the state-of-the-art devices made from other semiconductors. However, these high values were simply because of the small conductivity of the substrate due to the low *n*. Therefore, they can be much improved simply by using the usual SBD structure consisting of an n^--Ga_2O_3 epitaxial layer on an n^+-Ga_2O_3 substrate. Figure 4 shows the reverse *J-V* characteristics. The reverse V_{BR} values were about 150 and 115 V for $n=3\times10^{16}$ and 5×10^{16} cm^{-3}, respectively, which were reasonably high for the *n*. Note that all the densities were simply derived by dividing the measured values by the area of the anode metal.

In conclusion, we fabricated Ga_2O_3 SBDs on a single-crystal β-Ga_2O_3 (010) substrate. The devices showed good device characteristics such as an ideal factor close to 1.0 and reasonably high reverse V_{BR}. These results indicate that Ga_2O_3 SBDs have comparable or even more potential than Si and typical widegap semiconductors SiC and GaN have for power device applications. This work was partially supported by NEDO and JST PRESTO programs, Japan.

[1] M. Higashiwaki et al., Appl. Phys. Lett. **100**, 013504 (2012), [2] K. Sasaki et al., Appl. Phys. Exp. **5**, 035502 (2012).

Table 1: Material properties of major semiconductors and Ga_2O_3.

	Si	4H-SiC	GaN	Diamond	β-Ga_2O_3
Band gap (eV)	1.1	3.3	3.4	5.5	4.8-4.9
Electron mobility (cm^2/(Vs))	1,500	1,000	1,200	1,800	300
Breakdown field (MV/cm)	0.3	3.0	3.3	10	8
Dielectric constant	11.8	10	9.5	5.5	10
Baliga's FOM (low freq.)	1	570	860	21,000	3,200

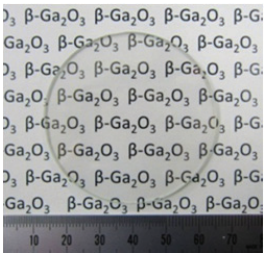

Fig. 1: Single-crystal 2-inch-diameter β-Ga_2O_3 (010) substrate fabricated by the EFG method.

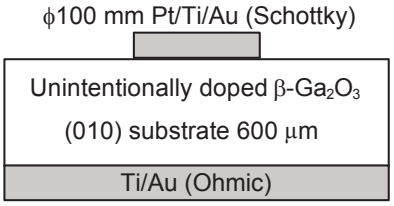

Fig. 2: Cross-sectional schematic illustration of Ga_2O_3 SBD.

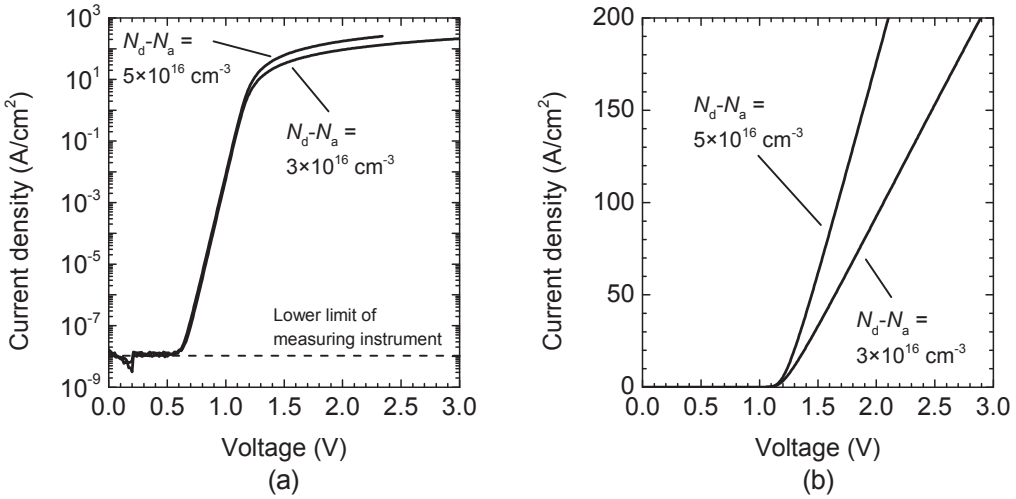

Fig. 3: Forward *J-V* characteristics of Ga_2O_3 SBDs in (a) single logarithmic and (b) linear plots.

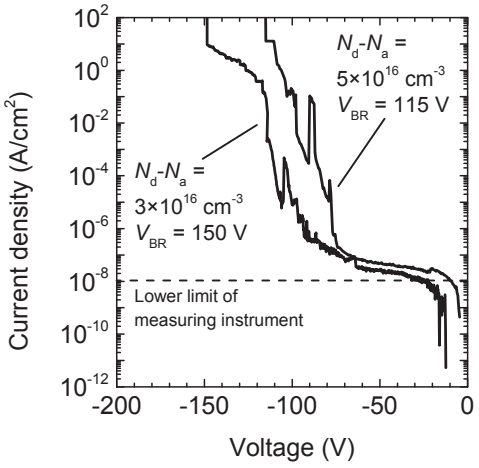

Fig. 4: Reverse *J-V* characteristics of Ga_2O_3 SBDs.

Quaternary nitride enhancement mode HFET with 260 mS/mm and a threshold voltage of +0.5 V

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The demand for robust and fail-safe GaN-based enhancement mode (e-mode) heterostructure field effect transistors (HFET) is high. Several different approaches for e-mode HFET fabrication have been demonstrated already [1, 2]. Most approaches deplete the channel by either manipulating the surface potential or the thickness of the barrier layer. Here, we demonstrate a new approach for the heterostructure design following the idea to reduce the interface charge itself by applying a quaternary barrier layer with rather low polarization.

The e-mode HFET presented consist of a GaN buffer and a quaternary barrier layer, whose composition and thickness have been chosen carefully to result in an e-mode device. Special attention in the design process has been paid to the barrier-inherent polarization to reduce the total amount of polarization-induced interface charges. Additionally, a capping layer for carrier concentration enhancement in the access region has been applied to reduce the series resistance of the devices.

The schematic cross section of our devices is shown in Fig. 1. The barrier layer of all devices consists of $Al_{0.20}In_{0.05}Ga_{0.75}N$ which is expected to have nearly the same polarization as the GaN buffer (indicated as "low P" in Fig. 1). The three devices only differ in their capping layers. Whereas for device A, the barrier layer material has been applied also as capping layer, devices B and C have capping layers with higher polarization, 8 nm of $Al_{0.44}In_{0.05}Ga_{0.51}N$ for device B ("high P") and an 8 nm layer with a graded composition for device C. The grading is realized by increasing the Al content from 20 % to 50 % while keeping the In content constant at 5 %. The corresponding band diagrams and the carrier concentration for the as-grown layer stacks are given in Fig. 2. The simulation indicates that for device B, a second channel might be formed at the interface between capping and barrier layer. For device C, the formation of this second channel is suppressed by the graded capping layer, which results in a conduction band diagram similar to a modulation-doped FET [3]. For all devices, a chlorine-based recess etch was used prior to Ni/Au gate metal evaporation. The recess etch depth was adjusted to 11 nm to ensure complete removal of the capping layer. An AFM picture of the recessed gate area is shown in Fig. 3.

The results of Hall and van der Pauw measurements for the as-grown and unrecessed samples are shown in Fig. 4. The low-polarization sample A yields a very low sheet carrier concentration of only 1.8×10^{12} cm^{-2} with a still acceptable mobility above 1300 cm^2/Vs indicating that polarization matching has been almost achieved. The heterostructures with carrier enhancement capping layers show the expected higher carrier concentrations in the range of $4 - 5.7 \times 10^{12}$ cm^{-2} and high mobility. Fig. 5 shows the transfer characteristics of the unpassivated devices for $V_{ds} = 10$ V. The characteristics of device A are severely affected by the high series resistance in the access regions, whereas devices B and C are quite similar. A closer look at the off-state gate current reveals that device B has a 3 to 5 times higher gate leakage, which could be due to a lateral contact of the gate to the second electron channel in the access region predicted by the simulation. Still, the gate and drain current in off-state are well below 10^{-6} mA/mm for all devices. The threshold voltage lies in the range of 0.5 – 0.6 V. As the devices are Schottky-gated, the gate diode turn-on limits the device performance at approx. $V_{gs} = 1$ V. Nevertheless, an outstanding on-off ratio of more than 8 orders of magnitude is achieved for the devices B and C. To enable device operation at even higher gate voltages, a gate dielectric should be applied. Experiments with this topic are currently ongoing.

Finally, the devices have been passivated with 120 nm SiN by plasma enhanced CVD. An increase in gate and drain leakage can be observed and finds its origin in surface or interface conductivity of the not fully optimized SiN. Nevertheless, for all devices the extrinsic transconductance has increased due to further carrier concentration enhancement in the access region by the passivation. Best performance is achieved for sample B, yielding a maximum extrinsic transconductance of 260 mS/mm, which is among the highest reported for a 1 µm gate length e-mode HFET.

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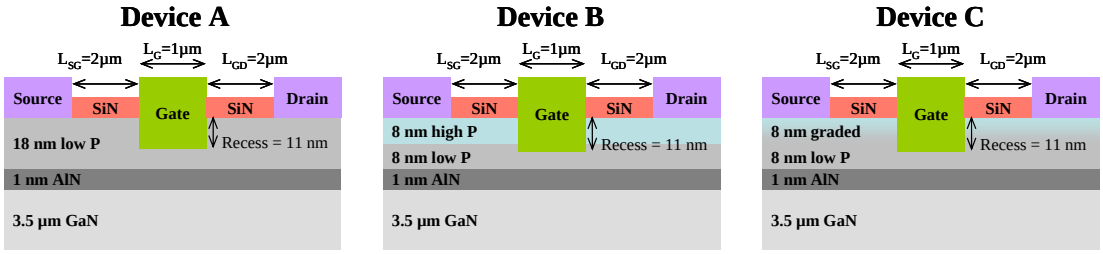

Fig. 1. Schematic cross section of the investigated devices. SiN passivation layer has a thickness of 120 nm.

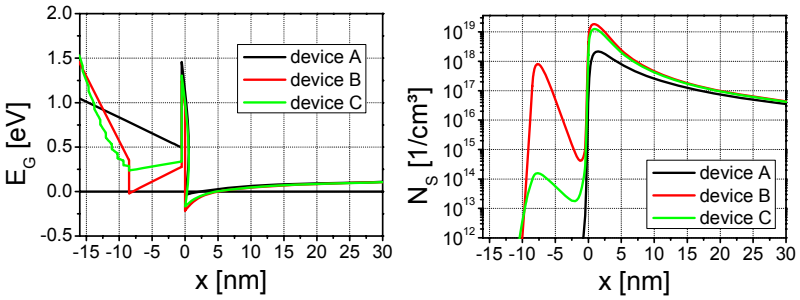

Fig. 2. Calculated conduction band diagram for the investigated devices (left)
Calculated electron density N_S (right)

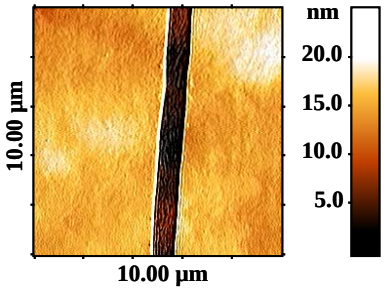

Fig. 3. AFM scan of gate recess

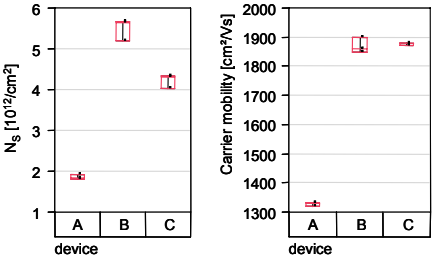

Fig. 4. Hall and van der Pauw measurements of the as grown, unrecessed wafers.

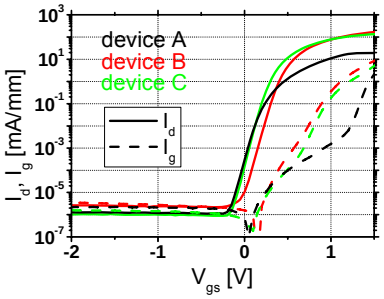

Fig. 5. Transfer characteristics of the unpassivated devices, V_{ds} = 10 V

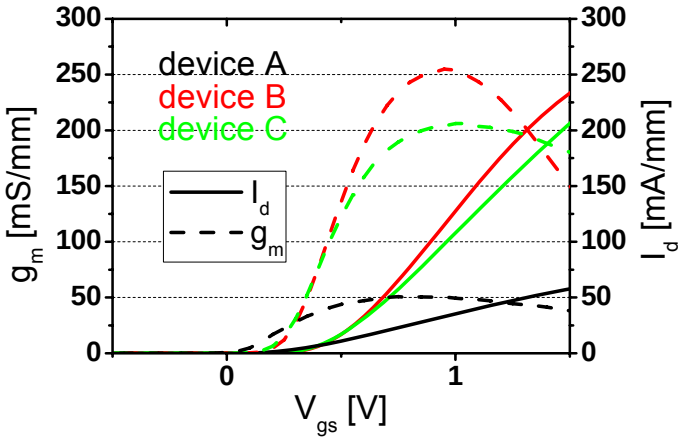

Fig. 6. Transfer characteristics of the passivated devices. V_{ds} = 10 V

Methods for Attaining High Interband Tunneling Current in III-Nitrides

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III-Nitride based tunneling devices have generated a great deal of interest due to their ability to operate at very high powers/current and elevated temperatures. Additionally, with the increasing interest for making GaN-based photovoltaics, the need for efficient interband tunneling in multi-junction solar cells will be a necessity too. But, to date, due to the nitride's large bandgap and lack of very high bulk doping capabilities, it has proved very difficult to create III-Nitride interband tunnel diodes operating at high current densities. One solution is to use a fairly high concentration of indium in the central tunnel junction to decrease the bandgap and thereby exponentially increase the tunneling probability, while also making use of the spontaneous and piezoelectric polarization charge available in the nitrides to supplement the creation of two quantum wells adjacent the tunnel junction, thereby creating a resonant interband tunneling diode (RITD).

Multiple GaN/InGaN/GaN RITDs were designed, fabricated, and tested. The device stack shown in Fig. 1(a) displays the growth layer-by-layer, of RITD01. By using an N-polar GaN substrate a very high composition InGaN can effectively be grown. Outside of the doped InGaN layers, AlGaN outside barriers were placed to increase the quantum confinement. On either side of the AlGaN barriers, heavily doped caps were placed to promote low-resistance ohmic-like contacts and charge injection. Additionally, Fig. 1(b) shows the device stack for RITD02 which implemented the use of δ-doping to exaggerate the band bending effects and sheet carrier concentration induced by the polarization effects at the heterointerfaces.

Tunneling across a narrow junction is highly dependent upon the availability of both carriers and empty energy states on either side of the junction. By increasing the depth of the quantum wells, as well as enhancing the quantum confinement, we can drastically improve the tunneling probability. The band diagrams shown in Fig. 2 are an illustration of RITD01 with and without AlGaN outside barriers. Carrier confinement in the conduction band is enhanced by a 0.38 eV additional band offset for the quantum well with the AlGaN barrier added, and a 0.09 eV enhancement in QW confinement occurs in the valence band. During forward bias, the QW confined states on either side of the junction will align in energy and interband tunneling will occur. Consequently, deeper quantum wells allow for an increased density of states within the QW, leading to greater tunneling current.

Initial tests showed poor contacts with very low currents and no NDR. But, after cycling the forward sweep multiple times on the same device, the contact essentially self-annealed and a burn-in was achieved, resulting in good ohmic behavior with drastically higher currents. The four sweeps seen in Fig. 3 are immediately following the self-anneal. For each sweep, the PVCR of the NDR decreased drastically, and after the fourth sweep it was nonexistent. Every device tested on this sample exhibited a very similar pattern. Additionally, as has been the case in many nitride-based tunneling diodes, hysteresis was observed. The reverse sweeps shown in the inset of Fig. 3 did not display any NDR, but were very similar in shape and magnitude. The hysteresis in conjunction with the vanishing NDR in the forward sweeps is most likely due to donor-like hole traps found close to the valence band edge near the tunnel junction interface [1]. However, if the reverse sweeps extended beyond a critical voltage, the NDR would reappear in subsequent forward sweeps, suggesting that the traps became depleted. For RITD02 the δ-doping created an increase in the depth of the quantum wells, and thus a further increase in the peak tunneling current density was recorded, rising from ~20 kA/cm^2 to ~40 kA/cm^2, although there was a drastic decrease in the PVCR. Additionally, the forward sweeps shown in Fig. 4a exhibited a much more stable curve. Finally, Fig. 4b displays that in the reverse there are NDR-like effects, which up to this point has rarely been exhibited in nitride based interband tunneling diodes.

In conclusion, the authors have reported an increase in forward interband tunneling current density from 17.7 A/cm^2 [2] to 39.8 kA/cm^2 by applying outside AlGaN confinement barriers and δ-doping to a common structure. Some of the devices still exhibit hysteresis effects caused by traps, but some seem to display less of an effect, which needs to be studied further to provide stability. Optimization of the barrier thickness and Indium composition must also be performed to continue to push the peak current density up in value

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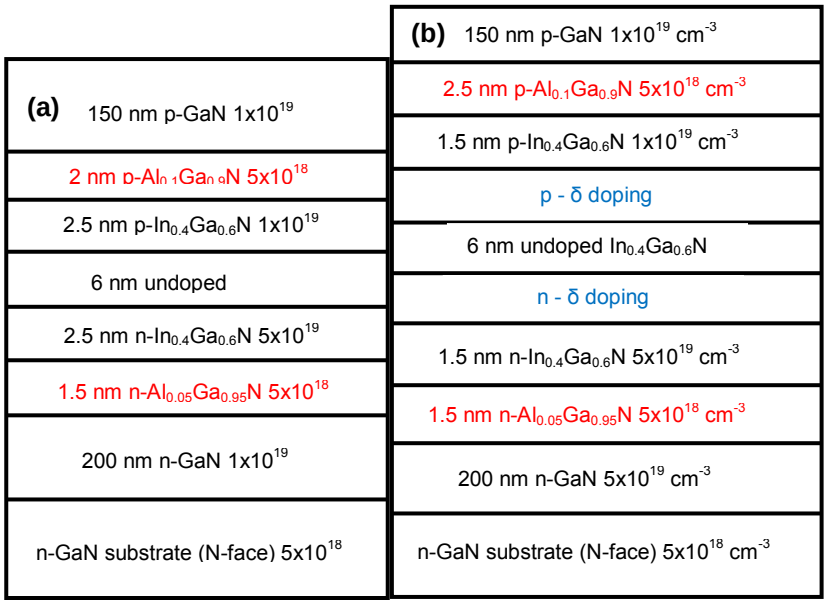

Figure 1: (a) Schematic of RITD01 with outside AlGaN barriers. (b) Schematic of RITD02 with outside AlGaN barriers as well as delta doping layers.

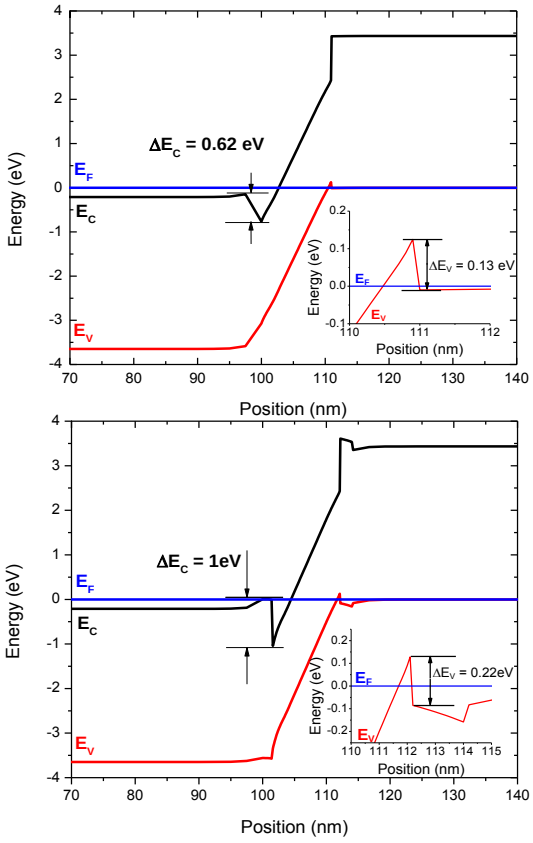

Figure 2: (a) The calculated band diagram of a device without AlGaN outside barriers. (b) The calculated band diagram of RITD01 with AlGaN outside barriers included. The conduction band and valence band (inset) QW offsets are illustrated for clarity.

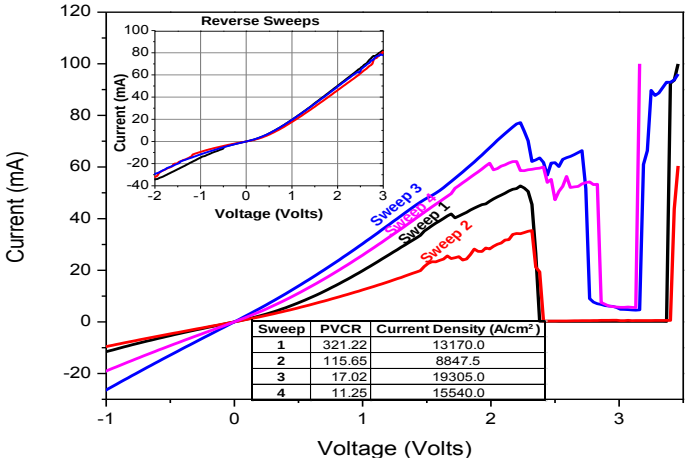

Figure 3: The IV curves for 4 subsequent tests located on RITD01. The top left inset shows 3 reverse sweeps on the same device. The bottom inset displays the relative PVCRs and current densities.

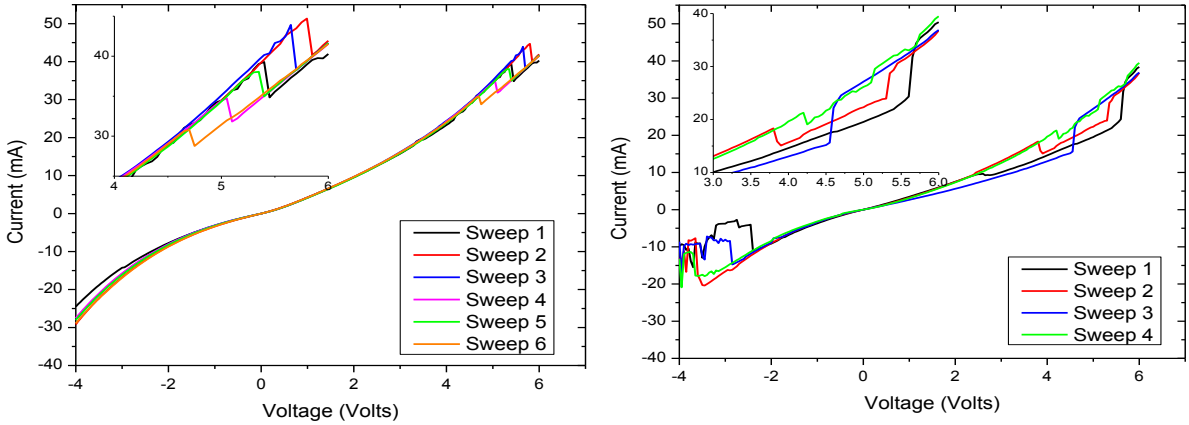

Figure 4: (a) The forward sweep IV curves for RITD02. (b) The reverse sweep IV curves for RITD02, which are displaying NDR-like behavior.

Experimental Demonstration of a Wafer-Bonded Heterostructure based Unipolar Transistor with $In_{0.53}Ga_{0.47}As$ Channel and III-N Drain

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We report the first demonstration of a fully functional wafer-bonded current aperture vertical electron transistor (BAVET). A maximum drain current (I_d) of 29 mA and transconductance (g_{m_d}) of 7.4 mS at a V_{gs} = 0 V is measured for a device with a width of (75×2) μm and an aperture length (L_{ap}) of 8 μm.

Motivated by the goal of designing a transistor with both ultra-high frequency and power density characteristics, an alternative device design concept in the form of a BAVET was developed [1]. The device concept is based on forming a heterojunction between a narrow band-gap semiconductor like III-Arsenide (III-As) and a wide band-gap semiconductor like III-Nitride (III-N). Due to a large lattice mismatch between the two material systems, direct wafer-bonding is used to form the desired heterostructure. The operation of a BAVET is based on a current aperture vertical electron transistor (CAVET) [2]. For an ideal BAVET device, electron conduction starts at the source electrode in the InGaAs channel. It then follows a vertical path to the III-N drain layer through a narrow conductive opening called an aperture (denoted by L_{ap} in Fig. 1). The vertical current conduction is confined to the aperture by selectively creating implant-induced isolation regions, called the current blocking layer (CBL) (see Fig. 1). The overlap between the gate and CBL (denoted by L_{go} in Fig. 1) is the effective gate-length performing channel modulation in a BAVET. A Ga-polar III-N template comprising of an *n*+ GaN/*n*- GaN/*n*- $In_{0.1}Ga_{0.9}N$ structure is wafer-bonded to the III-As template consisting of an *n*+ $In_{0.53}Ga_{0.47}As$/*i* $In_{0.52}Al_{0.48}As$/*n*- $In_{0.53}Ga_{0.47}As$ field-effect transistor structure. The polarization-induced barrier at the InGaN-GaN interface is mitigated by employing δ-doping at the interface. The III-As and III-N layer structures, the design optimizations and the fabrication process for a BAVET are described in detail in [3].

An essential requirement to achieving ideal current saturation characteristics in a BAVET is to eliminate the vertical leakage currents through the CBL (see Fig. 1) [3]. For the devices discussed herein, the measured ratio of electron current through the aperture (L_{ap}= 4 μm) and the CBL (L_{ap} = 0 μm) devices is ~ 10^4 at a V_{ds} = 12 V (see Fig. 2). The DC characteristics of a BAVET exhibit current saturation characteristics in drain (I_d) and source (I_s) currents (see Fig. 3(a)). Channel pinch-off is observed in I_s vs. V_{ds} curves at a threshold voltage (V_{th}) = - 5.4 V. The measured V_{th} is within ~ 6% of the theoretical value. This demonstrates that the presence of a non-ideal wafer-bonded interface is not detrimental towards enforcing the gate-control in the channel required for an ideal device behavior. Fig. 3(b) shows that the peak drain-current transconductance (g_{m_d}) is adversely affected by the gate-drain leakage (I_{gd}), when compared to the peak source-current transconductance (g_{m_s}). To investigate the origin of I_{gd}, a device called the split-gate BAVET is fabricated with the dimension of gate metallization restricted to the L_{go} regions as opposed to a conventional solid-gate BAVET where it extends over L_{ap} + (2 x L_{go}) (see Fig. 4(a), (b)). Contrary to expectation, a split-gate BAVET exhibits higher gate leakage (I_g) and weaker gate control of the channel in the I_g and I_s vs. V_{gs} characteristics, respectively, in comparison to a solid-gate device (see Fig. 4(c), (d)). This indicates that the high electric field at the drain-side of the L_{go} region contributes to the increase in I_{gd} in a BAVET (see Fig. 4(b)). In a solid-gate BAVET, the presence of a Schottky-gate over the aperture acts as a field-plate which reduces I_{gd} at a given V_{gd} and effectively enhances the gate-drain breakdown voltage in comparison to the split-gate device. The weak pinch-off behavior in the I_s-V_{gs} characteristics of a split-gate device is observed to be independent of the L_{go} dimension (see Fig. 5). To investigate lack of pinch-off in I_s, Drain-Current Injection method [4] is used to measure the dependence of applied V_{gs} on I_s and V_{ds} characteristics while injecting a constant I_d (I_{d_inject}). In Fig. 6(a), the I_s vs. V_{gs} curves exhibit a deviation in the $\Delta I_s/\Delta V_{gs}$ slope when V_{gs} is made more negative, which in effect prevents the channel turn-off. To maintain a constant I_{d_inject}, the decrease in $\Delta I_s/\Delta V_{gs}$ causes a drop in the measured V_{ds} (see Fig 6(b)). The drop in V_{ds} is observed to have a weak dependence on the applied ΔV_{gs}. This indicates that in the high-V_{gd} region of the channel, the impact-ionization effect dominates over the gate-breakdown phenomenon, and thus adversely affects the pinch-off in I_s. In summary, a novel wafer-bonding based III-As/III-N unipolar transistor is demonstrated to work as a conventional transistor for the first time. Future work will require a wide band-gap gate dielectric to improve the transistor characteristics.

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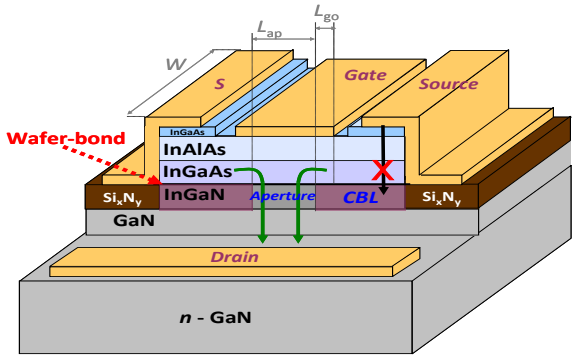

Fig. 1: Three-dimensional schematic of a solid-gate BAVET. The path of electron conduction through the aperture is shown by the green arrows. The leakage path through CBL is shown by a black arrow. The specified dimensions are the aperture width – W, the aperture length – L_{ap} and the gate-CBL overlap – L_{go}.

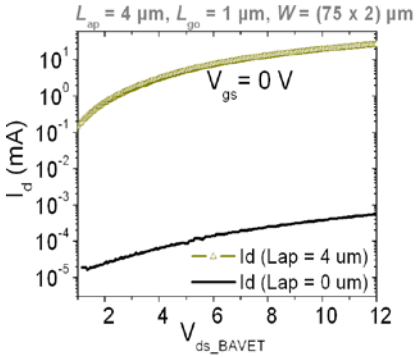

Fig. 2: Three-terminal I_d-V_{ds} measurement on BAVETs with L_{ap} = 4 µm and L_{ap} = 0 µm showing a comparison of aperture conductivity and current blocking properties of CBL, respectively.

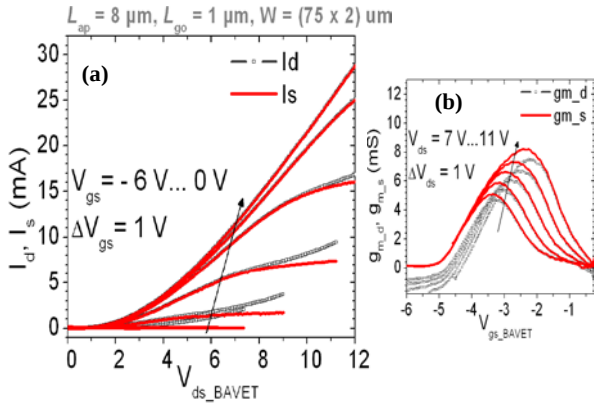

Fig. 3: (a) Transfer characteristics of a solid-gate BAVET showing channel modulation in the I_d and I_s vs. V_{ds} measurements. **(b)** Transconductance for the drain current (g_{m_d}) and source current (g_{m_s}) vs. V_{gs} with maximum g_{m_s} = 8.2 mS and g_{m_d} = 7.4 mS at a V_{ds} = 11V.

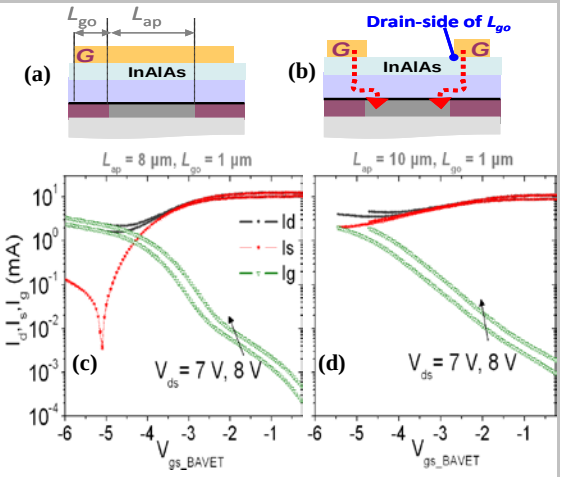

Fig. 4: Cross-sectional schematics of **(a)** solid-gate (L_g = L_{ap} + 2 x L_{go}), and **(b)** split-gate (L_g = 2 x L_{go}) BAVETs. The gate-drain leakage path near the drain-edge of the gate is shown by the dashed red arrows. I_g, I_s, I_d vs. V_{gs} characteristics of **(c)** a solid-gate BAVET showing a channel pinch-off, and **(d)** a split-gate BAVET showing a higher I_g and a poor I_s pinch-off.

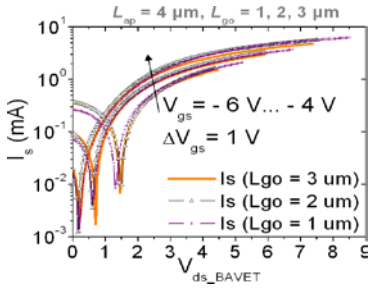

Fig. 5: I_s-V_{ds} characteristics for split-gate BAVETs with different L_{go} dimension measured for V_{gs} varying from -6 to -4 V.

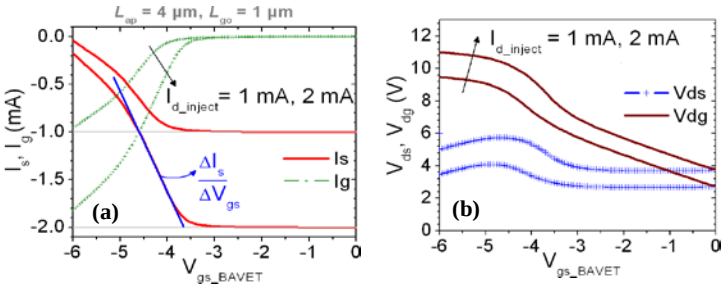

Fig. 6: Drain-Current Injection method measurements while injecting a constant I_d (two sets of measurements done with I_d = 1 mA and 2 mA) for a solid-gate BAVET. **(a)** I_s, I_g vs. V_{gs} characteristics of the BAVET. The slope ($\Delta I_s/\Delta V_{gs}$) is extrapolated from the region where the pinch-off is initiated.
(b) V_{ds}, V_{dg} vs. V_{gs} measurements, showing a drop in the V_{ds} corresponding to the change in $\Delta I_s/\Delta V_{gs}$. The curves for V_{dg} are plotted by using V_{dg}= V_{ds}+V_{gs}.

Electrical Evidence of Disorder at the SiO_2/4H-SiC MOS Interface and its Effect on Electron Transport

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Silicon carbide Schottky diodes have been in commercial production since 2002, their use has saved about $2B in energy and prevented about 10M tons of CO_2 from being released into the atmosphere worldwide, equivalent to taking 1.7M automobiles off the roads [1]. Recently, SiC power DMOSFETs entered commercial production [2], ushering in a new era of opportunity for wide bandgap power electronics. Going forward, high-voltage SiC MOSFETs and IGBTs hold the key to more efficient energy utilization and renewable energy production.

Unfortunately, SiC MOSFETs and IGBTs continue to be limited by low inversion layer electron mobility (the ratio of inversion mobility to bulk mobility in 4H-SiC is ~0.05, compared to ~0.5 for silicon). Although the SiC MOS community made rapid progress in the late 1990's with the discovery of post-oxidation annealing in nitric oxide [3,4], in recent years progress has stalled. In this paper, we report new electrical evidence of disorder at the SiO_2/4H-SiC interface. This disorder may be the mechanism limiting inversion layer mobility in SiC MOS devices.

One measure of interface disorder is the dispersion in interface state time constants. In 1967, Nicollian and Goetzberger [5] showed for silicon that random variations in fixed oxide charge were responsible for non-uniformities in surface potential across the interface, resulting in a dispersion in interface state time constants. It has been known since 1994 [6] that this dispersion is also present in SiC MOSFETs, and at levels ~2x larger than in silicon. In this paper we present evidence that the actual surface potential variations on 4H-SiC may be as large as 10x that of silicon, large enough to induce percolative transport in the inversion layer and reduce field-effect mobility to the levels currently observed. We also find evidence of a spatial distribution of interface traps across a 10 – 15 Å transition layer at the interface. Transition layers have also been detected by TEM and EELS studies [7], although these are wider and appear to lie within the SiC. Our observations lead us to conclude that structural, chemical, and electrostatic disorder at the SiC MOS interface is the dominant mechanism limiting the mobility. Focusing on interface disorder may open a new avenue for progress in SiC power MOSFET performance.

The key to this new understanding is an assumption in the MOS ac conductance technique [5] that interface state capture cross sections are independent of energy. This is not true in silicon [9] or SiC [6,10,11], since capture cross sections are observed to decrease *exponentially* with energy near the band edges. If one corrects for this effect [8], the actual surface potential fluctuations in 4H-SiC may be 5 –10x higher than previously thought, with a magnitude exceeding 0.5 V. Calculations indicate that his amount of surface potential variation would lead to percolative transport that could reduce inversion layer mobility to the range currently observed in SiC MOSFETs. However, MOS theory also shows that surface potential variations due to fixed oxide charges should be proportional to oxide thickness. Our measurements do not show this dependence, suggesting that another dispersion mechanism is also at work. We find that the observed dispersion is consistent with charge exchange with a spatial distribution of traps about 10 – 15 Å wide at the interface, possibly associated with interfacial sub-oxides involving carbon species. Therefore the disorder appears to involve both structural, chemical, and electrostatic components.

Although a complete understanding is not yet in hand, these observations open an avenue for future studies that may lead to renewed progress in interface quality and inversion layer mobility in SiC MOSFETs and IGBTs.

The authors acknowledge the generous support of the II-VI Foundation block grant program for this work.

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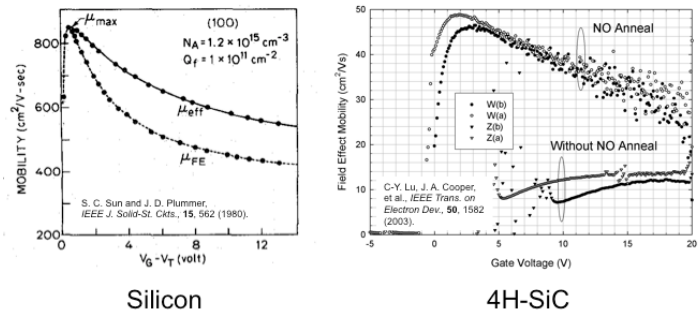

Fig 1. Comparison of inversion layer electron mobilities in silicon and 4H-SiC. In SiC, the mobility is higher for samples with a nitric oxide (NO) post-oxidation anneal, but the peak value is only about 6% of the electron mobility in bulk SiC.

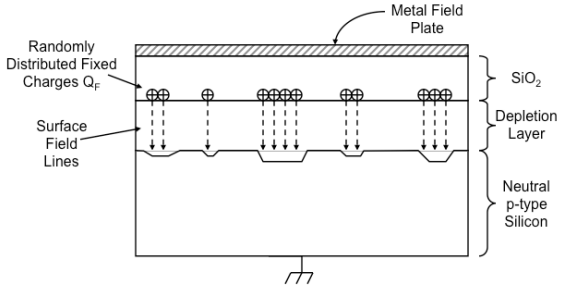

Fig 2. Effect of a random variation in fixed oxide charge. The surface potential, surface electric field, and depletion width all vary with position under the MOS gate.

$$\frac{G_P(\omega)}{\omega} = \frac{qD_{IT}}{2\sqrt{2\pi\sigma_{US}^2}} \int_{-\infty}^{\infty} \frac{\ln(1+\omega^2\tau^2)}{\omega\tau} \exp\left(-\frac{(u_S-\bar{u}_S)^2}{2\sigma_{US}^2}\right) du_S$$

$$\tau = \frac{1}{\sigma_N v_T n_S}$$ *is the time constant of the states opposite the Fermi level at this value of* u_S

Fig. 3 The ac conductance due to interface states G_P is obtained by integrating over surface potential u_S, weighted by the probability density function for surface potential, a Guassian with standard deviation σ_{US}. The interface state time constant τ depends on the interface state capture cross section σ_N, which may be a function of energy (see Fig. 4), and on the local electron density n_S, which depends exponentially on surface potential u_S.

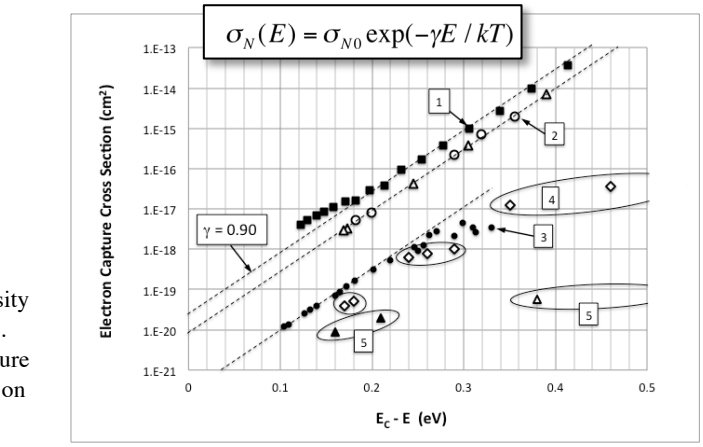

Fig. 4. Capture cross sections σ_N of interface states in 4H-SiC. Samples1-3 are measured using the ac conductance technique, 4-5 using CC-DLTS [11]. The exponential dependence on energy effectively cancels the exponential dependence of n_S on u_S in Fig. 3, leaving τ independent of u_S and masking the u_S variations.

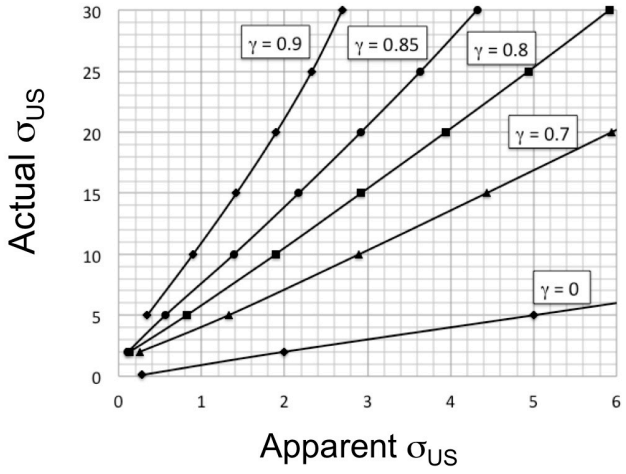

Fig. 5. Correction curves for $G_P(\omega)/\omega$ curves when capture cross sections are an exponential function of energy, as in Fig. 4. γ is the exponential slope factor for the σ_N plots in Fig. 4. For typical 4H-SiC samples, $\gamma \approx 0.9$ and the apparent $\sigma_{US} \approx 4$-5. From the above plot, the actual standard deviation of surface potential σ_{US} may be ≥ 30 kT/q. Such a u_S variation would represent a rugged potential landscape under the gate that can lead to percolative transport and significantly lower electron mobility, as shown in Fig. 6.

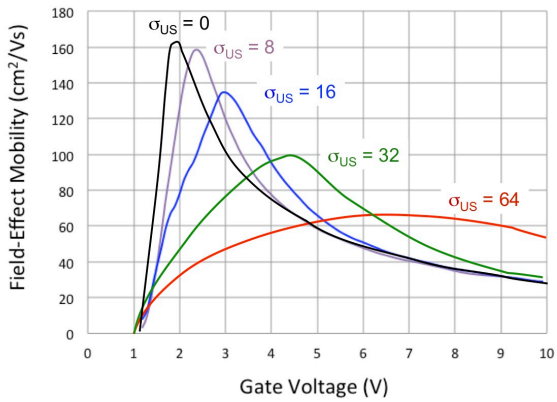

Fig. 6. Calculated field-effect mobility in 4H-SiC as a function of the standard deviation of surface potential σ_{US}, using a percolation model. For a uniform interface, $\sigma_{US} = 0$ and the peak mobility is ~ 160 cm²/Vs. If $\sigma_{US} \sim 30$, as suggested by Fig. 5, the peak mobility is reduced by as much as a factor of two. This effect could account for the low mobility in 4H-SiC MOSFETs.

Asymmetric Dual-Grating Gate InGaAs/InAlAs/InP HEMTs for Ultrafast and Ultrahigh Sensitive Terahertz Detection

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The development of Terahertz optoelectronic devices is a subarea of major currently ongoing advanced research effort. Electronic and photonic solidstate devices reache fundamental limitations in Terahertz frequency range, therefore this development is very crucially relying on the availability of new materials, new physical mechanisms, new device designs, and new fabrications/approaches. Here we explore terahertz detectors based on engineered plasmonic structure. We report a record sensitivity of 6.4 kV/W and noise equivalent power (NEP) of 15 pW/$\sqrt{\text{Hz}}$ in the above 1 THz region. The key point of this major breakthrough is careful design and fabrication of Field Effect Transistor (FET) structures combining i) interdigitated metal gates that ensure efficient coupling with incoming terahertz electromagnetic field and ii) an asymmetric metallization scheme that breaks the mirror symmetry of the internal electric-field profile in the channel[1]. Terahertz detection has only been reported mainly in the subterahertz regions (0.1-1THz) with sensitivities of about five times weaker in Schottky barrier diodes (SBDs[2]), as well as conventional single-gate plasmonic FETs[3] and symmetric grating gates plasmonic (S-DGG) FETs[4].

A Schematic view and scanning electron micrograph of asymmetric grating gates (A-DGG) FET detector are shown in Figure 1. The transistor structure consists of an $In_{0.52}AlAs/In_{0.53/0.70/0.53}GaAs/InP$ heterostructure with selective doping in the InAlAs layer (the electron mobility is 11000 cm^2/Vs). The spacing between metal fingers of the two sub-grating gates is set to be d1 and d2 with *d1/d2* = 0.5. This introduces asymmetric boundaries conditions in each unit cell of the structure. Figure 2 shows numerical simulations of photovoltaic response, electric-current spatial distribution and absorbance spectrum for U_{g1} = 0 V, U_{g2}= U_{th2} (< 0). One can see a giant enhancement of responsivity until four orders of magnitude (Fig.2a) in asymmetric structures ($d1 \neq d2$) compared to symmetric ones ($d1 = d2$). Figure 2b shows the electric-current distribution, underneath an A-DGG unit cell. It is clearely seen that the photocurrent (thus the responsivity) dramatically increases in the undepleted regions, as the portions of the channel under the second sub-grating gates is strongly depleted. Two different processes may be considered to analyze the enhancement of the photovoltage in our A-DGG-FET structures: i) resonant excitation of plasmon modes in undepleted portions of the 2D electron channel that generate strong THz photocurrent due to the nonlinear behavior of these plasmons. Indeed as seen in Fig.2c the calculated absorbance spectrum shows two resonances around 1.3 THz and ~ 2.2 THz. ii) Non resonant excitation of overdamped plasmons in depleted regions. The strong depleting of those regions greatly enhances the channel resistance, which leads to enormous enhancement of the photovoltage induced between the source and drain contacts of the entire A-DGG-FET structure. Therefore these structures combine the advantages of both, resonant and non-resonant plasmonic THz detectors. Figure 3a shows measured photovoltaic response under illumination at 292 GHz for three different temperatures (50 K, 75 K and 125 K). By decreasing the temperature, one can see a peak appearing as a shoulder and narrowing on the detection curves. This peak is identified as gated plasmon resonance under the unbiased portions of the channel. The frequency width of this resonance can be estimated as $\delta f = (f/2)^{*}(\delta U_{g1}/(U_{g1} - U_{th1}))$ where f is the incident frequency. This width varies from 279 GHz to 100 GHz when the temperature decreases. This corresponds to the plasma waves damping time of the order of 20 ps and an intrinsic response speed of the same order. Figure 3b shows measured responsivities at 300 K and related NEP under illumination at 1 THz. Responsivities of as high as 2.2 kV/W and NEP below 15 pW/$Hz^{0.5}$ have been obtained. These values are lower than those of commercial room temperature THz detectors such as Golay cells (200 – 400 pW/$Hz^{0.5}$) [4] or SBDs (100 pW/$Hz^{0.5}$)[2]. Figure 4 shows measured responsivities at 300 K when constant source to drain voltages are applied in the structure (V_{ds} = 0. 0.2, and 0.4 V) under illumination at 1, 1.5 and 2 THz. One can see marked increase in responsivity from 0.4 to 6.4 kV/W at 1.5 THz when V_{ds} reaches 0.4 V (Fig.4b) and the responsivity showing a monotonic decrease with increase in radiation frequency. Nevertheless Fig 4c exhibits an opposite dependency with a maximal peak responsivity of 4.8 kV/W at 2 THz. This is interpreted as a resonant-like behavior due to the A-DGG structure.

To our knowledge, these are the highest sensitive THz detectors reported in the frequencies above 1 THz and the response speed of these A-DGG detectors is expected to be high owing to ultrafast plasmon dynamics.

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[2]http://virginiadiodes.com/index.php?option=com_content&view=article&id=12&Itemid=3.[3]Y.F. Sun et al APL **98**,252103 (2011). [4]D. Coquillat, et al. Opt. Exp. **18**. 6024.(2010). [5]OAD-7 Golay Detector Operating Manual, Cardiff, U.K., Jan. (2005).

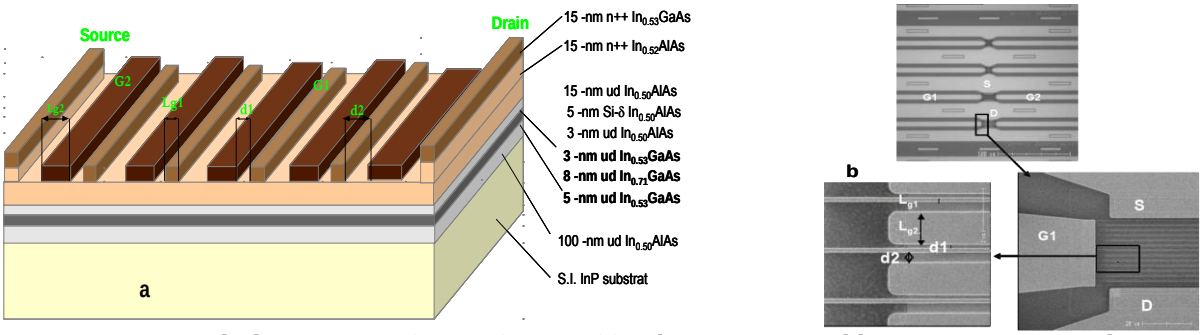

Figure 1: Asymmetric dual grating-gate (A-DGG) FETs. (a) Schematic view and heterostructure material systems. (b) scanning electron micrograph of A-DGG FETs.

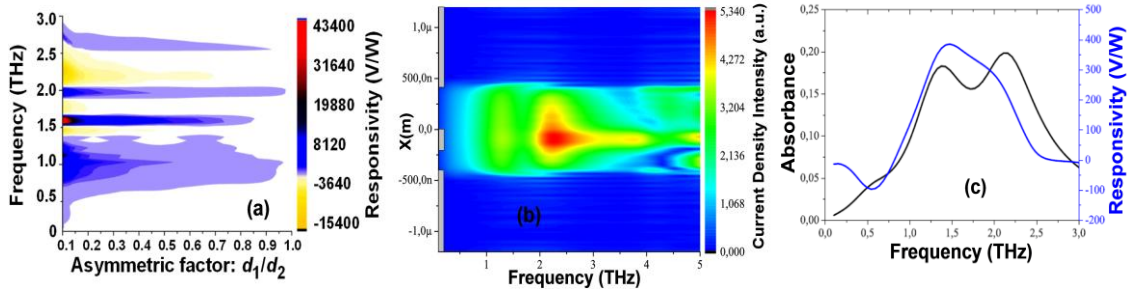

Figure 2: (a) Simulated relative responsivity as a function of d_1/d_2. L_{g1} = 400 nm, L_{g2} = 2.4 µm, $d_1 + d_2$ = 800 nm, W = 3.6 µm. Electron density under G2: $2.5x10^{11}$ cm^{-2}, and that the other area: $2.5x10^{12}$ cm^{-2}. (b) Simulated current distribution underneath a unit A-DGG cell for the assymetric factor of d_1/d_2 = 0.5

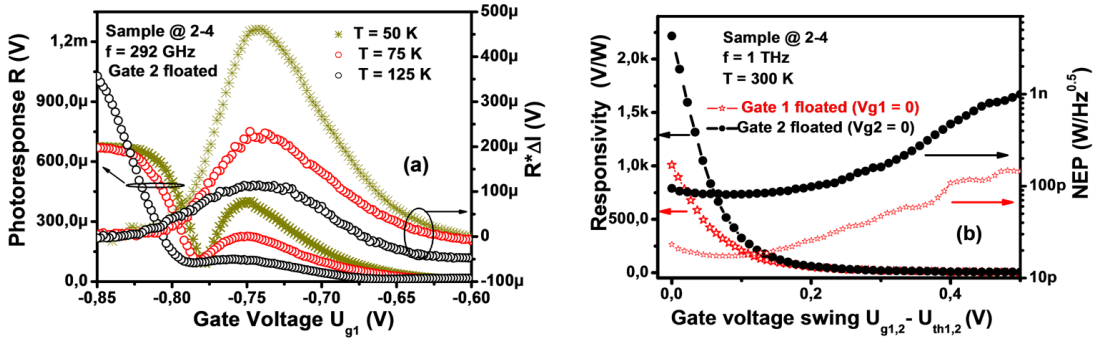

Figure 3: (a) Measured responsivity (left) the channel voltage R*ΔI (right) as a function of gate voltage U_{g1}, at 292 GHz for different temperature. R is the channel resistance ΔI ($I_{\text{with radiation}} - I_{\text{without radiation}}$) is the difference induced in drain current by the incoming THz radiation. b- Measured responsivity as functions of gate voltage swing $U_{g1,2}$-$U_{th1,2}$ at 1 THz and 300 K (left). (b) Measured noise equivalent power as a function of gate voltage swings.

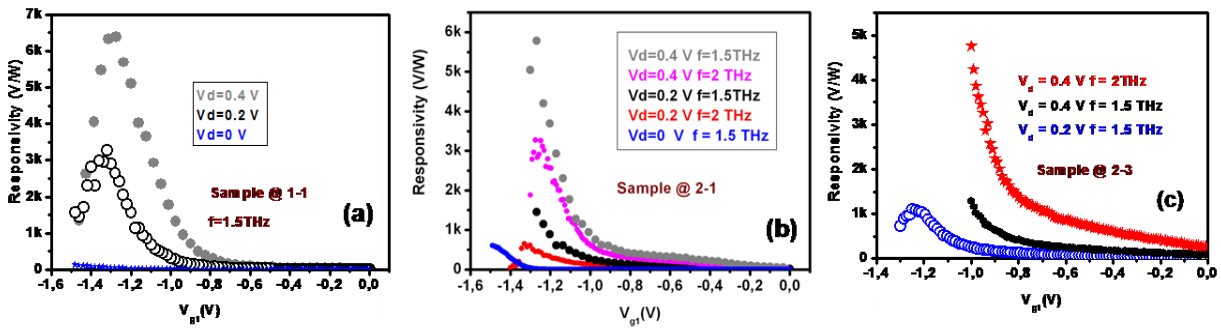

Figure 4. Measured responsivity as a function of U_{g1} while U_{g2} = 0 V for constant source to drain voltage V_{ds} (0, 0.2 and 0.4 V) at 300 K and illumination frequencies of 1.5 and 2 THz.

Session IV.B (Dean's Hall II)

1/2-Dimensional FETs

Tuesday AM, June 19th, 2012

Session Chair(s): Eric Pop, University of Illinois and Joshua Robinson, Penn State University

8:20 AM IV.B-1
Role of Screening, Heating, and Dielectrics on High-Field Transport in Graphene
A. Y. Serov, Z.-Y. Ong, V. E. Dorgan and E. Pop, Dept. of Electrical and Computer Engineering, University of Illinois, Urbana-Champaign, Illinois, USA and Micro and Nanotechnology Lab, Urbana Illinois, USA

8:40 AM IV.B-2
Graphene field-effect transistors with self-aligned spin-on-doping of source/drain access regions
H. C. P. Movva[1], M. E. Ramón[1], C. M. Corbet[1], F. S. Chowdhury[1], G. Carpenter[2], E. Tutuc[1], and S. K. Banerjee[1], [1]Microelectronics Research Center, The University of Texas at Austin, Texas, USA and [2]IBM Research, Austin, Texas, USA

9:00 AM IV.B-3
High Performance, Large Area Graphene Transistors on Quasi-Free-Standing Graphene Using Synthetic Hexagonal Boron Nitride Gate Dielectrics
M. J. Hollander, A. Agrawal, M. S. Bresnehan, M. LaBella, K. A. Trumbull, R. Cavalero, S. Datta, and J. A. Robinson, The Pennsylvania State University, University Park, Pennsylvania , USA

9:20 AM IV.B-4 Invited Paper
MoS_2-based devices and circuits
B. Radisavljevic, D. Krasnozhon, M.B. Whitwick, and A. Kis, Electrical Engineering Institute, School of Engineering, EPFL, Lausanne, SWITZERLAND

10:00 AM Break

10:20 AM IV.B-5
Extraction of Near Interface Trap Density in Top Gated Graphene Transistor Using High Frequency Current Voltage Characteristics
H. Madan[1], M. J. Hollander[1], J. A. Robinson[2], and S. Datta[1], [1]Elec4ical Engineering, The Pennsylvania State University, University Park, Pennsylvanis, USA and [2]Material Science and Engineering. The Pennsylvania State University, University Park, Pennsylvnia, USA

10:40 AM IV.B-6
Pulsed Nanosecond Characterization of Graphene Transistors
E. Carrion, A. Malik, A. Behnam, S. Islam, F. Xiong and E. Pop, Dept. of Electrical and Computer Engineering, University of Illinois, Urbana-Champaign, Illinois, USA and Micro and Nanotechnology Lab, Urbana, Illinois, USA

11:00 AM IV.B-7
Graphene Nanomesh Contacts and Its Transport Properties
T. Chu and Z. Chen, ECE Department and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana, USA

11:20 AM IV.B-8
First Demonstration of Two-Dimensional WS2 Transistors Exhibiting 105 Room Temperature Modulation and Ambipolar Behavior
W. S. Hwang1, M. Remskar2, R. Yan1, V. Protasenko1, K. Tahy1, S. D. Chae1, H. Xing1, A. Seabaugh1, and D. Jena1, 1Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA and 2Solid State Physics Department, Jozef Stefan Institute, Ljubljana, SLOVENIA

11:20 AM IV.B-9

Low-frequency Noise in Contact and Channel Regions of Ambipolar InAs Nanowire Transistors

C. J. Delker[1], Y. Zi[2], C. Yang[2,3], D. B. Janes[1], [1]School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana, USA, [2]Department of Physics, Purdue University, West Lafayette, Indiana, USA, and [3]Department of Chemistry, Purdue University, West Lafayette, Indiana, USA

Role of Screening, Heating, and Dielectrics on High-Field Transport in Graphene

Andrey Y. Serov, Zhun-Yong Ong, Vincent E. Dorgan and Eric Pop
Dept. of Electrical and Computer Engineering, University of Illinois, Urbana-Champaign
Micro and Nanotechnology Lab, 208 N Wright St, Urbana IL 61801. E-mail: epop@illinois.edu

Graphene is an interesting material for electronic applications due to its high intrinsic mobility at low-field. However, high-field transport in graphene is less well understood, with the simple assumption often made that it is limited by substrate optical phonon (SO) scattering. Here we model high-field transport in graphene on several dielectric substrates including SO and graphene phonons, proper charge screening, impurity scattering, and self-heating effects. Our model is carefully calibrated against existing experimental data for graphene on SiO_2 [1] at several ambient temperatures and different carrier densities. We then use it to investigate transport in graphene on other dielectrics where experiments do not exist yet.

We use the hydrodynamic model [2], including acoustic phonon (AP) scattering, graphene optical phonon (OP) scattering, SO phonons (two transverse OPs, i.e. TO1 and TO2), ionized impurities and neutral impurities. The SO scattering rate is proportional to $1/(\varepsilon^{i} + \varepsilon_{gr}(q)) - 1/(\varepsilon^{0} + \varepsilon_{gr}(q))$ for the TO1 dielectric mode, and to $1/(\varepsilon^{\infty} + \varepsilon_{gr}(q)) - 1/(\varepsilon^{i} + \varepsilon_{gr}(q))$ for the TO2 mode, where ε^{∞}, ε^{i}, ε^{0} are the static(valence), intermediate, and static(electron) permittivities of the dielectric, and $\varepsilon_{gr}(q)$ is the screening dielectric function of graphene as a function of wave vector q, with the Thomas-Fermi approximation [3]. We include self-heating at high-field with separate graphene lattice temperature and substrate temperature using the substrate thermal conductivity and graphene-SiO_2 thermal boundary resistance [1,4]. AP and OP scattering heat the graphene lattice, and remote SOs dissipate power directly to the substrate (Fig. 1a).

The dependence of drift velocity on electric field (E-field) on SiO_2 is shown in Figs. 1b-c, in excellent agreement with experiments [1] at both 80 K and 300 K. The main contribution to the low-field mobility comes from impurity scattering, explaining similar mobilities at 80 K and 300 K [1,5]. The device temperature significantly increases in the considered range of E-fields as shown in Fig. 2a, where temperatures of electrons (T_e), graphene lattice (T_{gr}), and the top SiO_2 interface (T_{SiO2}) are all shown. The difference between T_{gr} and T_{SiO2} is caused by the thermal resistance of the graphene-SiO_2 interface [1]; this difference is small but getting bigger at higher field because the power dissipated into the graphene by OPs increases with the field. In Fig. 2b we find that the power is mostly dissipated by graphene OPs and not by SO phonons (as previous models had suggested) because SO phonons are more effectively screened by charge carriers. At higher carrier densities the role of SO phonons decreases due to screening, while the role of OP scattering increases as more carriers reach the OP energy emission threshold (~0.18 eV).

The effect of lattice heating on saturation velocity (v_{sat}) is shown in Fig. 2c, where we plot simulation results with and without self-heating; the latter case exhibits much weaker saturation, similar to a previous study [6]. We also examined the effect of ionized impurity concentration (n_{imp}) on v_{sat} as shown in Fig. 3a, and we found that at lower carrier density the effect can be substantial, but it reduces at higher carrier density; this can be attributed to the screening of impurities and stronger OP scattering. Using the same thermal parameters and n_{imp} we calculated high-field transport in graphene on BN, HfO_2 and Al_2O_3 as shown in Figs. 3b-c. We found that v_{sat} changes only moderately on different dielectrics, with BN exhibiting the highest v_{sat} and HfO_2 the lowest one, the latter due to the smaller phonon energies. We assumed identical n_{imp} here, but these could vary in practice under different fabrication conditions.

In summary, we calculated the dependence of drift velocity on E-field in graphene on various dielectrics. After including the proper screening of substrate phonons, we found that power is mostly dissipated by graphene optical phonons. We also found that self-heating causes much stronger velocity saturation and obtained the dependence of saturation velocity on ionized impurity concentration. Other parameters being equal, we found that BN allows a higher saturation velocity of graphene than SiO_2, HfO_2 or Al_2O_3.

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[2] R. Bistritzer et al, *Phys. Rev. B* 80, 085109 (2009)
[3] M.V. Fischetti et al, *J. Appl. Phys*. 90, 4587 (2001)
[4] X. Li et al, *Appl. Phys. Lett.* 99, 233114 (2011)
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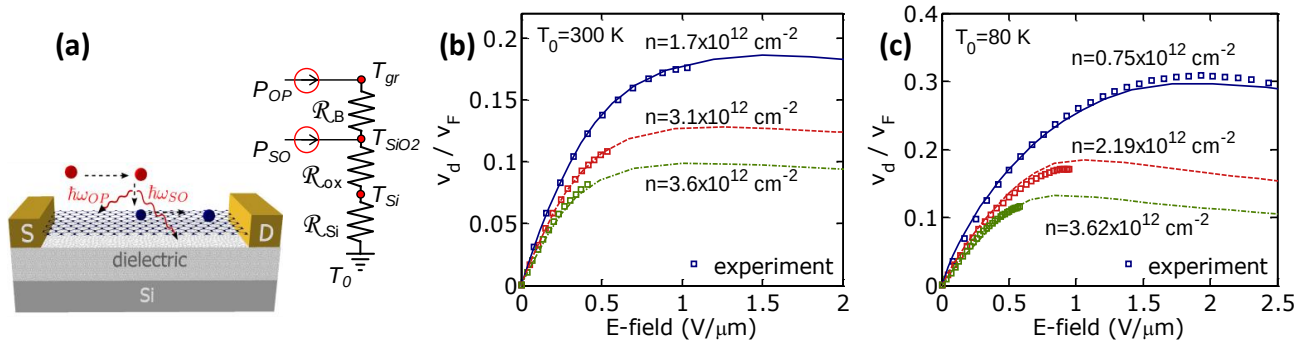

Figure 1. (a) Power dissipation in graphene devices via graphene optical phonons (OPs) and dielectric surface optical phonons (SOs). (b) Drift velocity v_d (normalized by Fermi velocity $v_F = 10^8$ cm/s) as a function of electric field (E-field) in graphene on SiO_2 at background temperature T_0 = 300 K. (c) Drift velocity at background temperature T_0 = 80 K. Experimental data (symbols) from Ref. [1] is used for comparison.

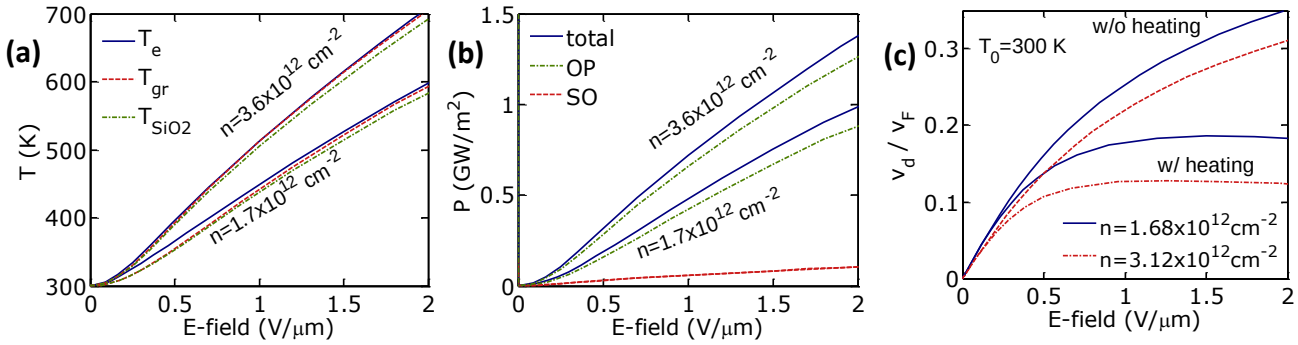

Figure 2. (a) Self-heating: electron temperature (T_e), graphene lattice temperature (T_{gr}) and SiO_2 substrate surface temperature (T_{SiO2}) as a function of E-field for two carrier densities. (b) Power dissipation in graphene transistors via graphene OPs (~90%) and dielectric SOs (~10%). (c) Drift velocity v_d normalized by v_F as a function of E-field with and without accounting for the device self-heating. The self-heating model here assumes a thermal resistance equivalent to that of ~300 nm SiO_2, as in Ref. [1].

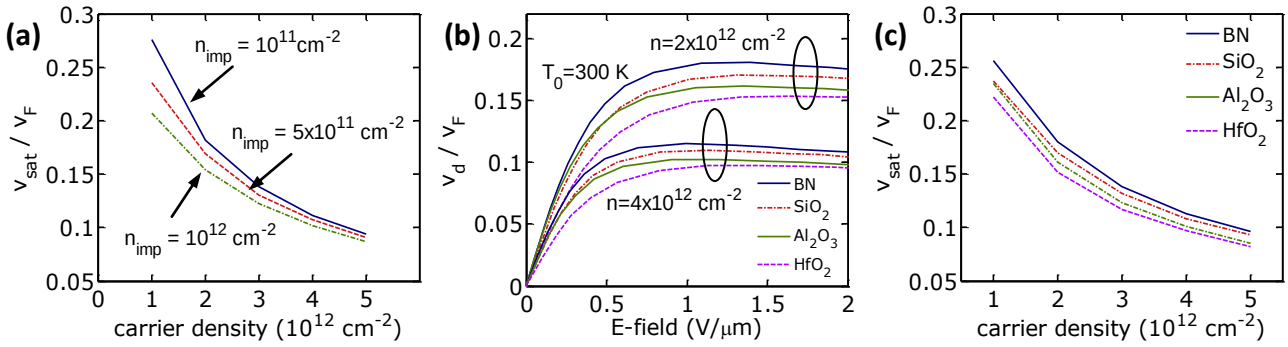

Figure 3. (a) Saturation velocity v_{sat} (normalized by v_F) in graphene on SiO_2 as a function of carrier density for different concentrations of charged impurity n_{imp}. (b) Drift velocity as a function of E-field at background temperature 300 K for different dielectrics: BN, SiO_2, Al_2O_3 and HfO_2. (c) Saturation velocity as a function of carrier density for graphene on BN, SiO_2, Al_2O_3 and HfO_2.

Graphene field-effect transistors with self-aligned spin-on-doping of source/drain access regions

Hema C. P. Movva [1], Michael E. Ramón [1], Chris M. Corbet [1], Fahad Sk. Chowdhury [1], Gary Carpenter [2], Emanuel Tutuc [1], Sanjay K. Banerjee [1]
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The exceptional electronic properties of graphene field-effect transistors (GFETs) make them a promising replacement for conventional Si CMOS transistors for high frequency analog applications. Radio frequency GFETs with intrinsic cut-off frequencies as high as 300GHz have been reported [1], with theoretically predicted THz frequencies only being limited by fabrication challenges. A major factor responsible for degradation of GFET performance is high series resistance of the access regions between the source/drain contacts and the top-gated graphene channel, which reduces maximum possible drive currents. A back-gate bias can be used to modulate this resistance, but this approach does not provide for independent control of multiple GFETs on the same substrate and for GFETs on insulating substrates. GFETs with self-aligned gates overcome this problem by reducing the access region resistance, but their fabrication is not straightforward [1, 2]. Here, we propose a simple scheme of improving GFET performance by reducing the source/drain access resistance using self-aligned charge-transfer doping. A novel and controllable way of "spin-on-doping" of the access regions with chemical dopants is demonstrated.

Back-gated GFETs were fabricated on highly-doped Si substrates with a 285nm thermally grown SiO_2 layer. Monolayer graphene was exfoliated and active regions were patterned by e-beam lithography (EBL) and oxygen plasma etching. A second EBL step was used to define metal contacts for 4-point probe structures, followed by e-beam evaporation of Ni contacts and a subsequent lift-off process. A dilute solution of poly(ethylene imine) (PEI) in methanol (0.02% w/w) was used for spin-on-doping of the GFETs at 1500 rpm for 60s, followed by a quick bake at 90°C for 20s to drive away any remaining methanol residues (Fig. 1(a)). PEI has been shown to dope graphene n-type due to its electron-donating, amine-rich structure [3]. Fig. 2 shows shifts in the Dirac voltage (V_{DIRAC}) of a back-gated GFET to more negative voltages with every successive spin-on-doping step, indicating control of the amount of n-doping. There is a reduction in the channel resistivity at 0V back-gate bias from 4400 Ω to 1500 Ω after doping. This reduction of resistance, when employed to the source/drain access regions of a top-gated GFET, can result in improved GFET performance.

Dual-gated GFETs were fabricated on clean, undoped back-gated GFETs after depositing a 20nm Al_2O_3 layer as top-gate dielectric using atomic layer deposition (ALD) [4]. A Ni top-gate was fabricated by a final EBL step, metal deposition and lift-off. Dilute HF (1:50) was then used to etch away Al_2O_3 from the source/drain access regions in a self-aligned manner using the top-gate metal as a hard mask (Figs. 1(b), (c)). 2-point resistance measurements between the source and drain (Fig. 3) show the Dirac points of a dual-gated GFET before and after doping. The undoped resistance profile has a primary Dirac point at ~ 0V corresponding to the un-gated access regions and a secondary Dirac point at ~ -17 V corresponding to the top-gated region. This n-type behavior of the top-gated graphene is unintentional and might have been induced by impurities during device fabrication. Resistance profiles after spin-on-doping show n-type doping of the access regions, thereby reducing the resistance at 0V back-gate bias from 2.8 kΩ in the undoped case to 1.2 kΩ after doping. There is negligible change in V_{DIRAC} of the top-gated graphene region, as can be seen in Fig. 4, which shows 2-point resistance measurements as a function of the back-gate (V_{BG}) and top-gate (V_{TG}) biases. Doping the access-regions only induces a shift in the back-gated V_{DIRAC} to a more negative voltage while the top-gated V_{DIRAC} remains almost invariant. This manifests as an overall reduction in the top-gated 2-point resistance at V_{BG} = 0V. Fig. 5 shows the improvement in transfer characteristics of the GFET after doping. The maximum drive current ($I_{D,max}$) increases from 7.6 µA to 16.6 µA and the transconductance (g_m) from 4.2 µS to 10.3 µS after doping.

To fully demonstrate the advantage of self-aligned doping, top-gated GFETs were fabricated on graphene transferred to single-crystal, atomically smooth, insulating quartz substrates (Fig. 1(d)) which are more suited for RF applications due to their low parasitic capacitances. The absence of a back-gate on quartz makes it impossible to electrostatically modulate the resistance of the access regions but spin-on-doping can be used to reduce this resistance. The transfer characteristics show a ~ 2X increase in drive current (I_D), a ~ 3X increase in device transconductance (g_m) and a ~ 10% increase in the I_{ON}/I_{OFF} ratio after doping (Fig. 6(a)). There is very little reduction in extracted carrier mobility [4] from 5600 cm^2/V-s to 5200 cm^2/V-s after doping. The output characteristics of the GFET after doping are also seen to be superior to the undoped case (Fig. 6(b)).

In summary, we have developed a simple and controllable "spin-on-doping" technique to chemically dope graphene with very little degradation in carrier mobility. Further, we fabricated GFETs on Si/SiO_2 and quartz substrates and demonstrated improved GFET performance after doping the source/drain access-regions in a self-aligned manner.

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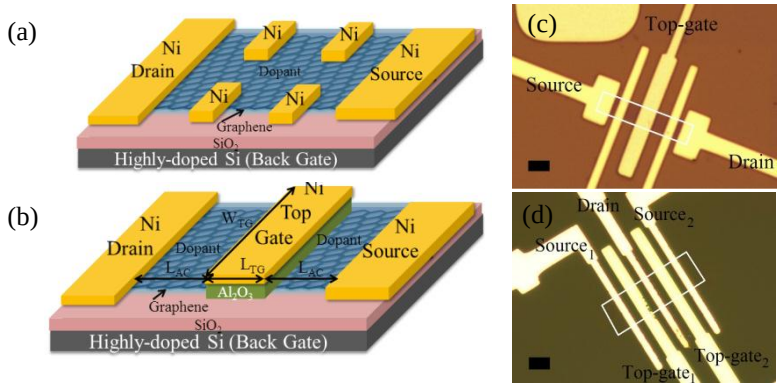

Fig. 1: (a) Schematic of a back-gated GFET on Si/SiO_2 after spin-on-doping and (b) a top-gated GFET with doped access regions. (c) Optical micrograph of a dual-gated GFET fabricated on Si/SiO_2 and (d) a top-gated GFET on quartz (both scale bars are 2μm). W_{TG}, L_{TG}: width and length of the top-gated region, L_{AC}: length of source/drain access regions. The graphene region is marked by a white line.

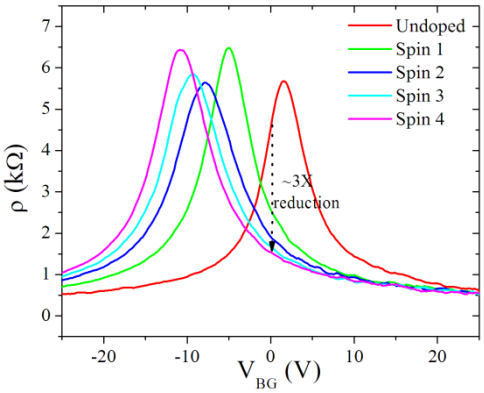

Fig. 2: Layer resistivity (ρ) versus back-gate bias (V_{BG}) measurements after successive spin-on-doping steps showing increasing n-type doping after every spin. Channel resistivity at V_{BG} = 0V reduces by a factor of ~ 3X after 4 spins.

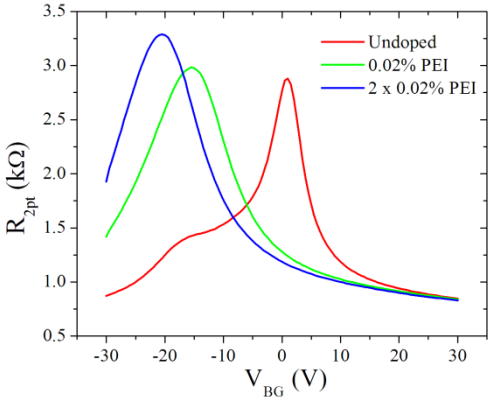

Fig. 3: 2-point resistance (R_{2pt}) versus back-gate bias (V_{BG}) (at top-gate bias (V_{TG}) = 0V) on a dual-gated GFET on Si/SiO_2 before and after doping. V_{DIRAC} of the access regions is at 0V and the top-gated region at -17V in the undoped case. The device dimensions are: W_{TG}/L_{TG} = 7.0 μm/1.0 μm; L_{AC} = 1.6 μm.

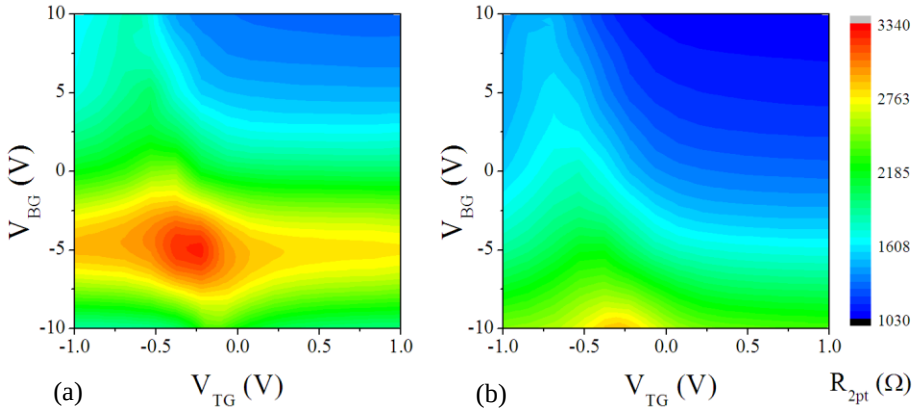

Fig. 4: 2-point resistance measurements as a function of the back-gate (V_{BG}) and top-gate (V_{TG}) biases on a GFET (a) as-fabricated and (b) after etching oxide from the source/drain access regions and spin-on-doping. Doping only shifts the resistance profile to a more negative value along the V_{BG} axis, keeping the profile along V_{TG} invariant.

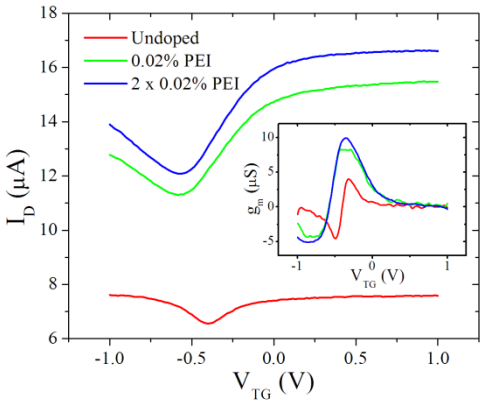

Fig. 5: Improvement in transfer characteristics of the GFET on Si/SiO_2 (Fig. 1(c)) after doping, showing a ~ 2.2X enhancement in $I_{D,max}$ and (inset) a ~ 2.5X improvement in g_m. The access region resistance reduces by 1.6 kΩ after the second spin.

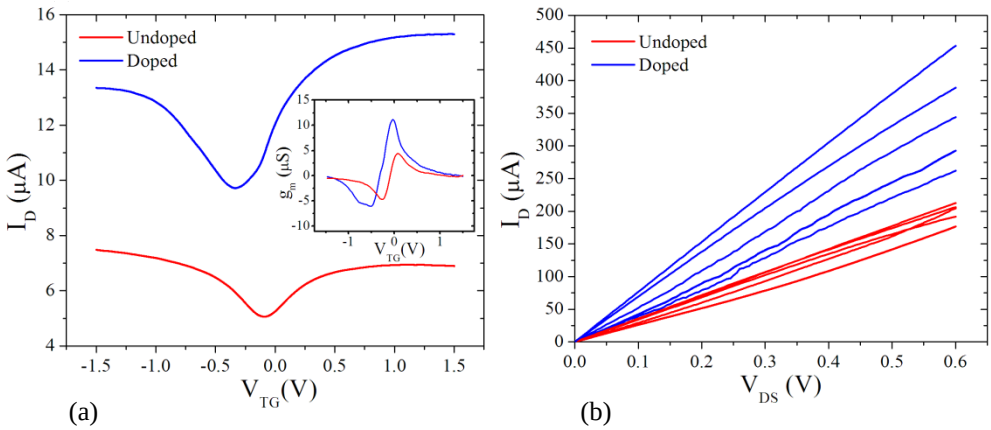

Fig. 6: (a) Transfer characteristics of the GFET on quartz (Fig. 1(d)) with improved drive current (I_D) after doping and (inset) enhanced device transconductance (g_m). The I_{ON}/I_{OFF} ratio also improves after doping. (b) Output characteristics of the GFET also show improved device performance. V_{TG}-V_{DIRAC} is swept from 0 V to 1 V in steps of 0.25 V. The device dimensions are: W_{TG}/L_{TG} = 7.0 μm/2.0 μm; L_{AC} = 1.8 μm.

High Performance, Large Area Graphene Transistors on Quasi-Free-Standing Graphene Using Synthetic Hexagonal Boron Nitride Gate Dielectrics

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In recent years, hexagonal boron nitride (h-BN) has gained interest as a material for use in graphene based electronics, where its ultra-smooth two-dimensional structure, lack of dangling bonds, and high energy surface optical phonon modes are desirable when considering the effect of dielectric materials in introducing additional sources of scattering for carriers within graphene. Initial work has indicated that use of h-BN in place of SiO_2 supporting substrates can lead to 2-3x improvements in device performance [1,2], suggesting that h-BN may be an excellent choice as top-gate dielectric for graphene devices. In this work, we integrate h-BN with quasi-free-standing graphene (QFEG) for the first time and demonstrate a 2x improvement in radio frequency (RF) performance and the highest $f_T \cdot L_g$ product yet reported for h-BN integrated graphene devices (25 GHz·μm).

QFEG is a form of large-area graphene derived from epitaxial graphene (EG) using a hydrogen passivation step, resulting in improved transport properties relative to conventional EG on SiC [3]. Integration of h-BN with QFEG is achieved utilizing a catalytic thermal chemical vapor deposition growth process on Cu substrates in conjunction with a large-area solution transfer process (Fig. 1). Two-finger RF transistors with gate length 750 nm are fabricated using conventional, production scale photolithographic methods. Fig. 1c shows the schematic cross section of a typical graphene transistor.

Room temperature Hall effect measurements and DC output characteristics of h-BN (t_{ox} = 50 nm) and HfO_2 (t_{ox} = 10 nm) coated QFEG transistors are shown in Fig. 2. Although extensive p-type doping is found to occur after hydrogen passivation, integration of HfO_2 dielectrics leads to significant electron doping and a shift in V_{Dirac} close to V_{gs}=0V while integration of h-BN leads to little change in the as-grown carrier density and V_{Dirac} remains at large positive values of V_{gs} (>10V). DC characteristics of h-BN gated transistors show reduced on-off ratios relative to HfO_2, yet demonstrate excellent drive current >1.6 A/mm at V_{ds}=1V (Fig. 2b,c). Peak transconductance is found to be <10 μS/μm (Fig. 3a), which is attributed to the relatively large EOT for these devices (~50 nm) as well as the increasing dominance of contact resistance at high drive currents (~200 Ω-μm). Normalizing transconductance with C_{ox}, we find that h-BN devices offer a very competitive g_m/C_{ox} ratio even for the limited range of testable voltages and despite the impact of contact resistance (Fig. 3b). Wafer scale testing confirms that use of solution transfer processing does not negatively impact wafer uniformity or device yield, which is found to be ~90% (Fig. 3c).

RF performance is excellent for h-BN gated transistors (Fig. 4a), exhibiting peak intrinsic f_T of 33.3 GHz at a gate length of 750 nm with V_{ds}=1V, which represents a 2x improvement relative to HfO_2 coated transistors, where intrinsic f_T was extracted from measured S-parameters using a standard short-open-load-thru de-embed process to calibrate out the effect of probe and pad parasitics. The increase in RF performance is found to be a result of improved transport properties relative to HfO_2 coated QFEG. Temperature dependent transport measurements indicate that h-BN dielectrics are effective in preserving carrier mobilities as high as 2700 cm^2/V sec, which is only ~10% smaller than the highest reported mobilities for un-coated QFEG, while modeling of the scattering processes indicates that use of h-BN dielectrics introduces less remote charged impurity and remote surface optical phonon scattering than HfO_2 dielectrics (Fig. 4b,c).

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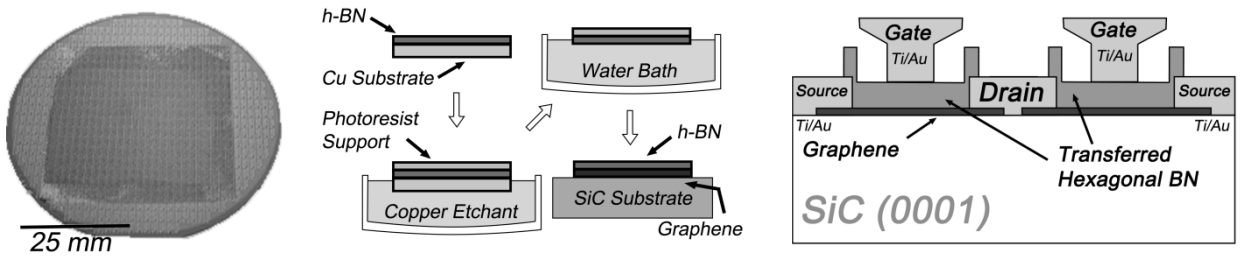
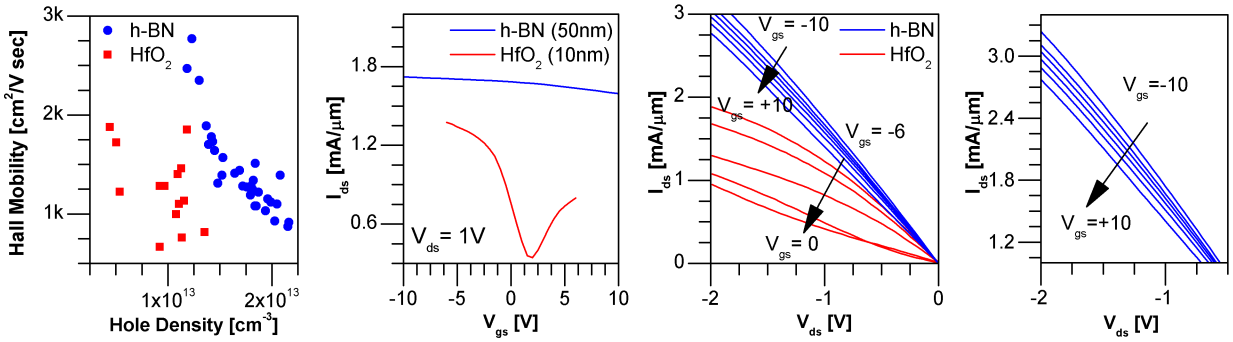


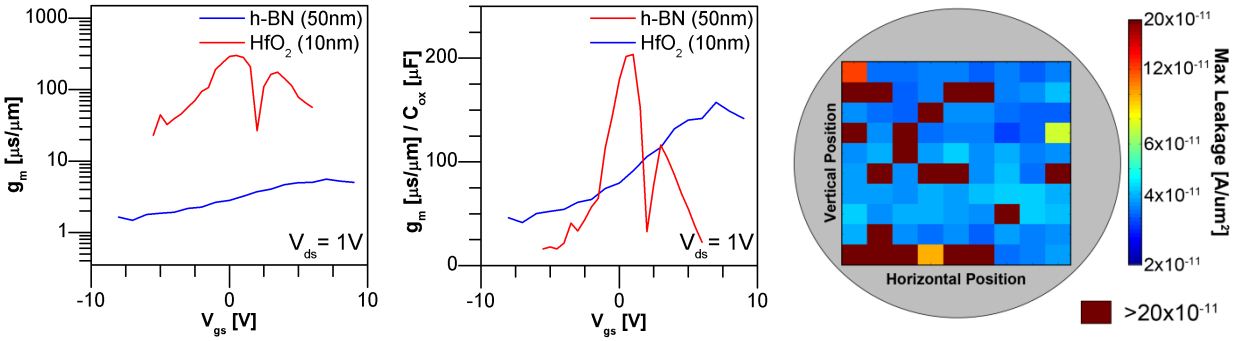
(a) (b) (c)

Figure 1. Photograph of 3-inch QFEG wafer with h-BN top-gate dielectric (a) and schematic representation of solution transfer process used to integrate h-BN with QFEG after catalytic synthesis (b). Schematic cross section of two finger graphene transistor (c).



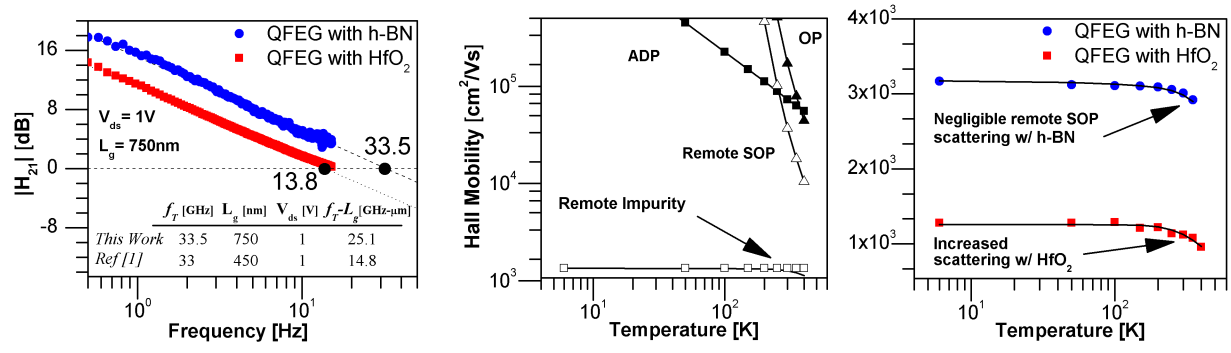
(a) (b) (c) (d)

Figure 2. Scatter plot of Hall mobility versus carrier concentration (a) compared to DC output characteristics of h-BN and HfO_2 coated graphene transistors (b),(c),(d).



(a) (b) (c)

Figure 3. g_m and g_m/C_{ox} of QFEG transistors (a),(b). Wafer map of peak gate current density (c).



(a) (b) (c)

Figure 4. Intrinsic RF characteristics of h-BN and HfO_2 coated transistors (a). Temperature dependent modeling of h-BN and HfO_2 coated QFEG showing the reduction in remote SOP and impurity scattering with h-BN gates (b),(c).

MoS_2-based devices and circuits

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Two-dimensional crystals offer several inherent advantages over conventional 3D electronic materials or 1D nanomaterials such as nanotubes and nanowires. Their planar geometry makes it easier to fabricate circuits and complex structures by tailoring 2D layers into desired shapes. Because of their atomic scale thickness, 2D materials also represent the ultimate limit of miniaturization in the vertical dimension and allow the fabrication of shorter transistors due to enhanced electrostatic control. Another advantage of 2D semiconductors is that their electronic properties (band gap, mobility, work function) can be tuned for example by changing the number of layers or applying external electric fields.

The best known 2D material today is graphene, [1] with its high room temperature mobility of at least 120,000 cm2/Vs. [2] Graphene however has no band gap which limits its potential field of applications in electronics to applications in analogue RF electronics where devices with cut-off frequencies above 100 GHz have been reported. [3]

Single layers of semiconducting transition metal dichalcogenides such as MoS_2 (figure 1a) could be used as an alternative to graphene in applications that require the presence of band gap, for example in low-power digital electronics. We have recently demonstrated that a 2D material in the form of semiconducting single-layer MoS_2 (Figure 1a) could be used to fabricate dual-gate field-effect transistors. Our devices consist of a single layer of MoS_2 0.65 nm thick contacted with gold electrodes and controlled by a local top gate separated from the channel by 30 nm of HfO_2 gate dielectric as shown on Figure 2b. Transistor gating response shown on Figure 1c shows extremely low room-temperature I_{off} (25fA/um), high I_{on}/I_{off} (10^8) and mobility comparable to thin-film Si (~200 cm^2/Vs) [4].

We have also incorporated MoS_2-based transistors into simple functional circuits. Figure 2a shows the output vs. input voltage characteristics of an MoS_2-based digital inverter. The inverter gain, shown on figure 2b is higher than 4 and shows that MoS_2-based inverters can be integrated in more complex logic circuits. Our circuits can also be operated as analogue amplifier. Figure 2c shows an example of an amplification of an input AC signal using an MoS_2 amplifier. We have also been successful in growing large-area CVD MoS_2 which is 1-3 layers thick, with gating characteristics of a resulting device shown on Figure 3. This should open the way to more complex circuits in future. MoS_2 also a Young's modulus comparable to stainless steel can be deformed up to 10% strain, making it the strongest semiconducting material and very interesting for applications in flexible electronics [5]. MoS_2 therefore combines the high degree of electrostatic control that can lead to efficient switching and low power dissipation with mechanical properties suitable for integration with flexible substrates.

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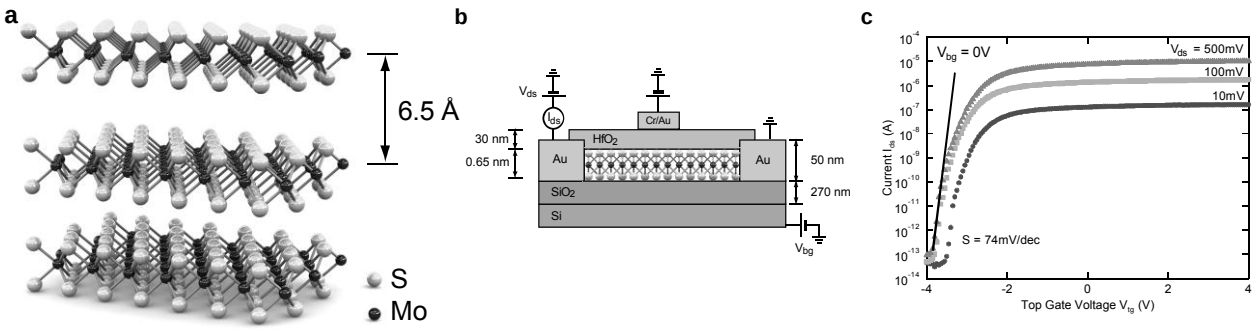

Figure 1. a. Crystalline Structure of MoS_2. Single layers, 6.5Å thick can be extracted and used to build electronic devices. b. Cross-sectional view of the structure of monolayer MoS_2 FET together with electrical connections used to characterize the device. Single layer of MoS_2 6.5 Å thick is deposited on degenerately doped Si substrate with 270 nm thick SiO_2. The substrate acts a back gate. One of the gold electrodes acts as drain while the other, source electrode is grounded. The monolayer is separated from the top gate by 30 nm of ALD-grown HfO_2. The top gate width for device is 4 μm while the top gate length, source-gate and gate-drain spacing is 500 nm. c. Room-temperature switching characteristics of a single-layer MoS_2 FET shows very low leakage currents (<25fA/μm), high current on/off ratio (10^8) and steep subthreshold slope (74mV/dec).

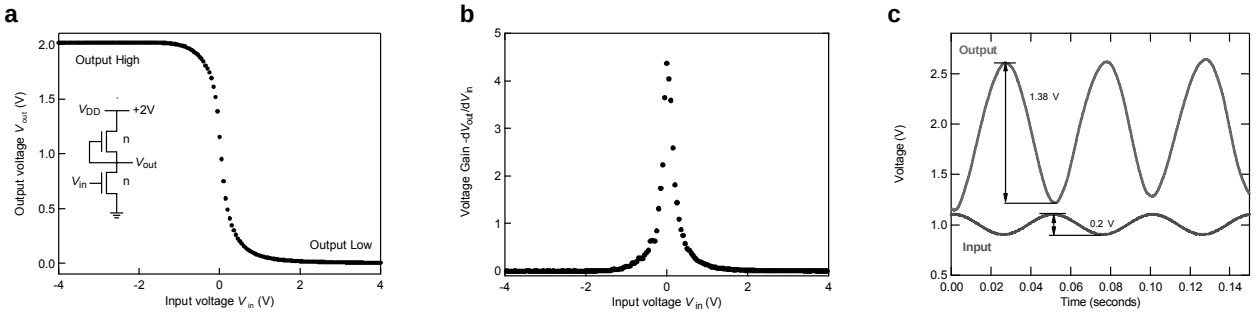

Figure 2. a. Output voltage as a function of the input voltage applied to the integrated MoS_2 inverter. b. The dependence of the inverter gain (negative value of dV_{out}/dV_{in}) on the input voltage. The maximal voltage gain above 4 indicates that our inverter is suitable for integration in arrays of logic devices. c. Demonstration of the small-signal amplifier operation. On the input of the amplifier a sinusoidal signal V_{in}-AC of amplitude ΔV_{in}= 100mV resulting in an amplified sinusoidal signal on the output.

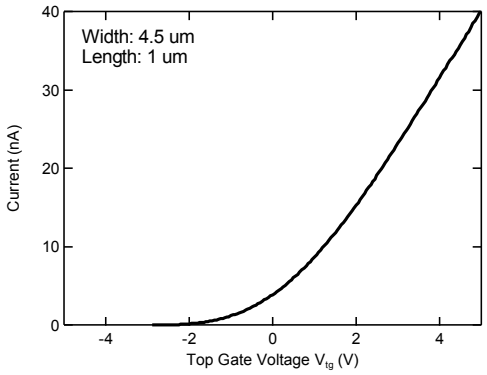

Figure 3. Gating characteristics of a top-gated FET based on large-area CVD grown MoS_2 shows n-type behavior typical of scotch-tape exfoliated MoS_2.

Extraction of Near Interface Trap Density in Top Gated Graphene Transistor Using High Frequency Current Voltage Characteristics.

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Graphene as a material has created a lot of interest due to properties like high saturation velocity [1], high current carrying capacity, ambipolar characteristics [2] and high transconductance. These properties make graphene based transistors a promising candidate for high frequency applications. Recently, there have been [2-3] demonstration of RF mixers with graphene transistors. Traditional DC measurements are not sufficient when considering graphene transistors for high frequency circuit design, making it essential to study the transistor IV performance at operating frequencies >GHz. In this work we outline an RF IV extraction technique and use physics based analytical model to evaluate the performance of graphene transistors with HfO_2 high-κ dielectric.

Figure 1 shows an SEM micrograph of the fabricated transistor on quasi-free-standing graphene (QFEG). QFEG is prepared on (0001) oriented 6H-SiC substrates through a combination of sublimation and hydrogen intercalation [4]. The sublimation of Si takes place at 1625°C for 15 minutes under a 1 Torr Ar ambient, while hydrogen intercalation follows at 1050°C for 120 minutes in a 600 Torr Ar/H_2 mixture, producing monolayer and bilayer QFEG. Ti (10 nm)/Au (100 nm) contacts are used as source/drain metallizations, after which gates are prepared. HfO_2 dielectric (10 nm thick) was deposited using an oxide seeded ALD (O-ALD) technique previously described in detail elsewhere [5].

The DC transfer characteristics of a 750nm gate length device are shown in Figure 2a. Figure 3a and 4a shows the DC transconductance (*Gm*) and output conductance (*Gd*) of the measured device. For the evaluation of RF IV (fig. 2b) it is essential to first evaluate the non-linear components (*gm*, *gd*) of the small signal model representing the device at high frequency. The s-parameters for the device are measured at the desired gate and drain bias conditions. After open and short de-embedding, the s-parameters are converted into y-parameters. Figure 5 shows the real part of Y_{21} and Y_{22} de-embedded data as a function of angular frequency (ω). The Y-intercept of these curves provides us with the RF *gm* and *gd*. Figure 3b and 4b shows the extracted RF *gm* and *gd* as a function of gate and drain bias. Through the integration of the evaluated *gm* and *gd* over gate and drain bias respectively, the RF current-voltage characteristics of the graphene FET is evaluated.

The RF source to drain current, i_{on} improves by 50% and the peak RF *gm* improves by 20% compared to DC I_{on} and *Gm*. This improvement is due to reduced charge trapping in the dielectric at very high frequencies. The two primary sources of traps in transistors are interface traps and bulk dielectric traps. The trap response time of interface traps is exponentially related to the energetic distance from the band edges. For example, midgap traps are the slowest while band edge traps are the fastest. In graphene, due to the absence of a bandgap these traps can readily exchange carriers with either the valance or the conduction band. Hence, even at RF measurement frequencies, these traps are active and degrade the RF IV characteristics. Alternatively, the bulk traps in the dielectric are slow traps as they rely on tunneling of the carriers into the oxide. Figure 6 shows the occupancy (probability>0.9) of bulk electron traps extending into the dielectric for different sweep rate, by the capture of electron from the graphene conduction band. It can be seen that for RF measurement, only the traps 1~2 nm deep will be active.

The measured RF and DC transconductance was modeled (Fig. 7) using the gradual channel approximation [Eq 3-4]. The model includes the effect of effective trap density (D_{it}) [Eq1-2] [6], contact resistance and access resistance [Eq-3]. The series resistance for this device is 340 ohm-μm. The extracted effective D_{it}, $2.3x10^{13}/cm^2/eV$ (DC) and $1.8x10^{13}/cm^2/eV$ (RF), shows the reduction in active traps at RF frequency confirming that the improvement in the RF IV performance is attributed to inactive slow bulk traps.

In summary, we have demonstrated for the first time the RF IV modeling of graphene transistors with HfO_2 high-κ dielectric. The extracted RF IV shows a 50% increase in current as compared to equivalent DC IV characteristics. The increase in current and transconductance is attributed to the reduction of active bulk traps at GHz frequency.

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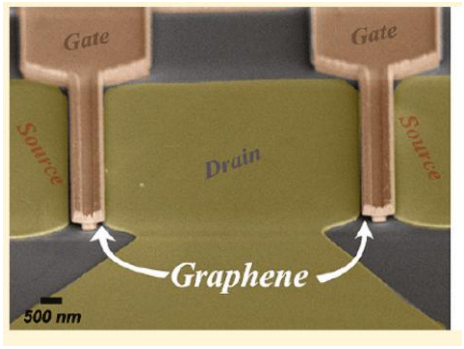

Fig. 1 SEM of fabricated graphene transistor in GSG configuration, with 10nm HfO_2 high-κ dielectric.

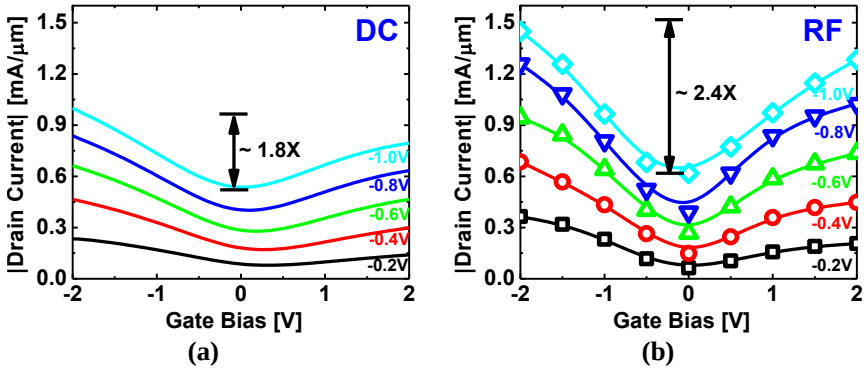

Fig. 2 (a) DC and (b) RF transfer characteristics of a 750nm gate length graphene FET. The drain bias is swept from -0.2V to -1.0V with a step size of 0.2. For the RF IV there is 1.5X increase in the drain current and 1.4X increase in the on to off ration as compared to DC IV measurement.

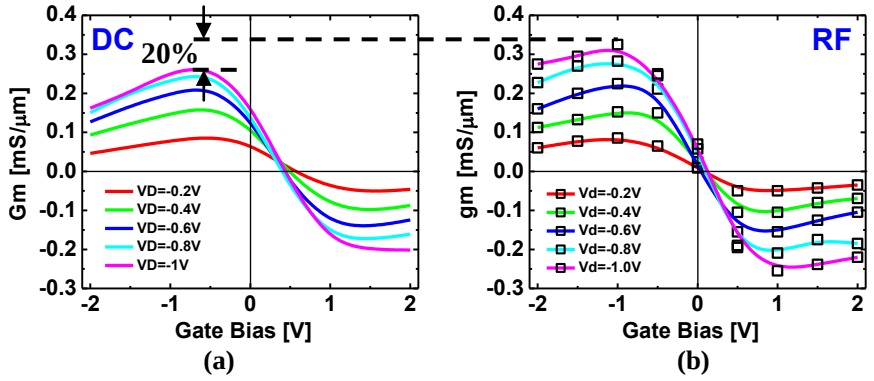

Fig. 3 (a) DC and (b) RF transconductance vs. gate bias. The peak RF *gm* is 20% higher than the peak DC *Gm*.

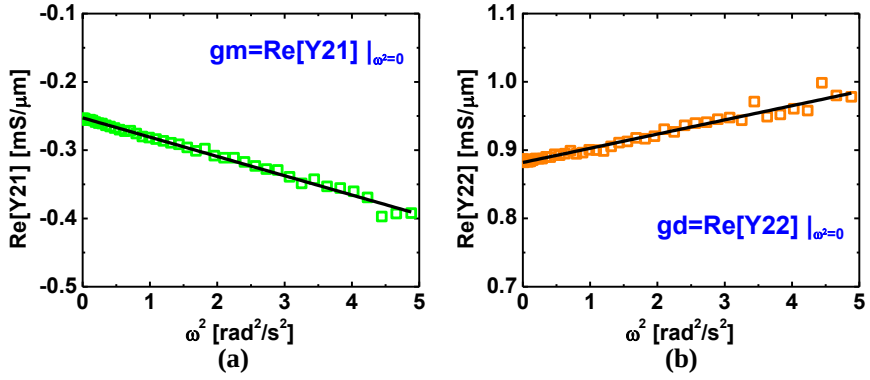

Fig. 5 Plot of de-embedded (a) $Re[Y_{21}]$ vs ω^2 and (b) $Re[Y_{22}]$ vs ω^2. The Y-intercept of $Re[Y_{21}]$ and $Re[Y_{22}]$ gives the RF *gm* and *gd* respectively. Bias condition: Vd= -1V and Vg=1V.

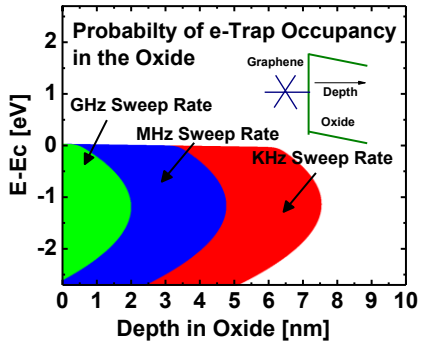

Fig. 6 The bulk electron-trap occupancy (probability >0.9), for GHz (RF), MHz and KHz (DC) sweep rate. For RF measurement the probing distance from the semiconductor oxide interface is limited to 1-2 nm.

Gradual Channel Approximation Model

$$V_0 = \left(1+\frac{q^2 D_{it}(\omega)}{C_{ox}}\right)^2 \left(\frac{\pi\hbar^2 v_f^2 Cox}{2q^3}\right) \quad \text{.....(1)}$$

$$ns = \frac{Cox}{q}\left(\begin{array}{l}\left|V_g - V_{dirac} - V_d(x)\right| + \\ +V_0\left(1-\left(1+2\frac{\left|V_g - V_{dirac} - V_d(x)\right|}{V_0}\right)^{1/2}\right)\end{array}\right) \quad \text{..(2)}$$

$$I_d = \frac{\frac{Wq}{L}\int_{Id*Rs}^{Vds-Id*Rs}\mu n(V)dV}{1+\frac{|Vds|}{E_{sat}L}} \quad \text{.....(3)}$$

$$gm = \frac{dI_d}{dVg} \quad \text{.....(4)}$$

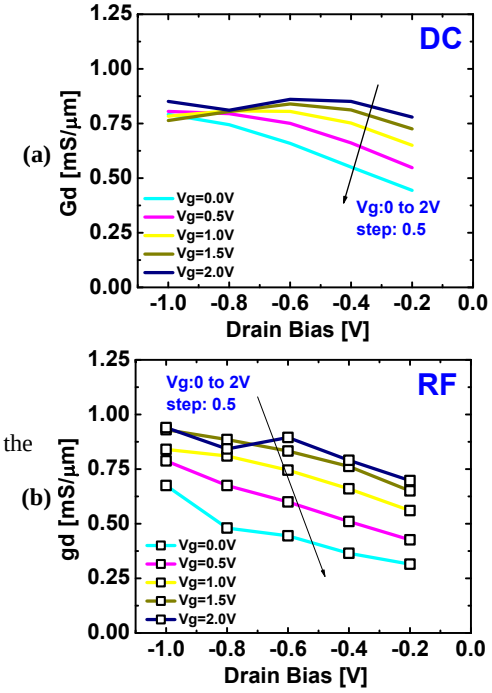

Fig. 4 (a) DC and (b) RF output conductance. Gate bias is swept from 0V to 2V with steps of 0.5V

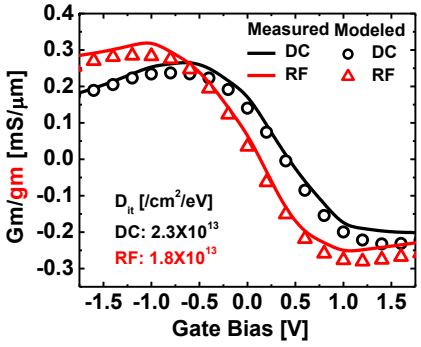

Fig. 7 DC and RF transconductance modeled using gradual channel approximation. Vd = -1V for the measurement.

Simulation Parameters

Parameters	DC	RF
Tox [nm]	10	
L [nm]	750	
V_{dirac} [V]	0.85	0.5
Rs [Ω-μm]	340	300
D_{it} [/cm²/eV]	2.3 X 10^{13}	1.8 X 10^{13}

Pulsed Nanosecond Characterization of Graphene Transistors

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We investigate the effect of pulsed current-voltage (I–V) measurements on the hysteresis and mobility of top-gated graphene field-effect transistors (GFETs). The hysteresis shift (ΔV_0) is the difference in Dirac voltage (V_0) between the forward and reverse gate voltage sweeps, primarily caused by charge trapping [1-3] at the graphene-dielectric interface. Here, we find that hysteresis can be entirely eliminated by using nanosecond pulsed testing, leading to "clean" electrical characteristics and reliable mobility extraction. In addition, we uncover several time constants in the transient trap-related response of a device.

Figures 1a-b show the typical GFET device schematic and layout used in this study. Figure 1c displays DC transfer characteristics, showing significant ΔV_0 in air and in vacuum. The presence of hysteresis in both cases suggests that both ambient adsorbates (e.g. water) and dielectric interface traps contribute to the measured hysteresis, as previously suggested [1-3]. Next, we use a pulse generator to simultaneously apply voltage pulses at the drain (V_D) and top gate (V_{TG}) of the GFET [4]; we measure the drain current (I_D) with an oscilloscope from voltage drops on load resistors in a simple circuit (not shown). Figure 2 displays the transient behavior as a 50 µs pulse is applied at V_D = 2 V (V_{TG} = 0 V). I_D reaches full steady state after ~15 µs, indicating the time it takes to completely fill all interface traps for this bias condition. The presence of two time constants at ~1 and 10 µs suggests two different trap mechanisms; the shorter is associated with the top dielectric (AlO_x) and the longer with the supporting dielectric (SiO_2) [2]. (The thermal time constant of such devices is of the order ~50 ns, much shorter than the trapping times.)

Figure 3a displays measured transfer characteristics for different V_{TG} pulse widths (pw_{TG}) and compares them with the simple DC characterization. As the pw_{TG} decreases, the forward and reverse sweeps collapse onto one another and the hysteresis voltage disappears. The hysteresis ΔV_0 extracted from each curve is shown in Fig. 3b as a function of pulse width. We note that for pulse widths $pw_{TG} \leq$ ~500 ns, the hysteresis ΔV_0 approaches 0 V. This suggests that the shortest trapping times are longer than 500 ns (consistent with Fig. 2), and that such short pulses avoid most trap-filling, leading to higher drain current values and cleaner characteristics.

We apply this method to extract effective hole mobilities (μ_h) from the measured transfer characteristics. The mobility is obtained by fitting a transport model to the experimental I_D–V_{TG} characteristics after subtracting the contact resistance (R_C ~ 2.5–3 kΩ·µm) [5,6]. The top-gate capacitance (C_{TG}) was estimated by sweeping the top-gate Dirac voltage against the back-gate voltage (Fig. 4) [7], giving ε_{TG} ~ 5.7 for the thin AlO_x (obtained by atomic layer deposition on an Al seed layer [7]). We note that mobility values are approximate since R_C and C_{TG} are both fitted and not directly extracted. Nevertheless, this exercise illustrates the consistency and reliability of such pulsed characterization vs. simple DC measurements. Figure 5a shows the hole mobility dependence on carrier density for 400 ns pulses (red) and DC measurements (black), from forward (FW) and reverse (RV) sweeps. The pulsed measurement extracts consistent mobility values, whereas with DC measurements the mobility appears (incorrectly) to be a function of sweep direction. Figure 5b shows the extracted µ dependence on pw_{TG} for three carrier densities: 0.7, 1, and 5×10^{12} cm^{-2}; open circles and solid diamonds represent values from the FW and RV sweeps. The mobility range from DC measurements (top and bottom lines) has an uncertainty up to 1000 $cm^2V^{-1}s^{-1}$ (or ~30%), while for pulsed characterization this uncertainty is significantly smaller (~50 $cm^2V^{-1}s^{-1}$ or <1%). The mobility is slightly higher at shorter pulses, likely due to the minimized trapped charge.

In conclusion, hysteresis of GFETs can be entirely eliminated with pulsed measurements of widths < ~500 ns, shorter than the trap time constants associated with the top and bottom dielectrics (1-10 µs). We also report transfer characteristics and mobility values that do not depend on voltage sweep direction (i.e. forward or reverse) or rate. Such results "correctly" represent the intrinsic properties of the GFET channel, as detrimental effects from oxide and interface traps (hysteresis and I_D degradation) can be eliminated.

[1] H. Wang et al, *ACS Nano* 4, 7221 (2010). **[2]** Y.G. Lee et al, *Appl. Phys. Lett*. 98, 183508 (2011). **[3]** D. Estrada et al, *Nanotechnology* 21, 085702 (2010). **[4]** I. Meric et al, *Nano Letters* 11, 1093 (2011). **[5]** M.-H. Bae et al, *ACS Nano* 10, 7936 (2011). **[6]** V.E. Dorgan et al, *Appl. Phys. Lett.* 97, 082112 (2010). **[7]** S. Kim et al, *Appl. Phys. Lett.* 94, 062107 (2009).

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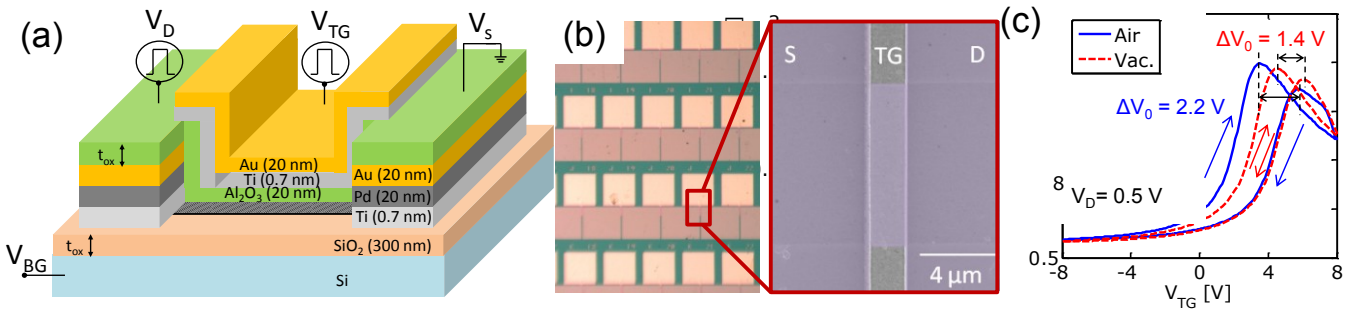

Fig. 1. (a) Schematic of top gated GFET. The graphene is obtained from chemical vapor deposition (CVD) on Cu; the device is fabricated by optical lithography with materials as shown. **(b)** Optical (left) and SEM (right) pictures of array of devices and close-up of channel, source (S), drain (D) and top gate (TG) electrode. **(c)** Hysteresis seen in DC measurement of resistance (R) vs. top gate voltage (V_{TG}) of a typical device ($L\times W = 2\times10$ μm) in air (blue-solid) and in vacuum (red-dashed). Arrows indicate forward and reverse sweeps. The hysteresis is marked as $\Delta V_0 = 3.2$ V and 1.8 V in air and in vacuum, respectively ($V_D = 0.5$ V).

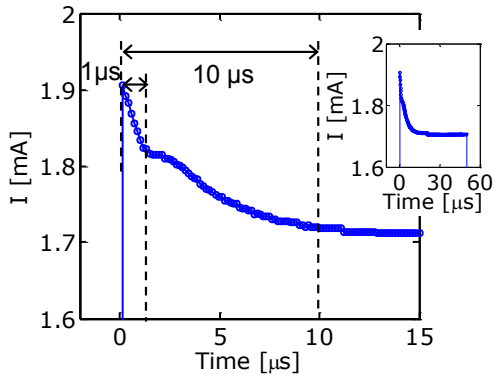

Fig. 2. Drain current monitored during first 15 μs of a 50 μs $V_D = 2$ V pulse (inset), in air. $L\times W = 2\times10$. I_D shows a transient due to population of dielectric charge traps. Two decay time constants distinguished at ~1 μs and ~10 μs, corresponding to traps in the top and bottom dielectric, respectively [2] (the thermal time constant is much shorter, ~50 ns). The current reaches steady state when all traps are filled, after > ~15 μs.

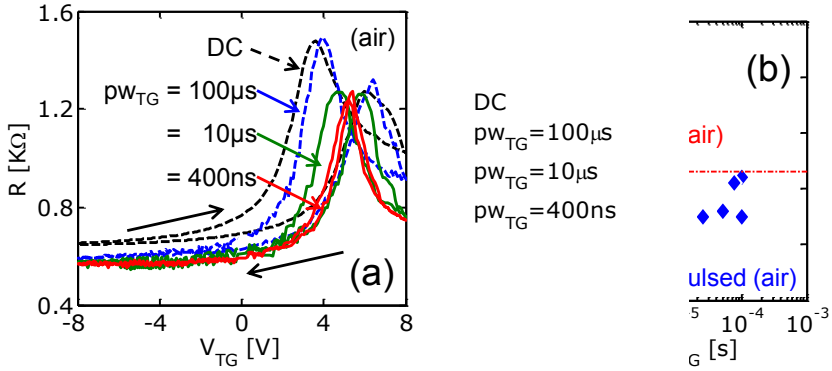

Fig. 3. (a) Typical R-V_{TG} characteristics of a device measured in air using DC (dashed lined) and pulsed configurations (solid lines). Pulses are applied at both the gate and the drain, such that the top gate pulse width (pw_{TG}) was twice the width of the drain pulse (pw_D): $pw_{TG} = 2pw_D$. Note the suppression of hysteresis between forward and reverse sweeps as pw_{TG} decreases. $V_D = 0.5$ V, $L\times W = 2\times10$ μm. **(b)** Measured shift in Dirac voltage (ΔV_0) as a function of pw_{TG} (blue diamonds) compared to Dirac voltage shift obtained from static DC measurement (red dashed line). Hysteresis is fully suppressed at pulse widths < ~500 ns.

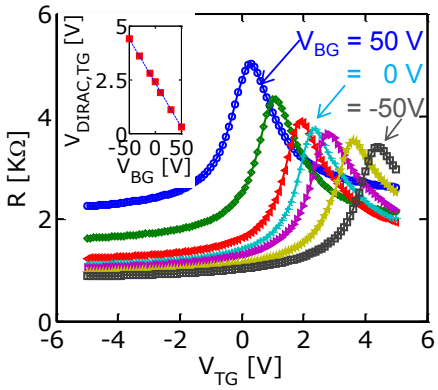

Fig. 4. Measured R vs. V_{TG} for different back gate voltages (V_{BG}). Device dimensions $L\times W = 5\times5$ μm. Inset shows the position of $V_{Dirac,TG}$ at different V_{BG}. The slope represents the ratio between the top-gate and back-gate capacitances $C_{TG}/C_{BG} \approx 22$. C_{TG} and ε_{TG} calculated as in [7] and used for mobility extractions. Only forward sweep shown.

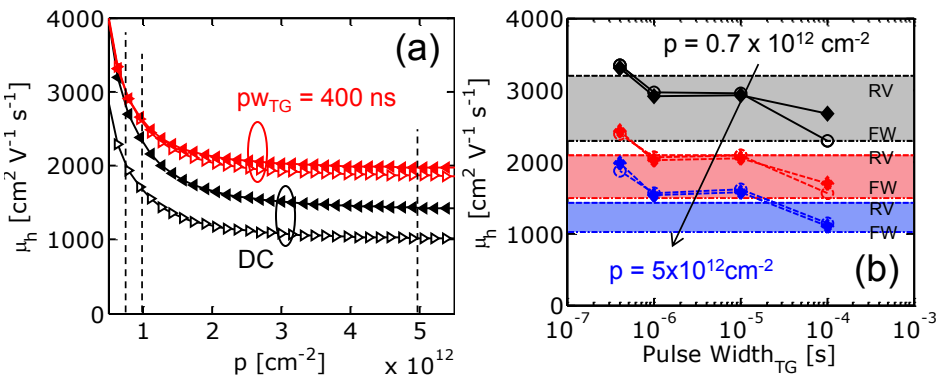

Fig. 5. (a) Extracted hole mobility (μ_h) from Figure 3a, as a function of carrier density (p) with $pw_{TG} = 400$ ns (red) and DC measurements (black). Forward and reverse sweeps shown with open right and solid left triangles respectively. **(b)** μ_h vs. pw_{TG} for different carrier concentrations: 0.7 (black), 1 (red), and 5×10^{12} cm^{-2} (blue). Values extracted from panel (a) at the marked (vertical dashed lines) concentrations. Open circles and solid diamonds are from forward (FW) and reverse (RV) pulsed sweeps respectively. Values extracted from DC FW and RV sweeps mark limits of shaded regions. Note the large mobility uncertainty of DC sweeps (up to ~1000 cm^{2}V^{-1}s^{-1} or ~30%) compared to pulsed sweeps (~50 cm^{2}V^{-1}s^{-1} or <1%).

Graphene Nanomesh Contacts and Its Transport Properties

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Introduction: Because of the absence of a bandgap in graphene, scientists recently started exploring various novel graphene based meta-materials that are defined through patterning of the two-dimensional (2D) graphene sheet. Among those, graphene nanomeshs (GNMs) have received considerable attention since they offer the potential of gap formation [1,2,3] possibly without the detrimental impact of edge effects [4].Most work in this context has focused on using GNMs formed on single layer graphene (SLG) as FET channels.Here we are presenting for the first time a study that combines the advantages of GNM with the use of few layer graphene (FLG). In particular, by creating the nanomesh structure in the contact area of the FLG, we are able to achieve two previously unrealized feats: 1) We obtain a substantially reduced contact resistance through the contact to multiple graphene layers and 2) we are able to observe on/off current ratios that rival those in SLG FETs. Based on these findings and a detailed study comparing the impact of scattering in GNM FETs and conventional graphene FETs, we are concluding that FLG FETs with GNM contacts are an excellent choice for future generations of graphene based devices.

Experiment and Results: Devices under study were prepared from mechanically exfoliated graphene on top of a 90nm SiO_2/p++ Si substrate. E-beam lithography is employed to define source/drain electrodes and nanomesh structures followed by O_2 RIE etching. Fig. 1 shows an SEM image and a cross-sectional schematic of a GNM FET. The temperature dependence of transfer characteristics for a graphene and GNM device are presented in Fig. 2. The graphene and GNM devices were fabricated on the same SLG flake for direct comparison. The graphene device in Fig.2a exhibits a sharp Dirac point close to Vg ≈0V indicating a pristine channel without much chemical doping. Away from the Dirac point, we observe both, long range Coulomb scattering and short range disorder scattering. It is expected that the short range disorder increases with temperature [5], which explains why the characteristics become increasingly sub-linear with increasing T. In contrast, the temperature dependence in the GNM device, shown in Fig.2(b), is only pronounced around the Dirac point,with the current increasing by a factor of 2.5 from 77K to room temperature. Next, we compare the conductivity of the SLG FET and the GNM FET at both, the Dirac point and the on-state, as shown in Fig. 3. For SLG, the thermally excited carrier concentration at the Dirac point can be estimated as $(T/\hbar v_F)^2$, which is much smaller than the electron-hole puddle density introduced by the SiO_2 substrate for the entire temperature range under investigation. Fig. 3(c) illustrates the potential landscape close to the Dirac point, with a variation on the order of 40meV. Consequently, a weakly temperature dependent Dirac point conductivity, ~200μS, was observed in the graphene device as shown in Fig. 3(a). On the other hand, we have observed a much lower (10X) Dirac point conductivity which is increasing with temperature for the case of GNM FETs. The dimensions of our GNM structure (20nm neck width and 60nm pore diameter) are relatively small compared to that of the electron-hole puddles (diameters of ~25nm with periodicities of several hundred nm [6]). "Bypassing" puddles embedded in the substrate, GNM FETs are able to exhibit their intrinsic carrier concentration at the Dirac point, an aspect previously unnoticed. Fig.3(b) compares the on-state conductivities of the two systems. A decrease of the conductivity with increasing temperature in SLG FETs indicates phonon scattering dominated carrier transport. Note that we did not observe any sign of decrease in GNM's on-state conductivity with increasing temperature. Our comparison clearly shows that temperature dependent scattering in GNMs is substantially weaker than in SLGs. The on-off ratio of the GNM FET increases from 10 at room temperature to 25 at 77K, whereas for SLG FETs it only mildly increases from 5 to around 7, as illustrated in Fig. 3(d).

Now we turn to FLG. FLG FETs are found to be less noisy [7, 8] and offer longer spin diffusive length [9] than SLG devices. However, it is understood that current flow in FLG FETs is typically dominated by the "top layer", the one in direct contact with the source/drain electrodes, and thus does not offer a big advantage in terms of current drive. Moreover, on-off ratios in FLG FETs are substantially smaller than in SLG FETs because of the screening of the back gate field through the stack of graphene layers at the on-state. In ref [7], Sui et al., pointed out that while the off-state conductance of FLG FETs increases with the number of graphene layers assuming that increasing graphene layers contribute to the total conductance, the on-state conductance shows a decreasing trend despite the fact that more graphene layers are added [7]. In our experiment, the number of graphene layers was identified by the relative intensity of reflected green light [9] and verified by AFM and Raman, as shown in Fig. 4. Different from conventional FLG FETs, our few layer GNM devices show a linear increase of conductivity with increasing layer number, for both on-state and off-state, as shown in Fig. 5(a). As illustrated in Fig. 5(b), the entire few layer graphene flake was patterned with the nanomesh pattern and source/drain contacts were defined on top. This ensures that the source/drain metal can contact all graphene layers through the pores in the nanomesh and all layers contribute to the total conductance even in the device on-state. Next, in order to directly compare the quality of GNM and conventional contacts, we have fabricated devices using GNM as contacts only. A pair of devices was fabricated on the same 5-layer graphene flake, as shown in Fig. 6(a). Both of the devices have unpatterned 5-layer graphene channels, while the top device has patterned GNM structures in the contact areas and the bottom device uses conventional contacts. The measured resistance as a function of gate voltage plot is provided in Fig. 6(b) for both devices. An on-off ratio close to 5 is observed in the GNM contacted device, which is much larger than the on-off ratio of 2 in the device with conventional contacts. Since the contact resistance is much smaller than the off-state resistance, we can correct for the channel length and contact area difference in the two devices. Fig. 6(c) shows the normalized resistance plot for comparison, which clearly indicates a much lower contact resistance in the GNM device. In addition, the improved on-state performance results in a greater on-off ratio.

Summary: In this work, we have studied GNM as both FET channel and contact material. We find that the FET performance in terms of on-off ratios is always improved with GNM patterning, due to the modified scattering in the GNM channel and improved channel coupling in the GNM contact case. In particular, our findings suggest that a novel graphene based device using an FLG channel with GNM contacts is able to achieve high performance, low noise and high reliability for various electronic applications.

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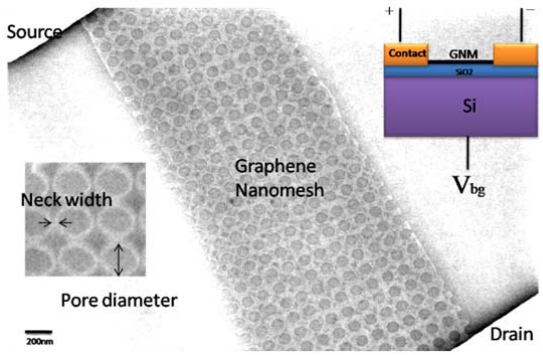

Fig. 1 Top-view SEM images of a GNMFET with pore diameters of 120nm and neck widths of 40 nm. Top-right inset is a cross-sectionalschematic.

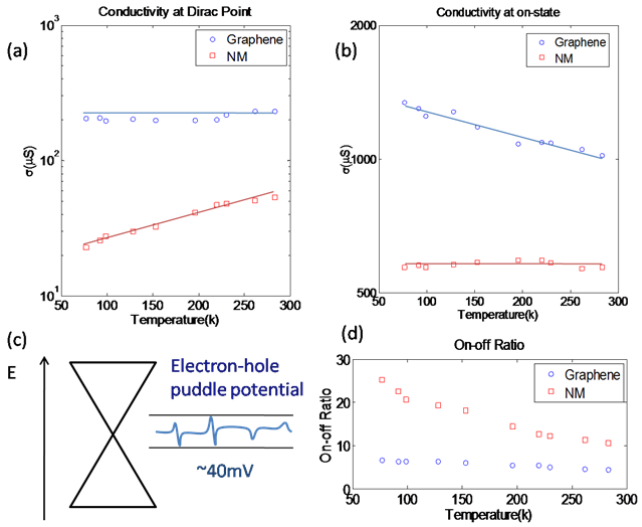

Fig. 3 Temperature dependence of (a) Dirac point conductivity(b) on-state conductivity (d) on-off ratiosof a SLGFET(blue)and GNMFET (red). The on state is defined at $V_{gs} - V_{Dirac}$ =-30V. (c)Electron-hole puddle potential landscape in SiO_2 substrate.

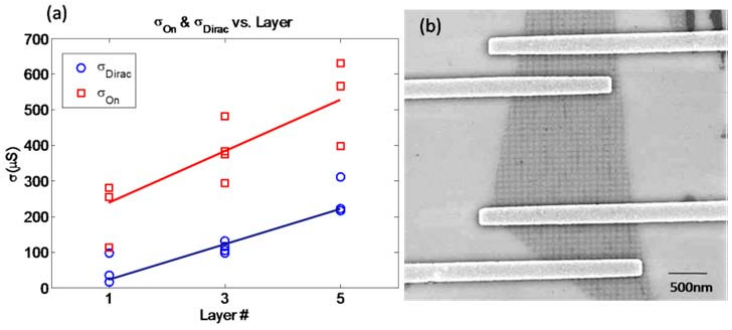

Fig. 5 (a) Conductivity σ_{on} and σ_{off} of GNMFET as a function of layer number. (b) SEM image of a few layer GNMFET.

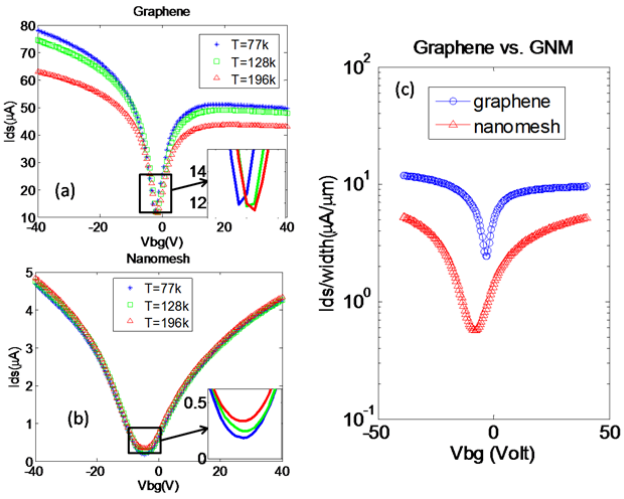

Fig. 2 Temperature dependence of transfer characteristics of a (a) graphene and (b) GNMdevice on the same SLG flake (c) Comparison of the transfer characteristics in a log plot.

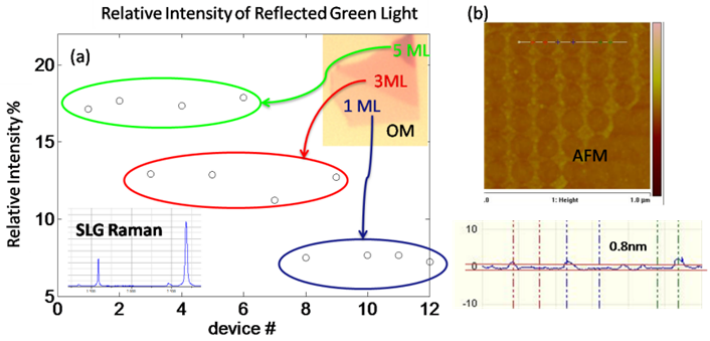

Fig. 4(a) Number of graphene layers identified by the relative intensity of reflected green light and (b) AFM image of a GNM. Inset shows Raman spectrum of a SLG.

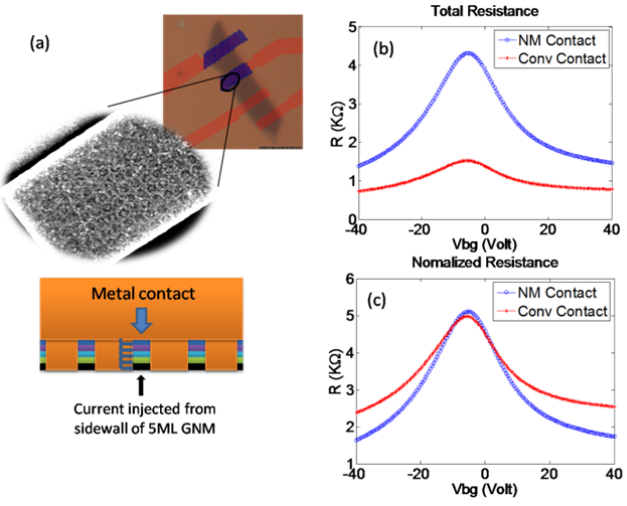

Fig. 6(a) 5-layer graphene devices with GNM contacts (top) and conventional contacts (bottom).SEM image of the contacts shows GNM structures underneath the metal. (b) TotalResistance and (c) Normalized resistance of 5-layer graphene devices with GNM contacts and conventional contacts.

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First Demonstration of Two-Dimensional WS_2 Transistors Exhibiting 10^5 Room Temperature Modulation and Ambipolar Behavior

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Spurred by the knowledge of isolation of graphene, other 2D transition-metal dichalcogenide materials in the form of MX_2 (where M=transition metal such as Mo, W, Ti, Nb, etc. and X=S, Se, or Te) have drawn considerable attention. The MX_2 family material consists of one or more sets of triple layers with one M and two X in a sandwich structure (X-M-X). Atoms within each layer are strongly held together by covalent-ion mixed bonds, while interlayer van der Waals forces are weak. Prior investigations of 2D materials have concentrated on optical properties [1]. Field-effect transistors (FETs) in MoS_2 and WSe_2 have been demonstrated with substantial gate modulation and stable current saturation [2, 3]. A recent calculation shows that the single layer WS_2 has the potential to outperform Si and other 2D crystals in FET-type applications due to its favorable bandstructure [4]. No prior device results have been reported for WS_2 for logic or optical devices. Here we report the first fabrication and demonstration of 2D WS_2 FETs and explore the effects of photosimulation on the transistor characteristics.

A schematic cross section image of the back-gated WS_2 device is shown in Fig. 1(a). The source and drain contacts are defined by electron beam lithography (EBL) using Ti/Au (5/100 nm) contacts. The optical image of the WS_2 device with L/W = 2.5/5 μm is shown in Fig. 1(b). The Raman spectra (λ = 488 nm) of the WS_2 region shown in Fig. 1(c) shows two peaks: one in the $E_{2g}{}^1$ range at ~356 cm^{-1} and the other in the A_{1g} range at ~421 cm^{-1}. The 2D Raman signal is fit to two single Lorentzian models, revealing that the chemical vapor deposited (CVD) 2D WS_2 retains the single crystal properties of WS_2 with unnoticeable structural modifications. The energy band line-ups of Fig. 1(d) indicate that the Fermi level of the contact metal is aligned in the band gap of WS_2. Figure 2(a) shows drain current versus gate-source bias, I_D *vs.* V_{GS}, at room temperature for a multilayer WS_2 FETs at two drain biases. The gate modulation is ~10^5× for V_{DS} =1 V, and ~10^4× for V_{DS} =5 V. The device shows clear ambipolar behavior indicating accumulation of electrons (*n*-type conductivity) for positive V_{GS} and of holes (*p*-type conductivity) for negative V_{GS} regions. Thus, electrons or holes are preferentially injected depending on the gate bias as illustrated in Fig. 2(b) and 2(c), as a consequence of the Schottky contacts. This is seen clearly in the family of I_D - V_{DS} curves in Fig. 2(d). The photoresponse of the WS_2 Schottky barrier FETs was measured by illuminating the device with a halogen lamp; the result is shown in Fig. 3(a). The image of Fig. 3(b) shows a schematic representation of electron-hole pair generation upon photon absorption, and the increase of drain current due to conduction by these excess carriers. We observe that the saturation drain voltage increases under illumination which can be attributed to the photogeneration of carriers which require greater drain voltage to achieve pinch-off in the channel near the drain. Figure 3(c) shows multiple cycles of the transient photocurrent response under monochromatic illumination at two wavelengths, corresponding to photon energies of 2.1 eV (580 nm) and 1.9 eV (650 nm), both of which are above the expected bandgap of monolayer WS_2 (~1.8 eV).

In summary, two-dimensional (2D) WS_2 transistors were fabricated and characterized for the first time from chemically-synthesized material. Raman measurements confirm the 2D crystal nature of the material, and the presence of a bandgap leads to high on/off current ratios and current saturation in the transistors at room temperature. In addition, the observed photoresponse of the 2D layered semiconductor can enable optical device applications.

This work was supported by the Semiconductor Research Corporation (SRC), Nanoelectronics Research Initiative (NRI) and the National Institute of Standards and Technology (NIST) through the Midwest Institute for Nanoelectronics Discovery (MIND), and by the Office of Naval Research (ONR) and the National Science Foundation (NSF). We thank J. Jelenc for technical help in crystal growth, Slovenian Research Agency of the Republic of Slovenia for financial support, contract no. J1-2352, and the Centre of Excellence NAMASTE.

[1] M. Krause, et al., *Status Solidi B***246**, 2786 (2009). [2] B. Radisavljevic, et al., *Nat. Nanotechnol.* **6**, 147 (2011). [3] V. Podzorov, et al., *Appl. Phys. Lett.* **84**, 3301 (2004). [4] L. Leitao, et al., *IEEE T. Electron dev.* **58**, 3042 (2011).

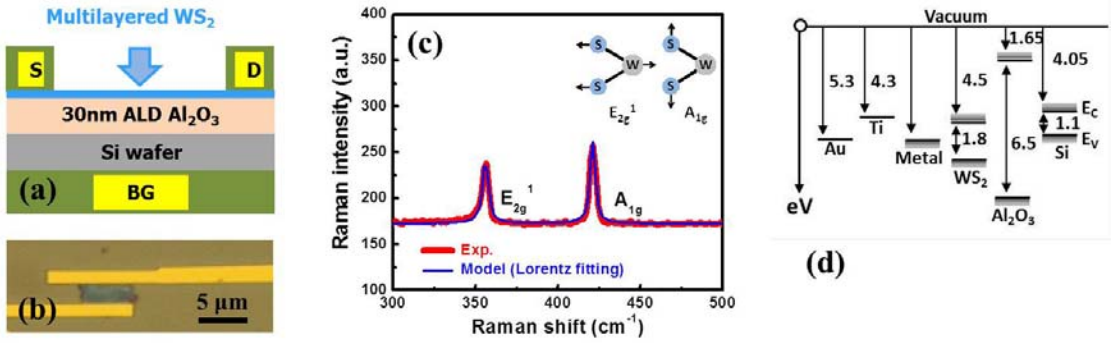

FIG. 1. (a) Schematic cross-section, (b) optical image of the WS_2 transistor with Ti/Au contacts. (c) Raman spectra (λ = 488 nm) of the multilayered WS_2. The inset shows the two primary vibrational modes of WS_2 leading to the two peaks in the Raman spectrum. (d) Work function, electron affinities, and bandgaps of each element indicating the formation of a Schottky barrier contact between metal and WS_2.

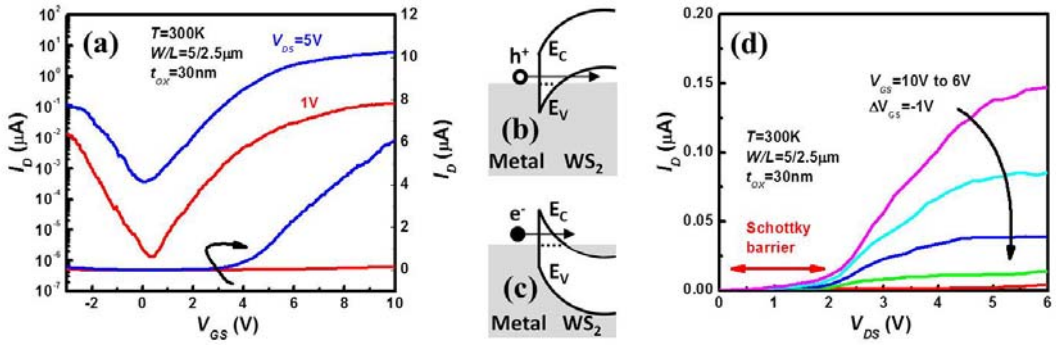

FIG. 2. (a) Drain current I_D *vs*. gate-to-source voltage V_{GS} showing ~10^5× on/off current ratio and ambipolar behavior. Schematic image of (b) accumulation of holes (*p*-type conductivity) at negative V_{GS} and (c) accumulation of electrons (*n*-type conductivity) at positive V_{GS}. (d) Common-source transistor characteristics, I_D *vs*. V_{DS} indicating the presence of Schottky barrier limited-current injection and current saturation.

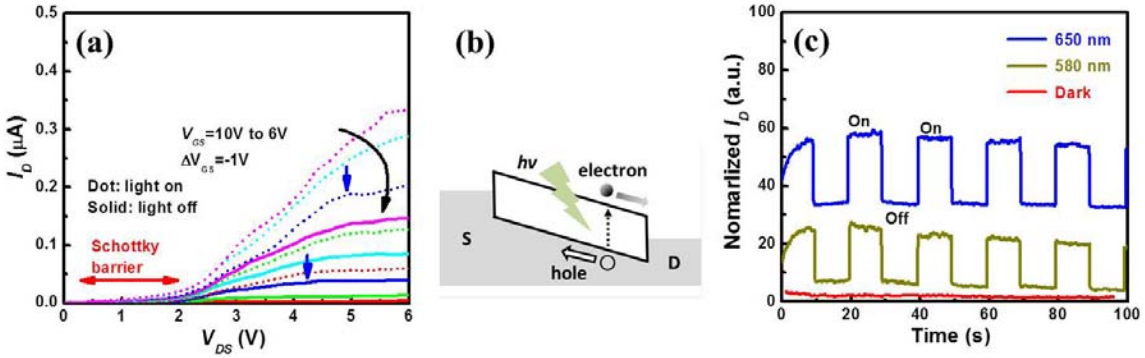

FIG. 3. (a) Dependence of WS_2 common-source characteristics on illumination. (b) Schematic representation of electron-hole pair generation by photon absorption, (c) The temporal photocurrent response of 2D WS_2 device at V_{DS} = 5 V and V_{GS} = 0 V at two wavelengths.

Low-frequency Noise in Contact and Channel Regions of Ambipolar InAs Nanowire Transistors

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Semiconductor nanowires are promising candidates for nanoelectronic applications such as high-speed electronics, chemical sensors, and transparent electronics. However, practical application of these devices is hindered by the excessive levels of low-frequency (1/f) noise. The general physical model of 1/f noise stems from carrier interactions with the surface oxide along the channel, but the problem is exacerbated in nanowires because of their high surface-to-volume ratio. However, other mechanisms may also contribute to carrier fluctuations leading to higher levels of noise, such as fluctuations in the metal-semiconductor source and drain contacts. Understanding the physics and contributions from the different regions is key to optimizing noise in nanowire devices, but few studies have distinguished between these mechanisms.

In this study, 30nm diameter InAs nanowires were grown by the VLS method, then made into back-gated transistors by dispersing the wires on a silicon wafer topped with 20 nm silicon dioxide for the gate. Nickel source and drain contacts were then deposited onto each wire. Channel lengths were varied between 100 nm and 1000 nm to study the effects of contacts on noise levels. The devices were biased as n-channel (V_{ds}>0) devices, and current-voltage (I-V) characteristics were measured. The measured data shows on-currents of several microamps in the on-state, plus ambipolar (p-branch) conduction at highly negative gate voltages. The p-branch behavior is caused by band-to-band tunneling of electrons out of the valence band directly into the drain at large negative gate bias and high drain bias. By observing the device resistance as a function of channel length, it can be seen that the n-branch shows a strong length-dependence on resistance, but the p-branch which depends primarily on the drain contact is not influenced by channel length.

Noise levels were measured at varying gate bias points for several device lengths. By observing the gate dependence of the normalized noise data A (S_I/I^2), noise contributions from the channel and the contacts can be separated. For the n-branch, a region with $A \sim V_{gs}^{-1}$ is observed for small V_{gs}-V_t values, indicating that the channel is dominating noise, and a region with $A \sim V_{gs}^{0}$ is observed for larger V_{gs}-V_t values, indicating that the noise is dominated by contact contributions. Similarly, the device resistance can be dominated by either channel or the contacts for lower or higher V_{gs}-V_t values, respectively. In the bias region where the contacts dominate, there is little variation between devices of different lengths, but in the region where the channel dominates, the shorter devices show much higher noise levels. In the p-branch, the current is limited by tunneling through the drain contact, and shows little length dependence for any bias, except for the shortest 2 devices which are influenced by short-channel effects.

It is clear that three different noise mechanisms are at work in these devices. At gate voltages above but near threshold, the interface trapping along the channel is the dominant mechanism. At higher gate voltages, once the channel is fully activated, fluctuations in the contacts are the dominant mechanism. At gate voltages far below threshold into the p-branch region, noise depends on fluctuations in the band-to-band tunnel barrier of the drain contact.

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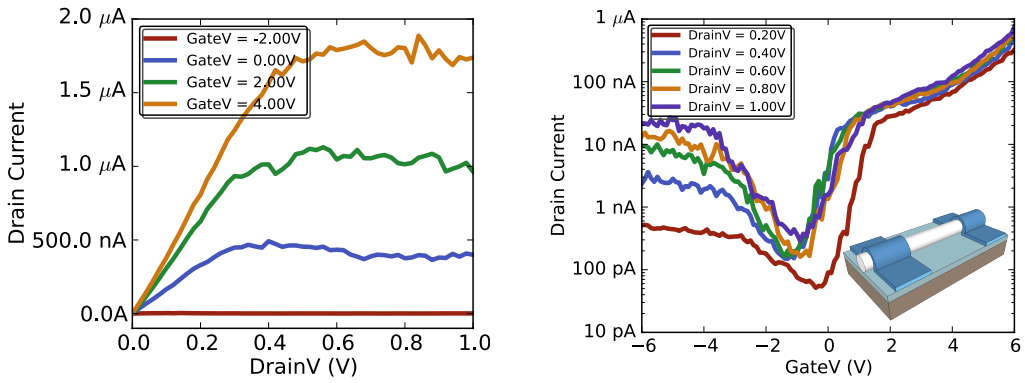

Fig 1. I-V characteristics for representative device showing ambipolar behavior. Inset shows structure of the back-gated devices.

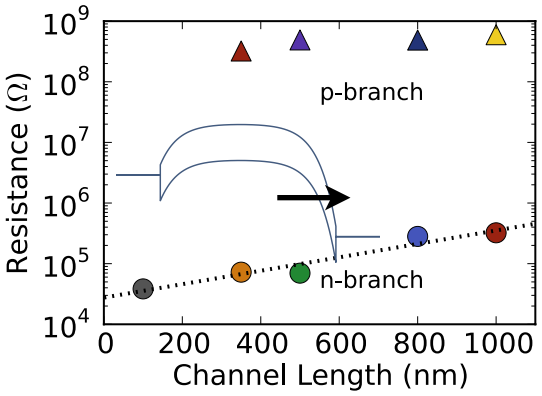

Fig 2. Resistance vs. Length in n-branch and p-branch. Inset shows band diagram of p-branch conduction mechanism.

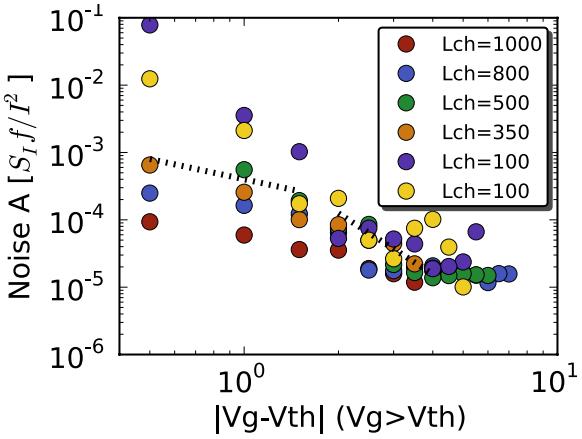

Fig 3. Noise amplitude in n-branch, showing length dependence when contacts ($A \sim V_g^0$) and channel ($A \sim V_g^{-1}$) dominate transport.

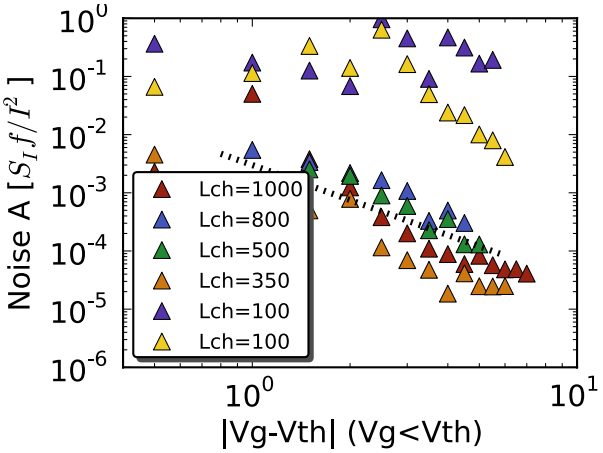

Fig 4. Noise amplitude in p-branch, showing length independence except for shortest devices.

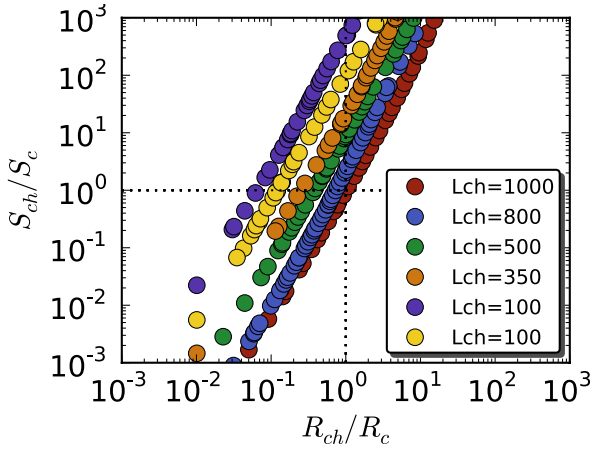

Fig 5. Channel noise / contact noise vs channel resistance / contact resistance. Each quadrant represents the channel or contact dominating the resistance or noise. Shorter lengths appear farther to the left, indicating higher contact influence on noise and resistance.

Session V.A (Dean's Hall I)

MOSFETs/FETs

Tuesday PM, June 19th, 2012

Session Chair(s): Mitsuru Takenaka, University of Tokyo and Kirsten Moselund, IBM Zurich

1:30 PM V.A-1 Invited Paper
High Performance III-V FETs for Low Power CMOS Applications
M. Radosavljevic, Intel Corporation, Technology and Manufacturing Group, Hillsboro, Oregon, USA

2:10 PM V.A-2
Vertical InAs Nanowire MOSFETs with I_{DS} = 1.34 mA/μm and gm = 1.19 mS/μm at V_{DS} = 0.5 V
K.-M. Persson, M. Berg, M. Borg, J. Wu, H. Sjöland, E. Lind and L.-E. Wernersson, Department of Electrical- and Information Technology, Lund University, Lund, SWEDEN

2:30 PM V.A-3
Possible Observation of Ballistic Contact Resistance in Wide Si MOSFETs
A. Majumdar[1] and D. A. Antoniadis[2], [1]IBM Research Division, T. J. Watson Research Center, Yorktown Heights, New York, USA and [2]Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, Massachusetts, USA

2:50 PM V.A-4
Regrown Ohmic Contacts to InxGa1-xAs Approaching the Quantum Conductivity Limit
J. J. M. Law, A. D. Carter, S. Lee, A. C. Gossard, M. J. W. Rodwell, ECE and Materials Departments, University of California, Santa Barbara, California, USA

3:10 PM Break

3:30 PM V.A-5 Invited Paper
Simulation Study of Nanowire Tunnel FETs
A. Schenk[1], R. Rhyner[1], M. Luisier[1], and C. Bessir[2], [1]Integrated Systems Laboratory, ETH Zürich, Zürich, SWITZERLAND and [2]IBM Research-Zürich, Rüschlikon, SWITZERLAND

4:10 PM V.A-6
Flicker Noise Characterization and Analytical Modeling of Homo and Hetero-Junction III-V Tunnel FETs
R. Bijesh, D. K. Mohata, H. Liu and S. Datta, Pennsylvania State University, University Park, Pennsylvania, USA

4:30 PM V.A-7
High Current Density InAsSb/GaSb Tunnel Field Effect Transistors
A. W. Dey[1], B. M. Borg[2], B. Ganjipour[2], M. Ek[3], K. A. Dick[2,3], E. Lind[1], P. Nilsson[1], C. Thelander[2] and L.-E. Wernersson[1], [1]Dept. of Electrical and Information Technology, [2]Dept. of Solid State Physics and [3],Division of Polymer and Materials Chemistry, Lund University, Lund, SWEDEN

4:50 PM V.A-8
Gate-first implant-free InGaAs n-MOSFETs with sub-nm EOT and CMOS-compatible process suitable for VLSI
L. Czornomaz, M. El Kazzi, D. Caimi, C. Rossel, E. Uccelli, M. Sousa, C. Marchiori, M. Richter, H. Siegwart and J. Fompeyrine, IBM Zurich Research Laboratory, Rüschlikon, SWITZERLAND

High Performance III-V FETs for Low Power CMOS Applications

M. Radosavljevic
Intel Corporation, Technology and Manufacturing Group, Hillsboro, OR 97124, USA

III-V compound semiconductor based quantum well field effect transistors are in general viewed as a promising transistor candidate for future high-speed low-power logic applications due to their excellent drive current performance at low voltage. In this presentation, I will review recent device developments of n-channel InGaAs transistors. To start, well-studied Schottky gate device architecture is adopted to demonstrate integration on Si substrate [1] as well as to establish performance advantages over state-of-the-art Si NMOS at V_{CC}=0.5V [2]. To enable further L_G scaling, high quality high-K dielectric is integrated [3] and non-planar Tri-gate architecture is implemented [4]. I will conclude by discussing InSb based p-channel device results [5], as well as InGaAs based tunnel FETs [6].

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[1] M.K. Hudait et al., *IEDM Tech. Dig.*, pp.625 (2007).
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Vertical InAs Nanowire MOSFETs with I_{DS} = 1.34 mA/μm and g_m = 1.19 mS/μm at V_{DS} = 0.5 V

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III-V MOSFETs are currently considered for extension of, or as an add-on to, the Si CMOS technology. Following the Si-technology evolution, it is attractive to consider advanced III-V transistor architectures with non-planar geometry and improved electrostatic control [1]. We report on vertical InAs single nanowire FETs with diameter of 45 nm diameter, integrated on Si substrates with L_G = 200 nm. The devices demonstrate normalized extrinsic g_m and I_{DS} of 1.34 S/mm and 1.19 A/mm, respectively, at a V_{DS} of 0.5 V, and with an on-resistance of 321 Ωμm, all values normalized to the circumference. The improvements in g_m and I_{DS} as related to previous work [2] are attributed to the improved higk-κ interface consisting of Al_2O_3/HfO_2, as well as to the nanowire source resistance, which is reduced by applying an inorganic spacer layer. The main performance limitation is identified as the drain resistance in the ungated top part of the wire. By scaling the NW diameter to 28 nm, we also observe subthreshold swing down to 80 mV/decade at 50 mV V_{DS}. However, the on-resistance increases for the narrow wires to 75 kΩμm, and the normalized current level is reduced as compared to the larger diameter wires.

A 4" highly resistive Si wafer, which is overgrown with a 300-nm-thick InAs buffer layer, serves as sample substrates [3]. Electron-beam-lithography defined gold particles placed in arrays prior to epitaxial growth are made on 2x2 cm^2 pieces. Each sample has 160 FETs, both single- and multi-wire devices, with RF compatible layout. High-κ gate oxides are deposited with an ALD process consisting of 0.5 nm Al_2O_3 at 250 °C and 6.5 nm HfO_2 at 100 °C, directly after epitaxial nanowire growth. For device isolation and stray capacitance minimization, source mesas are etched out from the buffer layer. In a novel fabrication procedure, the first spacer layer, separating source and gate, is formed by plasma-enhanced-chemical-vapor-deposition of 60 nm Si_3N_4. The sputtered tungsten gate is defined using an etch mask and a dry-etch procedure. The top spacer layer separating gate and drain is made of a spin-coated organic film and has a thickness of 150-250 nm, making the ungated top part of the wire the largest fraction of the series resistance that limit the performance.

DC characterization is performed for single and multi NW InAs NW FETs, where the best single NW device of 45 nm diameter shows a normalized I_{DS} of 1.82 mA/μm and 1.34 mA/μm at a V_{GS} of 1.0 V and *a* V_{DS} of 1.0 V and 0.5 V, respectively. These devices also show a corresponding g_m of 1.45 mS/μm and 1.19 mS/μm at a V_{DS} of 1.0 V and 0.5 V, respectively. The V_t is extrapolated using the maximum transconductance method and determined to -0.27 at V_{ds} = 0.5 V. The device shows a low hysteresis of less than 5 mV at a V_{DS} of 0.5 V, most likely due to a low trap concentration within the low temperature deposited HfO_2 film. Devices scaled in diameter to 28 nm, with a 5.0-nm-thick Al_2O_3/HfO_2 film, and with 96 wires in parallel show a normalized I_{DS} of 0.112 mA/μm, a transconductance of 0.154 mS/μm, and a V_t of -0.23 V at a V_{DS} of 0.5 V and within 0.5 V V_{GS}. While the performance is lower in the on-state, the subthreshold swing is greatly improved down to 80 mV/decade at a V_{DS} of 50 mV. Data for both samples is benchmarked in Table 1 [4], demonstrating good performance as compared to alternative implementations. S-parameter measurements of our RF devices with 45 nm in diameter, show that FETs consisting of 192 wires in parallel, operate with f_t = 18.5 GHz and f_{max} = 32.2 GHz. Although these values represent a two fold increase to previous published data for InAs NW FETs [5], the performance is still limited by parasitic contact pad capacitances, originating from the limitations of the optical lithography used.

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[2] C. Thelander et al., *IEEE Electron Device Lett.*, vol. 29, no. 3, pp. 206-208, Mar. 2008
[3] S. Gorji Ghalamestani et al., *J. Crystal Growth.*, vol. 332, no. 1, pp. 12-16, Oct. 2011
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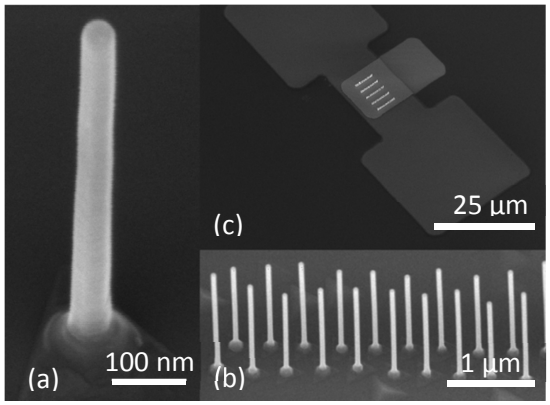

Fig 1. SEM images (30° tilt angle) of a single NW (a) and an array of NWs (b) after ALD as well as a 192 NW array with etched-out source mesa and sputtered W-gate-pad (c).

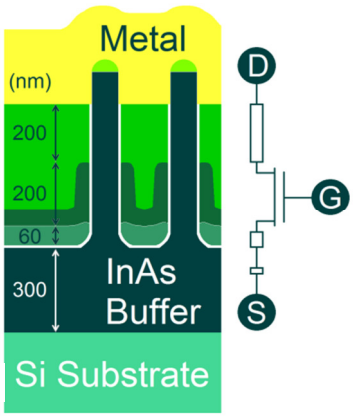

Fig 2. Schematic cross-section showing the different layer thicknesses in the fabricated device.

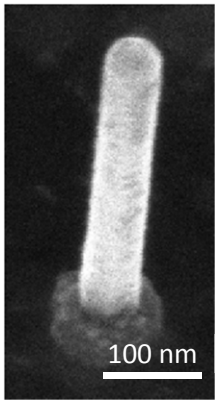

Fig 3. SEM image (30° tilt angle) of a single NW after the gate length definition.

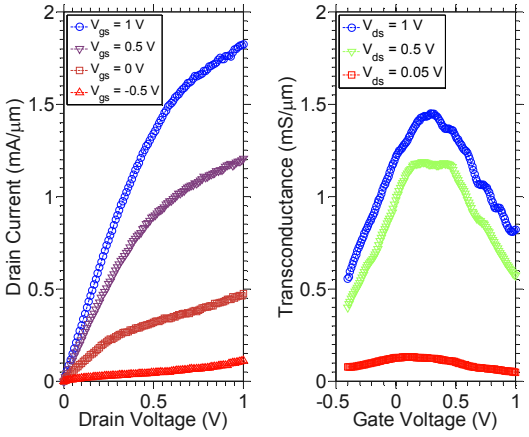

Fig 4. Normalized I_{DS} vs V_{DS} for a single 45 nm NW FET. Fig 5. Normalized g_m vs V_{GS} for a single 45 nm NW FET.

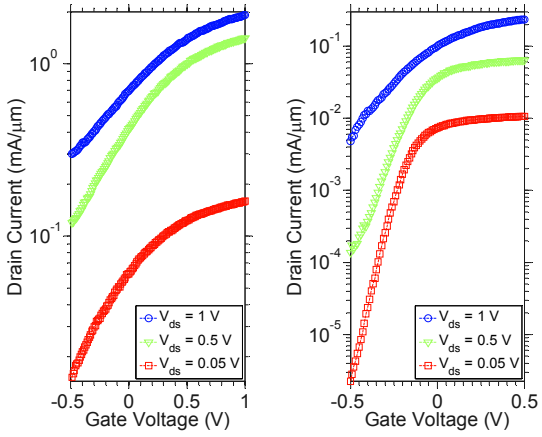

Fig 6. Normalized I_{DS} vs V_{GS} for a single 45 nm NW FET. Fig 7. Normalized I_{DS} vs V_G for a 28 nm NW array FET.

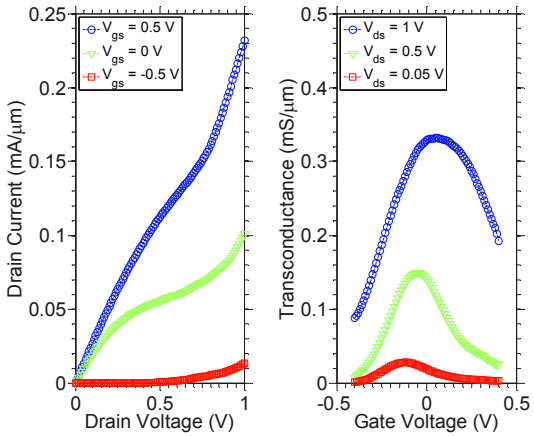

Fig 8. Normalized I_{DS} vs V_{DS} for a 28 nm NW array FET. Fig 9. Normalized g_m vs V_{GS} for a 28 nm NW array FET.

D (nm)	L_G (nm)	I_{ON} (mA/µm)	$g_{m,max}$ (mS/µm)	SS (mV/dec)	Tech	Reference
28	200	0.058	0.15	140	vertical NW	This work
45	200	0.67	1.19	560	vertical NW	This work
15	100	0.6	1.23	140	lateral NW	A. Dey et al EDL 2012
10	30	0.7	1.9	80	HEMT	D.-H. Kim et al EDL 2008
30	250	0.12	0.56	120	FinFET	J. J. Gu et al APL 2011
10	75	0.55	1.75	95	QWFET	M. Radosavljevic et al IEDM 2009
25	170	0.4	0.8	260	radial NW	X. Jiang et al Nano Lett 2007
13	230	0.9	1.72	180	XOI	K. Takei et al APL 2011

Table 1. Data benchmark for this work and other high performance technologies at a V_{DS} of 0.5 V and a V_{OD} of 0.5 V

Possible Observation of Ballistic Contact Resistance in Wide Si MOSFETs

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[2] *Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139 (daa@mtl.mit.edu)*

INTRODUCTION

Gate length L_G scaling in the Si industry has led to MOSFETs with higher on-state current I_{ON} and faster speeds. For short L_G FETs, series resistance R_{EXT} plays a major role in determining I_{ON}. It is well known that R_{EXT} exhibits a gate bias dependence. In this work, we present gate bias V_G and temperature T dependence of R_{EXT} of extremely-thin SOI (ETSOI) NFETs with channel width W = 3 μm. Based on a comparison of our data to the ballistic FET model, we argue that the V_G and T dependences of R_{EXT} for overlapped FETs are primarily due to those of ballistic contact resistance R_B.

EXPERIMENTAL

The devices used in this work are ETSOI NFETs, sketched in Fig. 1(a), with SOI thickness T_{SOI} = 6 nm, poly-Si/SiON gate stack with equivalent oxide thickness T_{OX} = 1.1 nm, and neutral stress liner, and were fabricated using an extension-last process flow with laser anneal for activating the dopants. Details of extraction of L_G and effective channel length L_E from capacitance data can be found in [1] and [2]. We extract R_{EXT} using the conventional dR/dL method with drain bias V_D = 10 mV at T = 295 K and even lower V_D = 2 mV at lower temperatures to stay within the linear ohmic regime [3].

RESULTS AND DISCUSSIONS

A plot of R_{EXT} versus sheet carrier density N_S at room temperature (T = 295 K) is shown in Fig. 2. We observe that R_{EXT} decreases by ~ 100 Ω.μm as N_S increases from 3 × 10^{12} to 1.5 × 10^{13} cm^{-2}. In terms of the conventional components of R_{EXT}, sketched in Fig. 1(b), inversion layer to source/drain extension (SDE) spreading resistance R_{SP}, and SDE resistance R_{SDE} exhibit V_G-, and the therefore N_S-dependence. However, our estimates of these dependences are on the order of 5 Ω.μm over the range of N_S [3]. Therefore, the N_S dependence of R_{EXT} at room temperature shown in Fig. 2 cannot be accounted for from known N_S dependences.

A possible explanation for the N_S dependence of R_{EXT} is the change in channel-to-SDE contact resistance in quasi-ballistic FETs. At low V_D, the on-resistance of a quasi-ballistic FET is $R_{ON} = R_{EXT} + R_{CH}(L_E) = R_{EXT0} + R_B + R_{CH}(L_E)$, where R_{EXT0} is independent of L_E and N_S, R_B is independent of L_E but dependent on N_S and called the ballistic resistance, and $R_{CH}(L_E)$ is the ohmic channel resistance [4]. The ballistic resistance R_B can be thought of as a contact resistance, and $R_B \sim 1/M$, where M is the number of transverse modes taking part in current conduction. As N_S increases, M increases, thereby leading to a decrease in R_B.

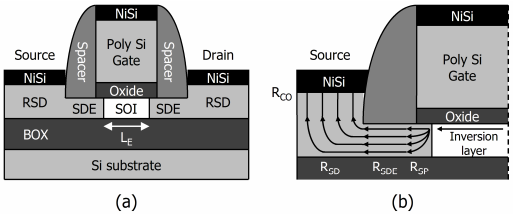

Fig. 1. (a) Schematic of ETSOI MOSFET showing the source/drain extension (SDE) region, raised source/drain (RSD), and buried oxide (BOX), and electrical channel length L_E. (b) Schematic of source side of ETSOI MOSFET depicting current flow and the associated resistances. The different components of series resistance are inversion layer-to-SDE spreading resistance R_{SP}, SDE resistance R_{SDE}, RSD resistance R_{SD}, and RSD-to-NiSi contact resistance R_{CO}.

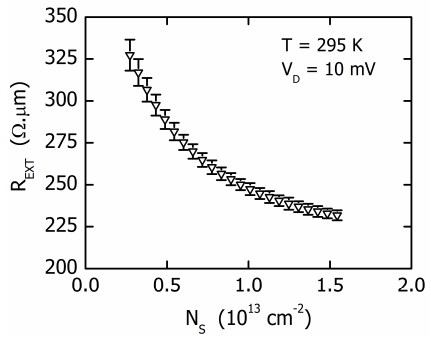

Fig. 2. Series resistance R_{EXT} versus sheet carrier density N_S of ETSOI NFETs at room temperature T = 295 K and drain bias V_D = 10 mV.

In order to investigate if the observed N_S dependence of R_{EXT} in our ETSOI devices is indeed due to that of R_B, we measured R_{EXT} versus N_S in the 25 to 295 K temperature range. The conventional components in R_{EXT} have a temperature dependence, but they are small. Nonetheless, instead of R_{EXT}, we plot $\Delta R_{EXT} = R_{EXT}(N_S) - R_{EXT}(N_S = 1.5 \times 10^{13}\ cm^{-2})$ versus N_S in Fig. 3(a) and ΔR_{EXT} versus T in Fig. 3(b) in order to naturally subtract out the T-dependent components of conventional R_{EXT}. In these figures, the symbols are measured data and show the following features: (i) at low temperatures ($T \leq$ 100 K), ΔR_{EXT} decreases rapidly with increasing N_S at low N_S and decreases slowly with increasing N_S at high N_S, and (ii) ΔR_{EXT} exhibits little T dependence at high N_S while it keeps decreasing with T at low N_S. As discussed next, all these features can be explained quantitatively by the N_S and T dependence of ballistic contact resistance R_B.

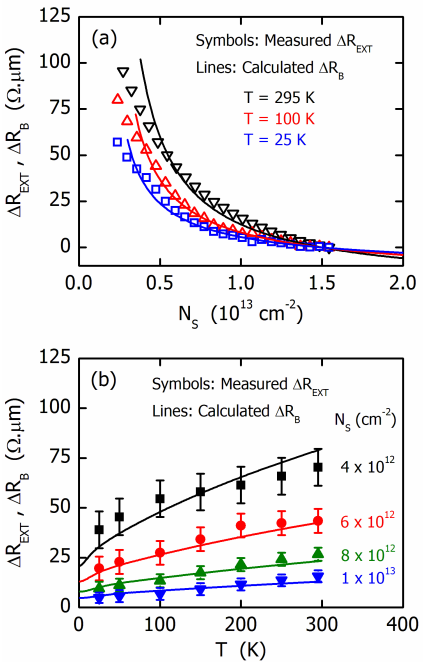

Fig. 3. Change in series resistance ΔR_{EXT} and ballistic contact resistance ΔR_B versus (a) carrier density N_S and (b) temperature T of ETSOI NFETs, where $\Delta R_{EXT} = R_{EXT}(N_S) - R_{EXT}(N_S = 1.5 \times 10^{13}$ cm$^{-2})$ and $\Delta R_B = R_B(N_S) - R_B(N_S = 1.5 \times 10^{13}$ cm$^{-2})$. Error bars in (a) are similar to those in Fig. 2 and are not shown for clarity. In both (a) and (b), the symbols are measured ΔR_{EXT} while the lines are calculated values of ΔR_B.

Width-normalized ballistic contact resistance R_B is [5]

$$R_B = \frac{\pi^{3/2}\hbar^2}{q^2}\sqrt{\frac{2}{kT}}\frac{1}{\sum_i \sqrt{m_{yi}}\,\Im_{-1/2}(x_i)}, \qquad (1)$$

where $\hbar$ is the reduced Planck's constant, k is the Boltzmann constant, q is the charge of an electron, m_{yi} and E_i are the effective mass in the direction perpendicular to the conductivity direction and subband energy of the i^{th}-subband, $\Im_{-1/2}(x)$ is the Fermi integral of order –1/2, $x_i = (E_F - E_i)/kT$, and E_F is the Fermi level. The value of E_F is determined by

$$N_S = (kT/\pi\hbar^2)\sum_i m_{Di}\ln(1+e^{x_i}), \qquad (2)$$

where m_{Di} is the density-of-states effective mass of the i^{th}-subband. In (1) and (2), m_{yi} and m_{Di} include valley degeneracy [6]. In order to calculate R_B using (1), we calculate E_F and E_i numerically from a one-dimensional (1D) self-consistent solution of Schrodinger and Poisson equations. The use of 1D calculations along the vertical direction is justified at low V_D when lateral fields are low.

The main features of R_B are as follows: Under the assumption of single-subband occupancy, $R_B \sim \sqrt{T}/N_S$ in the non-degenerate regime and $\sim 1/\sqrt{N_S}$ in the degenerate regime. These N_S and T dependences of R_B in the non-degenerate and degenerate regimes capture the key features of the experimental data shown in Fig. 3: as the 2D electron gas transitions from the non-degenerate regime (low N_S and high T) to the degenerate regime (high N_S and low T), R_B and therefore, R_{EXT} becomes less dependent on both N_S and T. Figure 3 also shows a comparison of measured ΔR_{EXT} and numerically-calculated $\Delta R_B = R_B - R_B$ ($N_S = 1.5 \times 10^{13}$ cm^{-2}). We find that the ballistic model fits the data fairly well over a wide range of N_S and T. One should note that there are *no fit parameters* in our model calculations. Based on this quantitative match, we conclude that the V_G and N_S dependences of R_{EXT} are primarily due to those of ballistic contact resistance R_B in our ETSOI devices.

To the best of our knowledge, this is the first report on the possible observation of ballistic contact resistance R_B in wide-channel Si MOSFETs at room temperature. Since the MOSFETs used in this work are wide, we arrived at our conclusion through the N_S and T dependences of R_B rather than the value of R_B because wide FETs have a large number of transverse modes M. We do note that R_B = 6.5 kΩ has been observed in the past in carbon nanotube MOSFETs at room temperature with the nanotube diameter in the 1-1.5 nm range [7].

CONCLUSIONS

In conclusion, using a comparison of our experimental data of R_{EXT} versus N_S and T to the ballistic FET theory, we have presented experimental evidence on the possible observation of ballistic contact resistance R_B in wide-channel Si MOSFETs. Finally, we note that the ballistic contact resistance R_B represents the ultimate limit of total series resistance R_{EXT} [8]. This limit for (100) Si is ~ 40 Ω.μm for NFETs and ~ 70 Ω.μm for PFETs at $N_S = 1 \times 10^{13}$ cm^{-2}. Furthermore, this limit of R_{EXT} is ~ 55 Ω.μm for III-V NFETs at $N_S = 1 \times 10^{13}$ cm^{-2} with isotropic effective mass m^*/m_0 in the 0.02-0.1 range. The value of R_B is slightly higher for III-V NFETs than that for Si NFETs because lower m^* and lower valley degeneracy lead to lower number of conducting transverse modes.

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We thank W. Haensch, S. Koswatta, I. Lauer, J. W. Sleight, and P. M. Solomon for stimulating discussions. A.M. thanks J. W. Sleight and G. Shahidi for encouragement and management support.

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Regrown Ohmic Contacts to $In_xGa_{1-x}As$ Approaching the Quantum Conductivity Limit

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We report contact resistances between source-drain regrowth and underlying semiconductor quantum well channels in test structures designed for characterization of source and drain access resistances in III-V MOSFETs. Regrowths included both N+ InAs and N+ graded InAs-$In_xGa_{1-x}As$; channel materials included both unstrained $In_{0.53}Ga_{0.47}As$ and unstrained InAs. The access resistivity correlates strongly with the sheet carrier concentration of the 2-dimensional electron gas, consistent with quantum- but not classical- transport theory. With source-drain regrowth of InAs contacts to InAs channels, the total access resistance is within a factor of two of the inverse of Landauer's quantum-state-limited conductance [1-3]. The state-limited conductance in TLM structures and the ballistic MOSFET transconductance both arise from the same physical process, hence the Landauer term in the TLM resistance does not contribute to the MOSFET source access resistance. Application of TLM data to transistor characterization must therefore correct for the state-limited access resistivity. Samples with contacts regrown onto channels with high $5\cdot10^{14}/cm^2$ sheet carrier concentration, hence low quantum-state-limited resistance, showed extremely low 12.7 Ω–μm access resistivity. This demonstrates the utility of MBE regrowth for source/drain formation in III-V MOS technology.

Epitaxial layer structures (Fig. 1) were prepared by solid source MBE. The channel material for samples (a, b,c,d) were 25 nm of $In_{0.53}Ga_{0.47}As$, 100 nm of n^+ $In_{0.53}Ga_{0.47}As$, 100 nm of n^+ $In_{0.53}Ga_{0.47}As$, and 15 nm InAs. ICP dry etching of SiO_2 formed dummy gates. Samples were oxidized by UV ozone, were dipped in 10:1 H_2O:HC, and were hydrogen cleaned (420 °C , 40 minutes). 60 nm of 5-10×10^{19} cm^{-3} Si-doped regrowth was deposited in the areas not covered by SiO_2. The regrowth was heteroepitaxial n^+ InAs on samples (a) and (b), homoepitaxial n^+ InAs on sample (c), and a non-linear grade from n^+ $In_{0.53}Ga_{0.47}As$ to n^+ InAs on sample (d). After regrowth, a planarization etch process removed regrowth debris from the dummy gate. Samples were metalized with 20 nm Ti / 60 nm Pd / 120 nm Au and mesa-isolated. Contact resistances between the semiconductor regrowth and the channel and contact resistance between the metal and regrowth were extracted by the TLM technique using the four-point technique.

For sample (a) (Table 1), the access resistance was 120 Ω–μm, the channel sheet resistivity 540 Ω, the regrowth sheet resistivity 24 Ω, and the metal/regrowth contact resistivity 2.1 Ω–μm (0.2 Ω–$μm^2$). For sample (b), the access resistance was 56 Ω–μm, the channel sheet resistivity 32 Ω, the regrowth and channel sheet resistivity 9.2 Ω, and the metal contact resistivity 3.8 Ω–μm (1.5 Ω–$μm^2$). For sample (c), the access resistance was 68 Ω–μm, the channel sheet resistivity 269 Ω, the regrowth sheet resistivity 19 Ω, and the metal contact resistivity 2.9 Ω–μm (0.4 Ω–$μm^2$). For sample (d), the access resistance was 12.7 Ω–μm, the channel sheet resistivity 14.5 Ω, the regrowth and channel sheet resistivity 11.3 Ω, and the metal contact resistivity 3.0 Ω–μm (0.8 Ω–$μm^2$).

Abrupt heterojunctions between the regrowth and channel increase the contact resistivity. This is seen comparing sample (a), InAs regrowth / $In_{0.53}Ga_{0.47}As$ channel, to sample (c), InAs regrowth / InAs channel. It is also seen comparing sample (b), InAs regrowth / $In_{0.53}Ga_{0.47}As$ channel, to sample (d) $In_{0.53}Ga_{0.47}As$-InAs graded regrowth / $In_{0.53}Ga_{0.47}As$ channel. Lower metal-regrowth contact resistivity is observed with more heavily-doped channels. This is seen comparing InAs regrowth on (sample a) thin 25 nm (n_s =$9\cdot10^{12}/cm^2$) versus (sample b) thick 100 nm (n_s =$9\cdot10^{14}/cm^2$) n^+ $In_{0.53}Ga_{0.47}As$ channels. It is also seen comparing (sample b) n^+ InAs regrowth on a thick $In_{0.53}Ga_{0.47}As$ channel with (sample c) n^+ InAs regrowth on a thin InAs channel; despite the InAs/ $In_{0.53}Ga_{0.47}As$ heterointerface in sample (b), lower contact resistivity is observed for the thicker channel.

A TLM structure can show at most Landauer's state-limited conductance; for highly degenerate concentrations, $G_{state} = (q^2 2^{1/2}/\hbar\pi^{3/2})\Sigma_i g_i^{1/2} n_{s,i}^{1/2}$, where g_i is the band degeneracy and $n_{s,i}$ the sheet carrier concentration in the i^{th} vertical eigenstate. The extracted zero-contact-spacing intercept of a TLM measurement is the sum of metal-regrowth and regrowth-channel resistances to the channel and this state-limited resistance $R_{state} = 1/G_{state}$. Noting the factor of two associated with the two contacts, the measured 136 Ω-μm resistance (sample c) between two regrown n^+ InAs contacts on the 15 nm InAs channel is within a factor of two of the channel's 80 Ω-μm 2-D state limited resistance. The low 12.4 Ω-μm (11.12 Ω-$μm^2$) contact-channel access resistivity observed with graded regrowth of contacts to a thick, high n_s channel (sample d) suggests that extremely low contact resistances can be achieved via MBE regrowth. Given that the Landauer resistance observed in a TLM structure will not contribute to MOSFET source access resistance, application of TLM data to transistor characterization in any material system must therefore recognize and correct for the state-limited access resistivity term.

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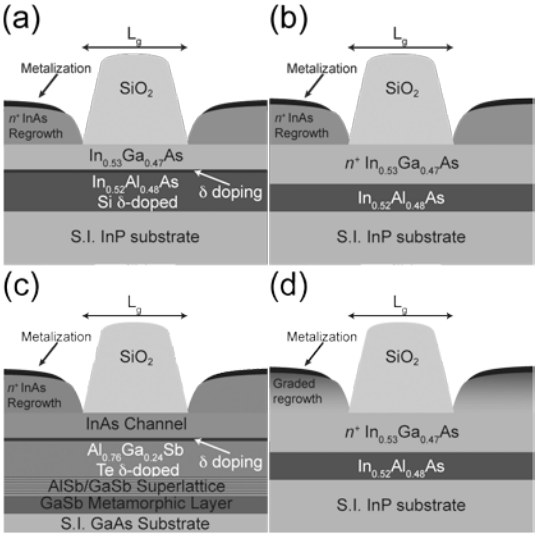

Figure 1: Channel-regrowth contact resistance test structures for (a) the 25 nm $In_{0.53}Ga_{0.47}As$ channel with n^+ InAs regrowth, (b) the 100 nm n^+ $In_{0.53}Ga_{0.47}As$ with n^+ InAs regrowth, (c) 15 nm InAs channel with n^+ InAs regrowth, and (d) 100 nm n^+ $In_{0.53}Ga_{0.47}As$ channel with graded regrowth.

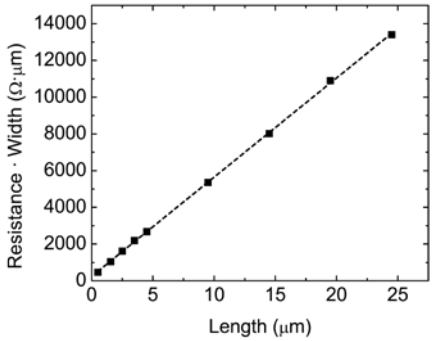

Figure. 2: TLM resistance for sample (a), 25 nm $In_{0.53}Ga_{0.47}As$ channel with n^+ InAs regrowth.

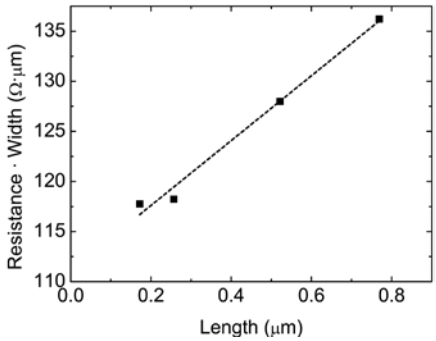

Figure. 3: TLM resistance for sample (b), 100 nm n^+ $In_{0.53}Ga_{0.47}As$ with n^+ InAs regrowth.

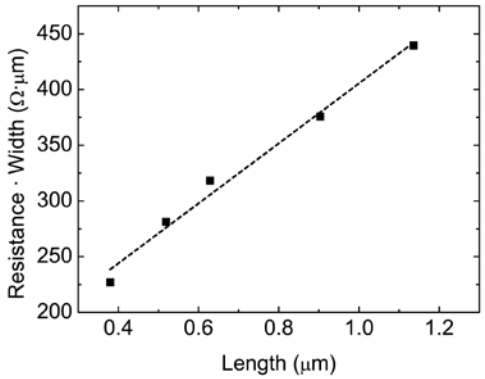

Figure 4: TLM resistance for sample (c), 15 nm InAs channel with n^+ InAs regrowth.

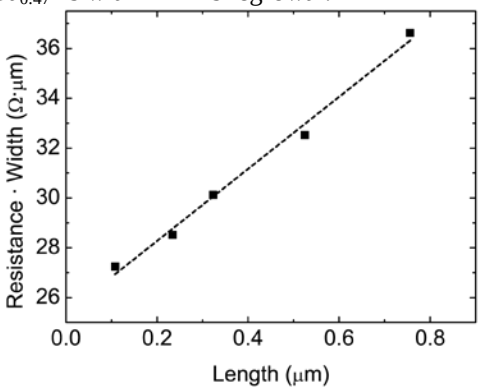

Figure 5: TLM resistance for sample (d), 100 nm n^+ $In_{0.53}Ga_{0.47}As$ channel with graded regrowth.

Table 1: Sample layer structures and measured resistivities.

Sample	(a)	(b)	(c)	(d)
N+ regrowth				
composition	InAs	InAs	InAs	$In_{0.53}Ga_{0.47}As \rightarrow$ InAs
thickness	60 nm	60 nm	60 nm	60 nm
doping	$5\text{-}10\cdot10^{19}/cm^3$	$5\text{-}10\cdot10^{19}/cm^3$	$5\text{-}10\cdot10^{19}/cm^3$	$5\text{-}10\cdot10^{19}/cm^3$
sheet resistivity	23.8 Ω	7.4 Ω	19.3 Ω	11.3 Ω
channel				
composition	$In_{0.53}Ga_{0.47}As$	$In_{0.53}Ga_{0.47}As$	InAs	$In_{0.53}Ga_{0.47}As$
thickness	25 nm	100 nm	15 nm	100 nm
doping	$9\cdot10^{12}/cm^2$	$5\cdot10^{19}/cm^3$	$9\cdot10^{12}/cm^2$	$5\cdot10^{19}/cm^3$
sheet resistivity	540 Ω	32 Ω	269 Ω	15 Ω
access resistivity per contact	120.8 Ω–μm	55.6 Ω–μm	68.2 Ω–μm	12.7 Ω–μm
metal/regrowth contact resistivity	2.1 Ω–μm 0.2 Ω–μm^2	4.6 Ω–μm 1.5 Ω–μm^2	3.0 Ω–μm 0.4 Ω–μm^2	3.0 Ω–μm 0.8 Ω–μm^2

Simulation Study of Nanowire Tunnel FETs

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Tunnel FETs (TFETs) are candidates for low-power logic switches with sub-thermal slope which could enable a strongly reduced supply voltage. To improve the ON-current compared to Si TFETs, III-V/Si hetero junctions have been proposed [1]. Using nanowires has additional advantages: (i) the possibility of many different material combinations [2], (ii) efficient strain relaxation in the case of small diameters [2], (iii) a good electrostatic control due to the surrounding gate. Tomioka et al. [3,4,5] and Björk et al. [6] have advanced the integration of InAs nanowires on Si with nanometer-scale hetero epitaxy. The present simulation study refers to their experimental data.

The combined application of a quantum transport solver and a TCAD tool can help to understand the behavior of InAs/Si hetero nanowire Esaki diodes and TFETs and can give guidelines to improve their performance by optimization of geometry, doping, gating, and biasing. We used the quantum transport simulator OMEN [7] which is massively parallel, multi-dimensional, atomistic, and based on a $sp^3d^5s^*$ tight-binding representation of the band structure. Quantum transport simulation can be done either in the Non-equilibrium Greens Function (NEGF) formalism (scattering) or in the Wave Function formalism (ballistic). OMEN has been applied to direct and phonon-assisted band-to-band tunneling (BTBT) in InAs, Si, and Ge nanowire homo TFETs [8]. The commercial device simulator Sentaurus-Device [9] is equipped with various local and non-local BTBT models. Neither a theory nor an analytical model for BTBT in a hetero junction between a direct and an indirect semiconductor exists. A practical workaround has to be used with S-Device, since a tunnel path across the hetero interface must either belong to a direct (zero-phonon) or to a phonon-assisted tunnel process. Therefore, (i) the "*dynamic nonlocal path BTBT model*" (short cut: "*Kane model*" [10]), calibrated for InAs, is also used on the silicon side, fitted to experimental data of [11], and (ii) the calibrated model for Si [12] (short cut "*Schenk model*") is also used on the InAs side after proper modifications [13].

The BTBT current of short, unconfined Esaki homo diodes ($\langle 111 \rangle$, 20 nm length, abrupt doping) was simulated with OMEN for different materials and doping levels. For the direct materials (InAs, GaSb) and for Ge, where coherent BTBT is dominant [8], the simulation of bulk diodes is straightforward. Bulk simulations are needed because there is also no geometrical confinement in the fabricated nanowire TFETs (diameters in the range 25 nm – 100 nm). Fig. 1 shows that InAs has the highest BTBT current density, followed by GaSb and Ge. The upper limit for InAs is $\sim 5 \times 10^4$ kA/cm^2. In the case of Si, due to the demanding electron-phonon coupling, at least one-dimensional confinement is necessary (the direction of confinement is $\langle \bar{1}10 \rangle$, periodic continuation was applied in $\langle 11\bar{2} \rangle$ direction). The bulk limit of Si remains below 100 kA/cm^2, a factor 500 smaller than that of InAs. Fig. 2 presents the comparison between OMEN and S-Device simulations of InAs Esaki diodes using the calibrated TCAD models. Based on the good agreement, the doping levels at the InAs side of InAs/Si nanowire hetero Esaki diodes produced at IBM Research-Zurich [13,14] were determined by reverse modeling (Fig. 3). Measured [5] and simulated InAs/Si nanowire TFET I_DV_{GS} characteristics are compared in Fig. 5. The striking features of the measured IV curves are: an almost constant slope over 2-3 orders of magnitude, very weak ambipolarity, and a strong saturation of the ON-current for each source-drain voltage. In contrast, simulation yields much higher ON-currents, a strong ambipolarity, curved slopes typical for BTBT, a minimum point slope of 45 mV/dec, and no ON-current saturation. The most likely explanation of the measured currents is that they are dominated by defect-assisted tunneling (DAT), either during interface or bulk SRH generation (Fig. 7). Although multi-phonon coupling parameters of the involved defects in InAs are not known, the shape of the I_DV_{GS} curves can be qualitatively reproduced with a physics-based DAT model [15] in S-Device (Fig. 8). We attribute the absence of BTBT in the measurement to compressive biaxial strain in the highly lattice mismatched system (Fig. 9).

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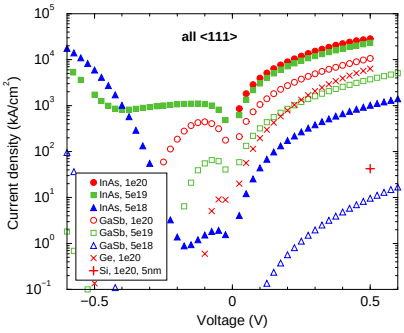

Fig. 1: Short Esaki (bulk) diodes with symmetrical doping simulated with OMEN. The single data point for Si was obtained for a 5 nm slab and took 5 h on Jaguar Cray XK6 using $\sim$ 20'000 CPUs.

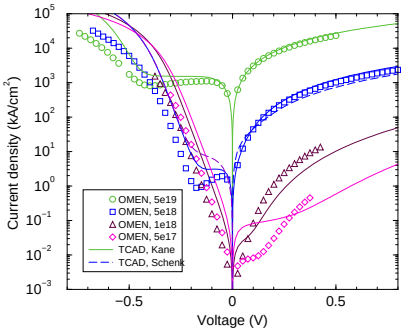

Fig. 2: Comparison between OMEN and S-Device simulations of short InAs Esaki (bulk) diodes with symmetrical doping as indicated. Good agreement is found in the high-doping (high-field) range.

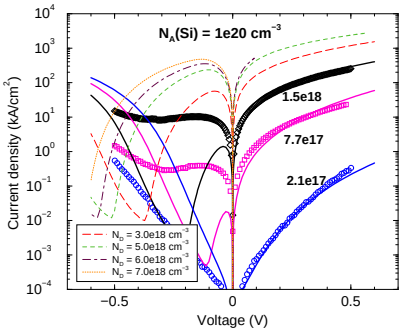

Fig. 3: Comparison between measured and TCAD-simulated InAs/Si nanowire hetero Esaki diodes. The ON-current is limited to $\sim \ 1 \times 10^4$ kA/cm^2, in good agreement with the homo diodes of Fig. 1.

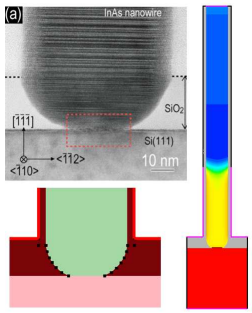

Fig. 4: TEM image of the InAs/Si nanowire TFET from Tomioka et al. [5] (upper left), simulation close-up (lower left), entire simulation domain with carrier concentrations (right).

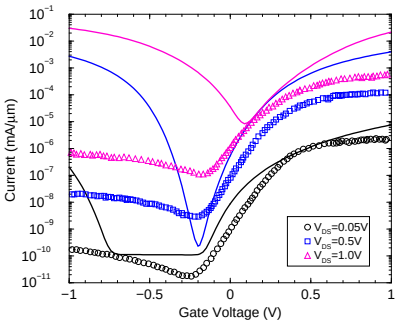

Fig. 5: Measured [5] and simulated InAs/Si nanowire TFET $I_D V_{GS}$ characteristics. Doping according to [5]. Work function = 4.65 eV, EOT = 4.5 nm.

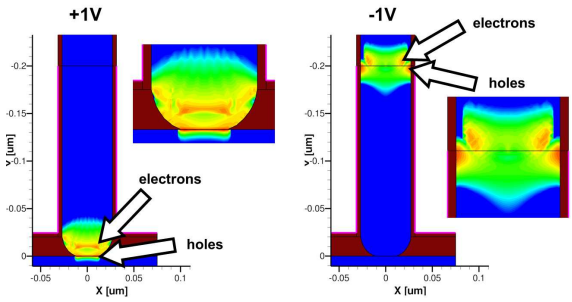

Fig. 6: BTBT rate distribution at V_{GS} =1 V (left) and V_{GS} =-1 V (right). The strong ambipolar current is caused by off-junction tunneling under the gate edge which is aligned with the high-low doping transition. It can be suppressed by a corresponding gate "underlap". The simulated ON-current at V_{GS} =1 V originates from in-junction BTBT with delta-like hole generation at the interface.

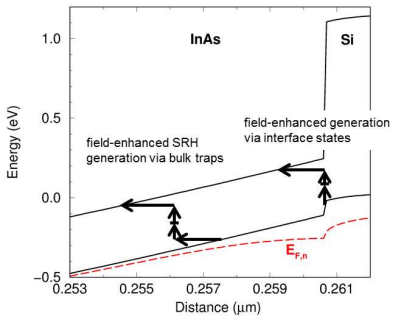

Fig. 7: Band edge profile (solid) and electron quasi Fermi level (dashed) in the vicinity of the hetero junction. Schematic of defect-assisted tunneling during SRH generation.

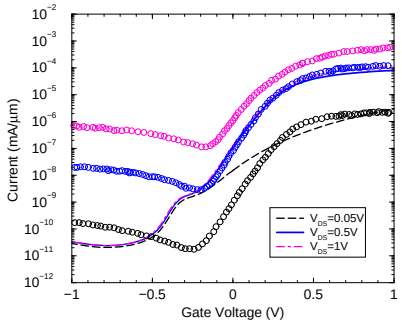

Fig. 8: Simulation with bulk DAT in restricted region (BTBT turned off). DAT parameters: zero-field lifetimes $\tau_n = \tau_p = 3 \times 10^{-8}$ s, lattice relaxation energy $S\hbar\omega_0 = 10.5$ meV, tunnel masses $m_n = 0.023\, m_0$, $m_h = 0.2\, m_0$.

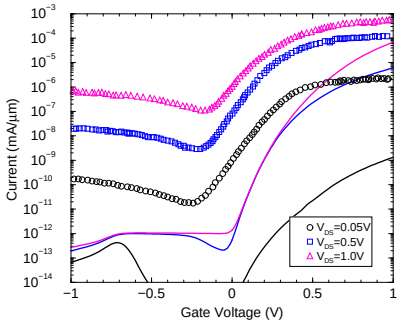

Fig. 9: Measured $I_D V_{GS}$ characteristics [5] and simulated BTBT current assuming homogeneous 8% compressive in-plane strain. Gap extracted from Van de Walle model [16], effective masses from OMEN [7].

Flicker Noise Characterization and Analytical Modeling of Homo and Hetero-Junction III-V Tunnel FETs

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Introduction: $GaAs_ySb_{1-y}/In_{0x}Ga_{1-x}As$ based III-V staggered hetero-junction (heterojn) Tunnel Field Effect Transistors (TFETs) have been demonstrated with MOSFET-like high drive currents (Ion) at low Vds [1], demonstrating feasibility for low supply voltage logic applications. More than 2x enhancement in Ion was demonstrated over the $In_{0.7}Ga_{0.3}As$ homo-junction (homoJn) counterpart due to reduction in the effective tunneling barrier (Eb_{eff}) at the hetero-interface. In this work, we characterize the flicker noise performance of $In_{0.7}Ga_{0.3}As$ homoJn and $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heteroJn TFETs to quantify the impact of heterointerface on flicker noise - an important figure-of-merit for low power analog applications. We show that heteroJn TFETs exhibit lower flicker noise than the homoJn TFET at a given Ion. Finally, we propose and develop a carrier number fluctuation (CNF) based analytical model to quantitatively model the flicker noise characteristics of homoJn and heteroJn TFETs.

Device Characterization and Modeling: Fig. 1 shows the schematic of the fabricated TFETs. The $In_{0.7}Ga_{0.3}As$ homoJn TFET with Eb_{eff} of 0.58eV and $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heteroJn TFET with Eb_{eff} of 0.25eV were fabricated (Fig. 2) using the process flow described in [2]. Temperature dependent transfer characteristics measured from T=77K to T=300K at Vds=500mV confirm that both band to band tunneling (BTBT) and trap assisted tunneling and thermionic-emission (TAT) processes [3] affect the transport in homoJn and heteroJn TFETs at room temperature, whereas at 77K, only BTBT determines the transfer characteristics (Figs. 3,4).A dynamic non-local band to band tunneling (BTBT) model [4] was used to model the measured transfer characteristics at T=77K. Table I lists the parameters used to model the measured transfer characteristics. Flicker noise measurements were done on TFETs with pillar width=10um, channel length=150nm and pillar thickness=150nm at T=77K, 300K and at a constant Vds of 500mV. At T=300K, where both BTBT and TAT affect the transfer characteristics, homoJn and heteroJn TFETs exhibit comparable drain current normalized noise levels (Fig. 7). At T=77K, where only band-to-band tunneling (BTBT) dominates, heteroJn TFET exhibits much lower flicker noise than homoJn TFET for a given drain current (Fig. 8). Since the current generation at T=77K is limited by BTBT at the tunnel junction, a carrier number fluctuation model is employed to explain the measured characteristics. Since BTBT in TFETs is independent of the channel length (unlike MOSFETs) we define an effective tunneling length L' [5] based on the spread of the band-to-band generated carriers in the channel which is much smaller than the channel length. Fig. 9(a) shows the band to band generation rate of electrons extracted from the dynamic non-local 2D numerical simulation of the TFETs. For a given drain current, L' is smaller in homojunction and larger for heteroJn TFET due to lower electric field (Fig. 9(b)-(c)) arising from lower Eb_{eff}. Electrons in the effective tunneling region with energy around the electron quasi-fermi level (E_{Fn}) experience trapping and detrapping from the traps in the oxide (Fig. 10). Fluctuations in the trapped charge lead to fluctuation in the junction electric field which, in turn, affects the band-to-band generation rate. The frequency spectrum of the drain current fluctuation varies as 1/f due to the superposition of the individual trapping events. Each trapping event implies electrons tunneling in the time domain into empty states that extend into the gate dielectric, The trapping time constant distribution is exponential decaying away from the gate dielectric/tunnel junction interface.(Fig. 10). Table II lists the set of equations used to model the TFET flicker noise characteristics. The normalized drain current noise is found to depend on the electric field, F, the effective tunneling length, L' and B parameter (Table II). For heteroJn, at a given drain current, though the electric field is smaller, the smaller value of B parameter and the larger L' results in lower flicker noise level. Assuming a trap density, N_{it}, of $1x10^{13}$ cm^{-2} the measured characteristics are in excellent agreement with the analytical model (Fig. 11).

Conclusions: Temperature dependent transfer characteristics measurements confirm that the current in heteroJn TFET is limited by band-to-band tunneling at Vds=500mV at low temperature. HeteroJn TFETs exhibit lower noise compared to homoJn TFET where the current transport is dominated by band-to-band tunneling alone. However, at 300K, heteroJn TFETs have comparable noise performance due to the strong presence of trap assisted tunneling ($Nit\sim10^{13}$ cm^{-2}). A carrier number fluctuation based model is developed, for the first time, to explain the flicker noise advantage of heteroJn TFETs over homoJn TFETs. HeteroJn TFETs not only provide higher drive currents but also exhibit lower flicker noise levels and hence make them suitable candidate for future low Vcc digital and analog applications.

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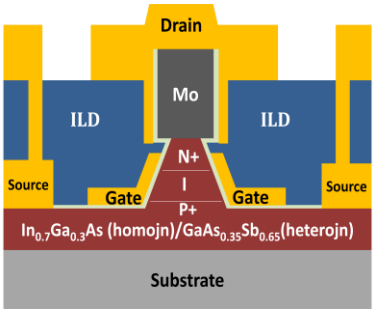

Fig 1.Schematic of the the fabricated vertical tunnel FETs [2].

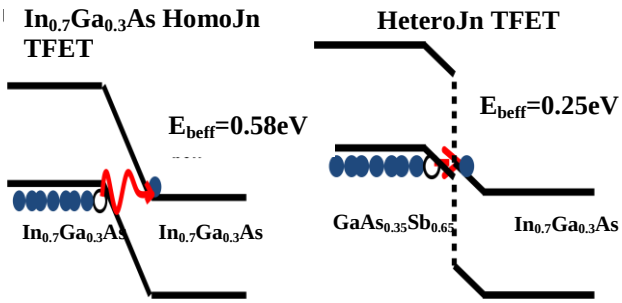

Fig 2. Eb_{eff} reduces from 0.58eV to 0.25eV as the source material is changed from $In_{0.7}Ga_{0.3}As$ to $GaAs_{0.35}Sb_{0.65}$.

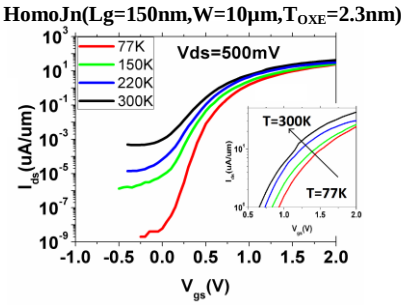

Fig 3.Temperature dependent transfer characteristics of homojunction TFET.

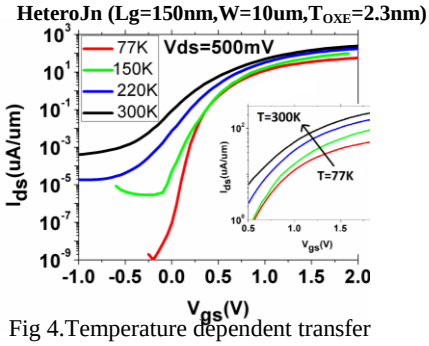

Fig 4.Temperature dependent transfer characteristics of heterojunction TFET.

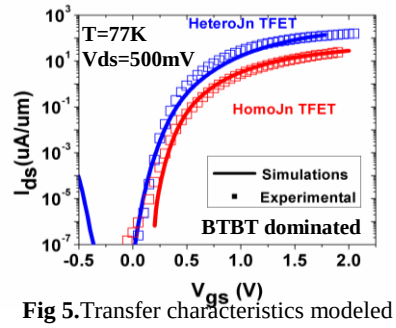

Fig 5. Transfer characteristics modeled with simulations at 77K.

Dynamic non-local band-to-band generation model [4]

Parameter	HomoJn TFET	HeteroJn TFET
T_{OXE}(nm)	2.3	2.3
Source Doping(cm^{-3})	$5x10^{19}$	$5x10^{19}$
m_r	$0.019m_0$	$0.022m_0$
E_{beff} (eV)	0.64	0.31

Table I. Simulation parameters used to model the measured transfer characteristics at 77K.

TFET FLICKER-NOISE MEASUREMENTS

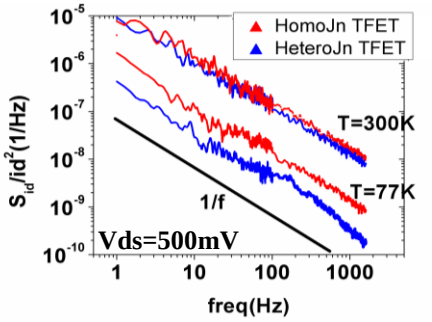

Fig 6. Normalized drain current noise spectrum at Ids= 2uA/um follows 1/f trend.

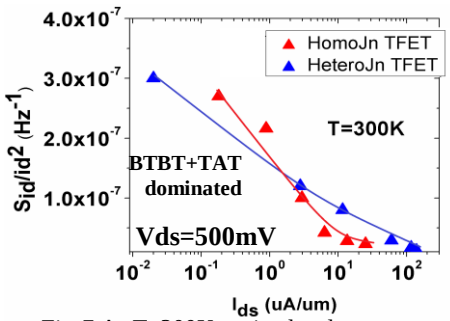

Fig 7.At T=300K, noise levels are comparable between homojn and heterojn.

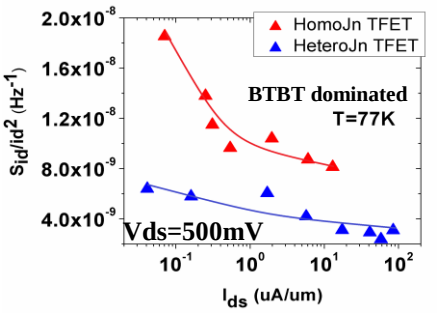

Fig 8. At T=77K, heterojn TFET exhibits lower noise at a given drain current.

TFET FLICKER NOISE - ANALYTICAL MODELING

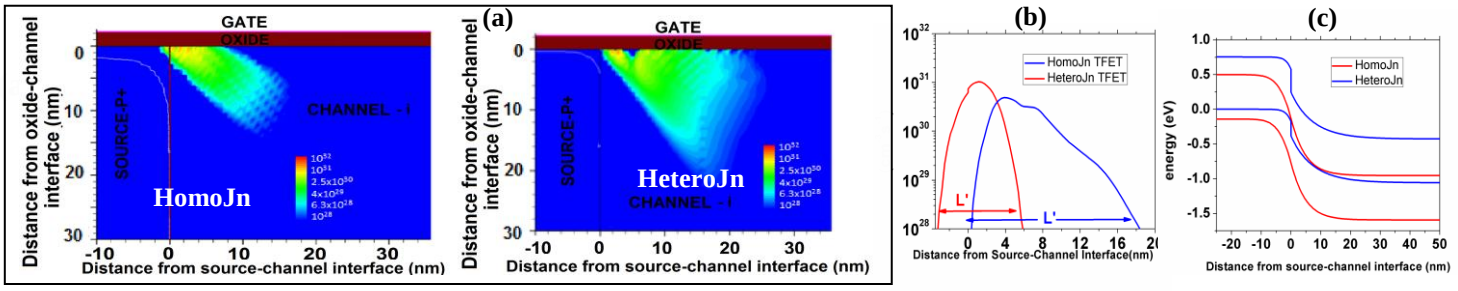

Fig 9.(a) Contour plot of electron band to band generation from 2D simulations (b) Effective tunneling length L' is defined based on the spread of band-to-band generated electrons (c) Corresponding band diagram shows that L' is higher in heteroJn due to smaller electric field at a given drain current level.

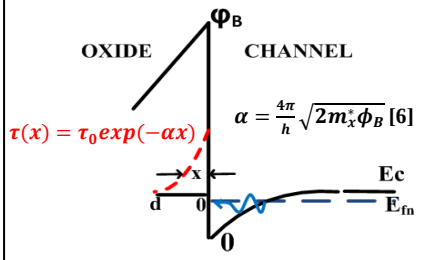

Fig 10. Trapping/de-trapping of electrons around E_{fn} into the trap states in the oxide with exponentially decaying time constant τ(x) results in flicker noise.

$$I_{ds} = AF^2 exp\left(\frac{-B}{F}\right); A = \frac{\pi m_r^{0.5} q^2}{9h^2[Eb_{eff}^{0.5}]}; B = \frac{\pi^2 m_r^{0.5} Eb_{eff}^{1.5}}{qh} \quad [4]$$

$$\Delta F = \frac{\Delta Q}{\varepsilon_{ox}}$$

$$S_{\Delta Q} = q^2 S_{\Delta Nt} = q^2 \frac{\tau_t}{1 + w^2 \tau_t^2} N_t f_t (1 - f_t)$$

$$\frac{S_{Ids}}{Ids^2} = \left(\frac{2}{F} + B\frac{B}{F^2}\right)^2 \frac{q^2 N_t(Efn)}{\varepsilon_{ox}^2 WL' \alpha f}$$

Table II. Proposed analytical equations describing flicker noise characteristics in TFET assuming pure BTBT dominated transport.

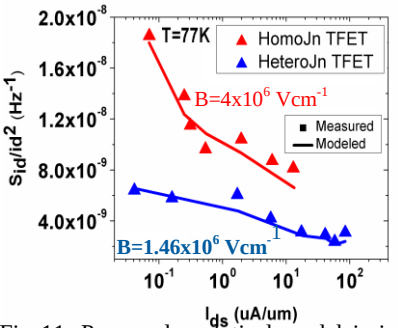

Fig 11. Proposed analytical model is in excellent agreement with the experimental data.

High Current Density InAsSb/GaSb Tunnel Field Effect Transistors

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Introduction. Steep-slope devices, such as tunnel field-effect transistors (TFETs), have recently gained interest due to their potential for low power operation at room temperature. The devices are based on inter-band tunneling which could limit the on-current since the charge carriers must tunnel through a barrier to traverse the device. The InAs/GaSb heterostructure forms a broken type II band alignment which enables inter-band tunneling without a barrier, allowing high on-currents. We have recently demonstrated high current density ($I_{ON,\ reverse}$ = 17.5 mA/μm^2) nanowire Esaki diodes[1] and in this work we investigate the potential of InAs/GaSb heterostructure nanowires to operate as TFETs. We present device characterization of $InAs_{0.85}Sb_{0.15}$/GaSb nanowire TFETs, which exhibit record-high on-current levels.

Device fabrication. The nanowires were grown from Au aerosols on a GaAs substrate using metal organic vapor phase epitaxy[2]. For the nucleation of the GaSb segment, a short stem of GaAs was first grown. Zn doping was introduced to reduce the series resistance in the GaSb segment, which was followed by growth of an unintentionally doped InAsSb top segment as well as a thin shell of InAsSb covering the GaSb segment. This shell facilitates the contact formation to GaSb and also allows for single-step source and drain contact process. At the final stage of the growth, the nanowires were annealed to form a neck region at the InAsSb/GaSb heterointerface, which reduces the conducting area and suppresses potential shell leakage currents[3]. The nanowires were transferred onto a prepatterned Si chip where source, drain and gate electrodes were defined by electron beam lithography and thermal evaporation of Ni/Au. An Al_2O_3/HfO_2, 3/70 cycles (0.3/8 nm), bilayer deposited at 100 ^oC with atomic layer deposition was used as a gate dielectric.

Electrical characterization. A record high on-current of 110 μA/μm (I_{DS} = 19 μA, circumference = 0.17 μm) was measured for $V_{DS} = V_{GS}-V_T$ = 0.5 V, with R_{ON} = 20 kΩ = 3.5 Ω·mm. Furthermore, the devices show a distinct negative differential resistance characteristic with a peak to valley ratio of 3. The maximum peak current density, with V_{DS} applied on the GaSb side, was measured to 1.2 mA/μm^2, with a peak position that moves to slightly higher V_{DS} with increasing positive V_{GS}. A fixed peak position with varying peak current suggests that the gate is indeed affecting the bands at the heterojunction and that the device is not a tunnel junction in series with a field effect transistor. The limited off-characteristics found for these devices are here likely affected by inter-band tunneling in the gate-drain region and/or hole accumulation under the gate. A conservative evaluation of the subthreshold swing (SS), at the slope on the gentle side of the hysteresis loop, representing an upper bound value, would be 300 mV/decade at V_{DS} = 0.3 V. Furthermore, the devices also show an I_{ON}/I_{OFF} ratio of 275 at V_{DS} = 0.3 V. Extraction of the SS is made difficult because of hysteresis in the transfer characteristics, possibly caused by trapped charges in the gate dielectric.

1. High Current Density Esaki Tunnel Diodes Based on GaSb-InAsSb Heterostructure Nanowires. B. Ganjipour, A.W. Dey, B. M. Borg, M. Ek, M.-E. Pistol, K. A. Dick, L.-E. Wernersson, and C. Thelander. *Nano Letters* 2011 *11* (10), 4222-4226
2. Formation of the Axial Heterojunction in GaSb/InAs(Sb) Nanowires with High Crystal Quality. M. Ek, B. M. Borg, A. W. Dey, B.Ganjipour, C.Thelander, L.-E.Wernersson, and K. A. Dick. *Crystal Growth & Design* 2011 *11* (10), 4588-4593
3. Diameter reduction of nanowire tunnel heterojunctions using in situ annealing. B. M. Borg, M. Ek, K. A. Dick, B. Ganjipour, A. W. Dey, C. Thelander, and L.-E. Wernersson, *Appl. Phys. Lett.* 99, 203101, 2011

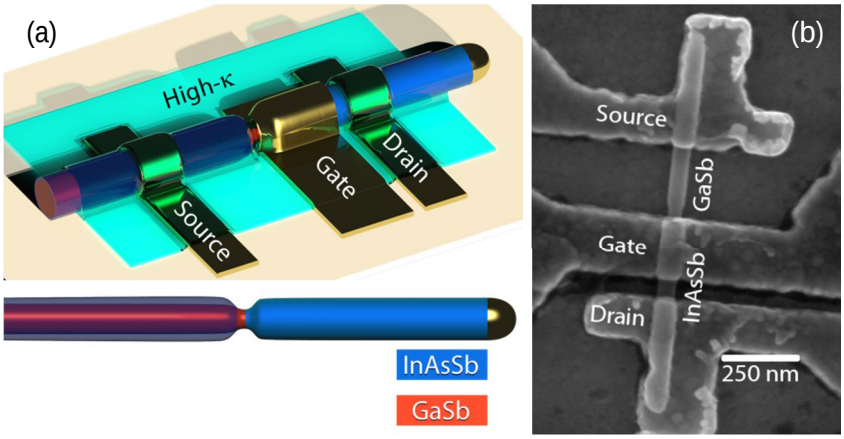

Fig. 1. (a) Schematic layout of an InAsSb/GaSb TFET. (b) SEM image of an InAsSb/GaSb TFET device. Electrode configuration for reverse biased operation.

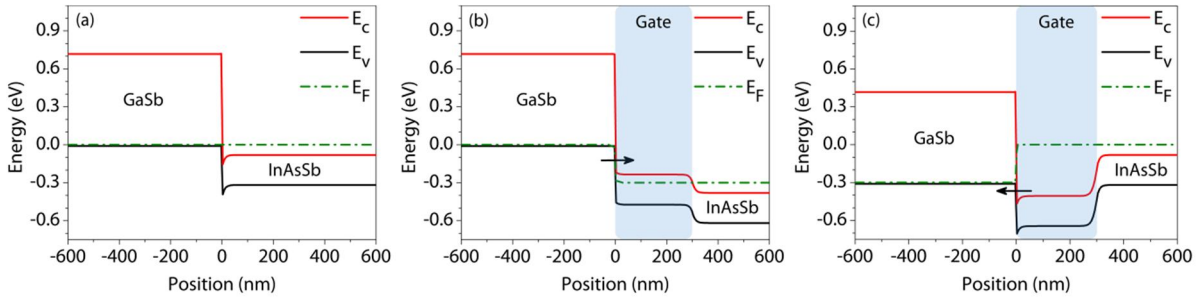

Fig. 2. Simulated band structure of an ideal InAsSb/GaSb heterointerface. (a) The band structure at equilibrium. (b) Reverse biased (positive drain bias on the InAsSb segment and GaSb grounded) with a positive gate voltage applied. (c) Forward biased (positive drain bias on the GaSb segment and InAsSb grounded) with a positive gate voltage applied.

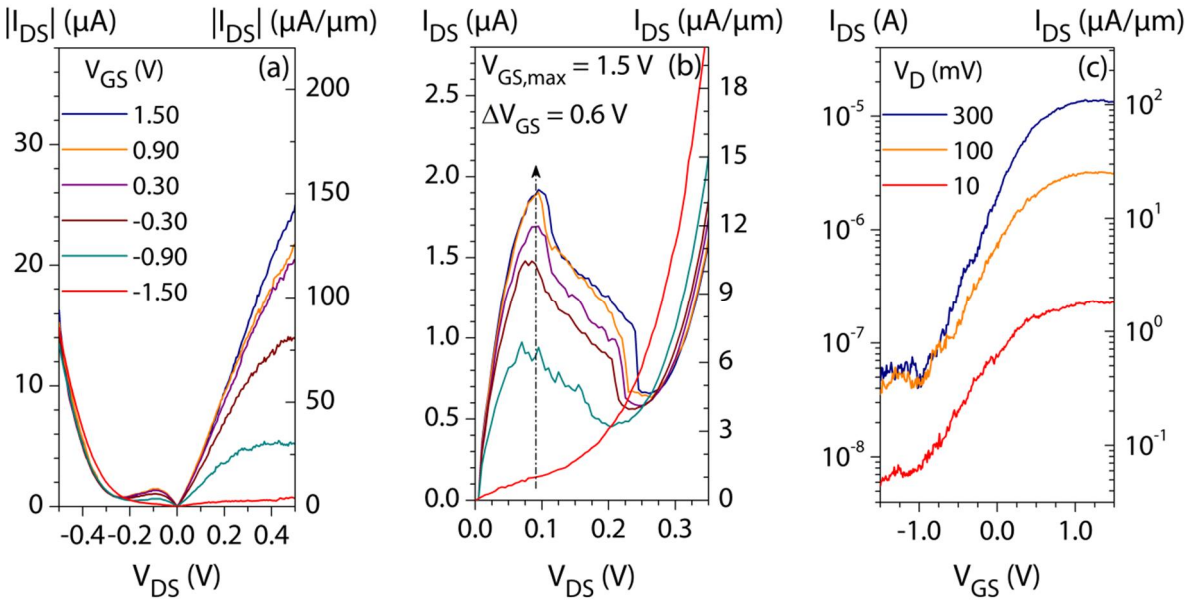

Fig. 3. Output and transfer characteristics of an InAsSb/GaSb TFET at room temperature. (a) Reverse biased with GaSb grounded. (b) Forward biased with InAsSb grounded. (c) Reverse biased with GaSb grounded.

Gate-first implant-free InGaAs n-MOSFETs with sub-nm EOT and CMOS-compatible process suitable for VLSI

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Compound semiconductors such as $In_xGa_{1-x}As$ ($x \geq 0.53$) are foreseen as potential candidates to replace silicon as a channel material for high performance logic application due to their better transport properties. Recently, planar or tri-gate III-V transistors with better performance metrics than main-stream silicon technology have been demonstrated**[1,2]**, confirming their potential to continue the traditional silicon scaling roadmap beyond the 14 nm node. These devices exhibit record on-performance**[1]** or record electrostatic integrity**[2]**, but their design does not take into account the very restrictive requirements of Very-Large Scale Integration (VLSI): self-aligned process, gate-first flow, sub-nm equivalent oxide thickness (EOT) gate stack and high thermal stability. In this contribution, we report on gate-first implant-free $In_{0.53}Ga_{0.47}As$ n-MOSFETs with sub-nm EOT and high thermal stability featuring a fully CMOS compatible process suitable for VLSI, and a good electrostatic integrity compared to state-of-the-art devices.

Transistor fabrication - The n-MOSFETs are fabricated on a 10 nm thick semi-insulating $In_{0.53}Ga_{0.47}As$ channel on InAlAs on InP according to the process flow summarized in Fig. 1. First, the gate stack is formed by depositing 1 nm of amorphous silicon, 1 nm of Al_2O_3 and 2 nm of HfO_2 as gate dielectric stack**[3]**, 30 nm of sputtered W as gate metal and 30 nm of SiN_x as gate capping layer. After gate-patterning by e-beam lithography and dry-etch, sidewall insulation is performed by depositing and dry-etching 50 nm of SiN_x, leaving the gate stack fully encapsulated. Subsequently, a careful channel surface cleaning is performed followed by selective area epitaxy of 50 nm thick *in-situ* doped raised S/D by MOVPE**[4,5]**. The transistors then follow a standard back-end process with a 100 nm thick 1st inter-layer dielectric (ILD1) and metal 1 (M1) contacts.

Long-channel devices - C_G-V_G characteristics, interface trap density (D_{it}) vs gate voltage and effective mobility vs channel charge density are measured on long-channel devices (L_G = 25 µm) and shown in Fig. 2 and 3. These gate-first devices, processed with a maximum thermal budget of 600°C for 15 minutes, exhibit a healthy C-V curve with no hysteresis, a low frequency dispersion in accumulation (besides gate leakage induced dispersion), an EOT of 0.9 nm and a peak D_{it} of 5×10^{12} $eV^{-1}cm^{-2}$. The excellent thermal stability of the gate stack allows us to demonstrate a sub-nm EOT InGaAs MOSFET for the first time. Furthermore, the extracted peak mobility of 1270 $cm^2/V.s$ which is higher than previously reported data**[3]** tends to indicate that there is no mobility degradation while scaling the EOT. We attribute this effect to the scaling of the HfO_2 thickness reducing the contribution of remote phonon scattering or fixed charges, thus improving the electron mobility.

Short-channel devices - I_D-V_G and I_G-V_G characteristics of a short-channel devices (L_G = 65 nm) are shown in Fig. 4. These devices exhibit a good IO_N/I_{OFF} ratio of 7×103 with an off-current limited by the gate leakage due to the scaled EOT. The low on-current (25 µA/µm at V_{DS} = 0.5 V) is mainly limited by the high access resistance due to the large gate-to-source/drain spacing L_{SIDE} of 35 nm. This spacing is one of the biggest challenge in implant-free VLSI type of devices, and has to be reduced in the 5 nm range in order to match the on-performance of reported non-VLSI devices**[1,2]**. Sub-threshold swing (SS) and drain-induced barrier lowering (DIBL) is plotted vs gate length in Fig 5 and 6. Thanks to the scaled EOT and the thin channel (10 nm), these devices demonstrate a good electrostatic integrity with a DIBL of 130 mV/V at L_G = 65 nm which is comparable to the best planar devices reported**[2]**. The long-channel SS of 88 mV/dec is in good agreement with the measured D_{it}. The short-channel SS of 174 mV/dec at V_{DS} = 0.5 V and L_G = 65 nm is similar to the one reported in **[1]** with a comparable D_{it}, or to planar devices from **[2]** with t_{ch} = 40 nm. At matched t_{ch} = 10 nm, devices from **[2]** show a much better short-channel effects control related to a 10-times lower measured D_{it}.

Conclusion - We have demonstrated the first InGaAs MOSFETs with sub-nm EOT featuring a gate-first implant-free process compatible with VLSI. At L_G = 65 nm, these devices are among the best reported ones in terms of electrostatic integrity but they suffer from a large access resistance related to a large gate-to-source/drain spacing. Future work will focus on scaling this spacing in the 5 nm range in order to achieve the desired on-performance.

Acknowledgments The authors acknowledge support from the European Union within the Marie Curie project FP7-PEOPLE-2009-IEF-255298 ASPECTS.

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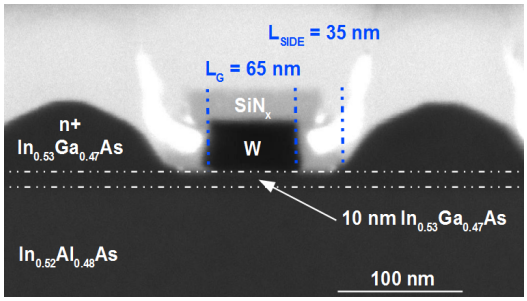

- III-V growth
- High-k / Metal gate / Gate cap deposition
- Gate patterning (L_G)
- Sidewall insulation (L_{SIDE})
- III-V cleaning and S/D regrowth (600°C)
- ILD1 deposition and patterning
- M1 contacts

*Fig 1: Cross-sectional STEM micrograph and **CMOS-like process flow** of a gate-first implant-free fully-depleted $In_{0.53}Ga_{0.47}As$ MOSFET with a **65 nm gate length**, 10 nm thick channel and self-aligned n+ raised $In_{0.53}Ga_{0.47}As$ S/D. The large gate-to-source/drain spacing (L_{SIDE}) of 35 nm is responsible for the large access resistance of the device.*

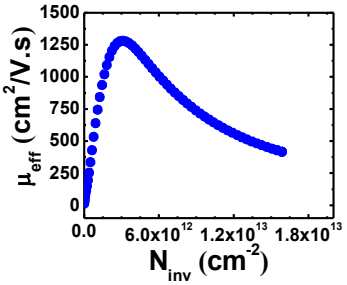

*Fig 2: Effective mobility (μ_{eff}) versus channel charge density (N_{inv}) extracted by the split-CV method, showing an excellent **peak mobility of 1270 $cm^2/V.s$** given the scaled EOT.*

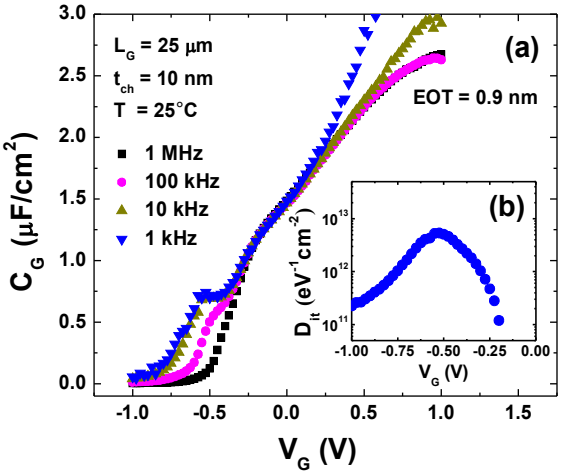

*Fig. 3: (a) C_G-V_G characteristics measured on a gate-first MOSFET as described in Fig. 1 with a **25 µm gate length**. (b) D_{it} versus gate voltage extracted by the high-low frequency method between 1kHz and 1MHz. The gate stack, composed of 1 nm Si / 1 nm Al_2O_3 / 2 nm HfO_2, has an **EOT of 0.9 nm** and a peak D_{it} of 5×10^{12} $eV^{-1}cm^{-2}$ after an annealing at **600°C for 15 minutes**.*

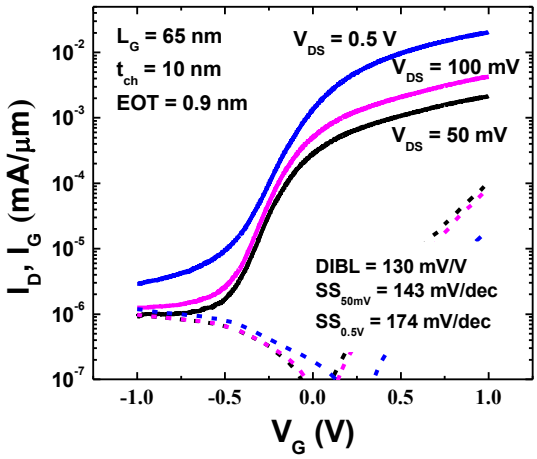

*Fig 4: I_D-V_G (full lines) and I_G-V_G (dashed lines) characteristics measured for several V_{DS} (50 mV, 100 mV and 0.5 V) on a gate-first MOSFET as described in Fig. 1 with a **65 nm gate length**. This device exhibit a good I_{ON}/I_{OFF} ratio of 7×10^3, with an off-current dominated by gate leakage. The low on-current is limited by the high access resistance due to the too large L_{SIDE} of 35 nm.*

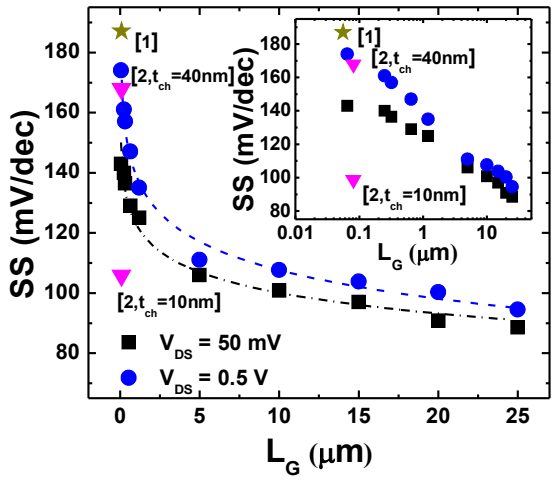

*Fig. 5: Sub-threshold swing (SS) versus gate length (L_G) measured at V_{DS} = 50 mV and V_{DS} = 0.5 V for gate-first MOSFETs as described in Fig. 1. Long-channel devices exhibit a good **SS of 88 mV/dec** at V_{DS} = 50 mV, while short-channel devices show a good electrostatic integrity with a **SS of 143 mV/dec** at V_{DS} = 50 mV and L_G = 65 nm.*

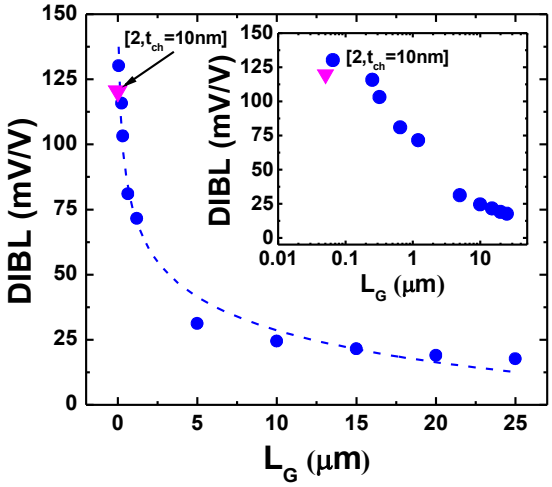

*Fig. 6: Drain-induced barrier lowering (DIBL) versus gate length (L_G) measured between V_{DS} = 100 mV and V_{DS} = 0.5 V for gate-first MOSFETs as described in Fig. 1. These devices exhibit an excellent DIBL scalability comparable to best reported planar devices[2] with a long-channel DIBL of 18 mV/V and a short-channel **DIBL of 130 mV/V at L_G = 65 nm**.*

Session V.B (Dean's Hall II)

Spin/Memory Devices

Tuesday PM, June 19th, 2012

Session Chair(s): Brian Doyle, Intel Corporation and Andy Kent, NYU

1:30 PM V.B-1 Invited Paper
Ultrafast Spin Torque Memory Based on Magnetic Tunnel Junctions with Combined In-plane and Perpendicular Polarizers
I. N. Krivorotov[1], G. E. Rowlands[1], T. Rahman[2], J. A. Katine[1], J. Langer[4], A. Lyle[4], H. Zhao[2], J. G. Alzate[5], A. A. Kovalev[6], Y. Tserkovnyak[6], Z. M. Zeng[6], H. W. Jiang[6], K. Galatsis[5], Y. M. Huai[7], P. Khalili Amiri[5], K. L. Wang[5], and J.-P. Wang[2], [1]Physics and Astronomy, University of California, Irvine, California, USA, [2]Electrical and Computer Engineering, University of Minnesota, Minneapolis, Minnesota, USA, [3]Hitachi Global Storage Technologies, San Jose, California, USA, [4]Singulus Technologies,Kahl am Main, GERMANY, [5]Electrical Engineering, University of California, Los Angeles, California, USA, [6]Physics and Astronomy, University of California, Los Angeles, California, USA, and [7]Avalanche Technology, Fremont, California, USA

2:10 PM V. B -2 Invited Paper
NanoMagnet Logic
W. Porod, P. Li, F. Shah, M. Siddiq, E. Varga, G. Csaba, V. Sankar, G. H. Bernstein, X. S. Hu, M. Niemier, J. Nahas, and A. Orlov, Center for Nano Science and Technology, University of Notre Dame, Notre Dame, Indiana, USA

2:50 PM V. B-3
Late News

3:10 PM Break

3:30 PM V. B-4
Nanowire Phase Change Memory with Carbon Nanotube Electrodes
F. Xiong[1,2,3], M.-H. Bae[1,2], Y. Dai[1,2], A. D. Liao[2], A. Behnam[1,2], E. Carrion[1,2], S. Hong[1,2], D. Ielmini[4] and E. Pop[1,2,3], [1]Micro & Nanotechnology Lab, Univ. Illinois, Urbana-Champaign, Illinois, USA, [2]Dept. of Electrical & Computer Engineering, Univ. Illinois, Urbana-Champaign, Illinois, USA, [3]Beckman Institute, Univ. Illinois, Urbana-Champaign, Illinois, USA, and [4]Dipartimento di Elettronica e Informazione, Politecnico di Milano, Milano, ITALY

3:50 PM V. B-5
A very reliable multilevel YSZ resistive switching memory
F. Pan, J. Jang,and V. Subramanian, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, California, USA

4:10 PM V. B-6
A Comprehensive Model for Crossbar Memory Arrays
A. Chen, Z. Krivokapic, and M.-R. Lin, TD Research, GLOBALFOUNDRIES, Sunnyvale, California, USA

4:30 PM V. B-7
Spin Neuron for Ultra Low Power Computational Hardware
M. Sharad, G. Panagopoulos and K. Roy, School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana , USA

Ultrafast Spin Torque Memory Based on Magnetic Tunnel Junctions with Combined In-plane and Perpendicular Polarizers

I. N. Krivorotov[1], G. E. Rowlands[1], T. Rahman[2], J. A. Katine[1], J. Langer[4], A. Lyle[2], H. Zhao[2], J. G. Alzate[5], A. A. Kovalev[6], Y. Tserkovnyak[6], Z. M. Zeng[6], H. W. Jiang[6], K. Galatsis[5], Y. M. Huai[7], P. Khalili Amiri[5], K. L. Wang[5], J.-P. Wang[2]

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Since the initial prediction and experimental demonstration of magnetization reversal by spin transfer torque (STT), there has been continuous progress toward the development of nonvolatile magnetic random access memory based on STT switching (STT-RAM) in nanoscale magnetic tunnel junctions (MTJs). In the most common STT-RAM configuration shown in Fig. 1(a), the magnetic moments of the free layer and the pinned polarizing layer of an MTJ lie collinear to one another in the plane of the junction. In this configuration (in-plane STT-RAM or IST-RAM), STT is small during the initial stages of the free layer's magnetic moment reversal, resulting in a relatively long nanosecond-scale switching time. Switching can be greatly accelerated in an alternative STT-RAM configuration, in which a second polarizer with magnetic moment perpendicular to the MTJ plane is added to the magnetic multilayer (orthogonal STT-RAM or OST-RAM). The initial STT from the perpendicular polarizer is large and has been predicted to induce ultrafast precessional switching of the free layer's magnetization on a time scale of 100 ps. The differences in the reversal modes expected for the IST-RAM and OST-RAM devices are illustrated in Figs. 1(c) and 1(d), wherein magnetization switching trajectories are shown for the two types of memory.

Here report measurements of ultrafast switching of magnetization in OST-RAM devices (Fig. 1(b)). We present a direct comparison of STT switching in IST-RAM and OST-RAM devices with nearly identical dimensions and multilayer compositions except for the presence of the perpendicular polarizer in the OST-RAM structure. The OST-RAM devices studied in this letter are 180×70 nm^2 elliptical nanopillars shown in Fig. 1(b) patterned from the following multilayer: (bottom lead)/ (in-plane polarizer)/ (barrier)/ (free layer)/ (barrier)/ (perpendicular polarizer)/ (cap). In these devices, (in-plane polarizer) ≡ $Pt_{37}Mn_{63}(20)$/ $Co_{70}Fe_{30}(2.5)$/ Ru(0.85)/ $Co_{40}Fe_{40}B_{20}(2.4)$, (perpendicular polarizer) ≡ $Co_{60}Fe_{20}B_{20}(0.75)$/ $[Co(0.3)\ /Pd(1.0)]_{10}$, (barrier) ≡ MgO(0.82), and (free layer) ≡ $Co_{60}Fe_{20}B_{20}(2.0)$ with the layer thicknesses given in nanometers. The reference IST-RAM devices in Fig. 1(a) are similar to the OST-RAM devices but lack the perpendicular polarizer.

We use vibrating sample magnetometry (VSM) to verify the presence of perpendicular magnetic anisotropy in the additional polarizer. Figure 2(a) shows VSM measurements for a magnetic field applied perpendicular to the plane of an unpatterned multilayer. The effectiveness of the $[Co(0.3)\ /Pd(1.0)]_{10}$ superlattice as a perpendicular polarizer is demonstrated by a nearly 100% remanence of the polarizer's magnetization. Figure 2(b) shows resistance versus magnetic field applied in the plane of an OST-RAM device. The observed magnetoresistance is due to switching of the free layer between parallel and antiparallel configurations with the in-plane polarizer.

We test the predicted differences in the switching of IST-RAM and OST-RAM devices by measuring the probability of reversal of the free layer in response to voltage pulses of varying magnitude and duration. Measured switching probability for an IST-RAM device is shown in Fig. 3(a) as a function of the applied voltage pulse magnitude and duration. These data illustrate that the pulse width required to achieve 50% switching probability, t_{50}, decreases with increasing pulse amplitude but remains long: 0.92 ns even at the maximum pulse amplitude of 0.74 V. Figure 3(b) shows the switching probability as a function of the pulse duration for the OST-RAM device. A large reduction in switching time is apparent, with the shortest observed value of 0.12 ns at the pulse amplitude of 1.58 V. The dependence of the switching time on the voltage pulse amplitude is summarized in Fig. 4(a).

To quantify the write energy reduction in OST-RAM, we plot the switching probability as a function of energy dissipated during the write process in Figs. 3(c) and 3(d). Figure 4(b) shows the write energy required to achieve 50% switching probability as a function of write pulse width, t_{50}, for both IST-RAM and OST-RAM devices. The minimum write energy for OST-RAM devices is 0.4 pJ, which is a significant reduction over the IST-RAM device, for which the minimum energy per write is 1.25 pJ. In conclusion, we have shown that adding a perpendicular polarizer to a standard IST-RAM device can significantly reduce the write time and the write energy.

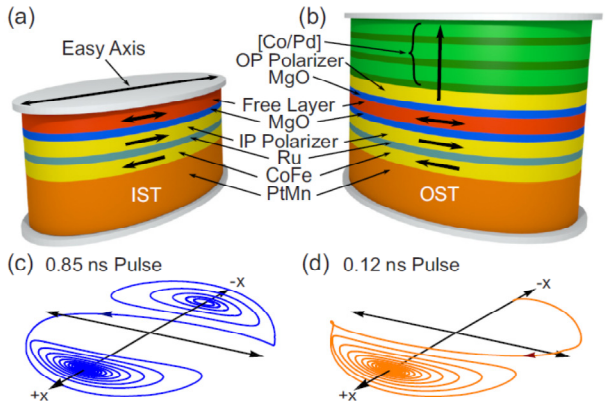

Fig. 1. (a) Schematic of the IST-RAM device consisting of a pinned in-plane synthetic antiferromagnetic polarizer and a CoFeB free layer. (b) OST-RAM device made by adding a perpendicular polarizer to the IST-RAM device. Simulated macrospin trajectories of magnetization starting near the negative x direction in response to 2.4×10^7 A/cm^2 square pulses in (c) IST-RAM and (d) OST-RAM.

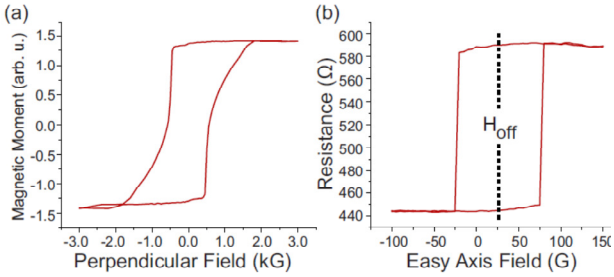

Fig. 2. (a) VSM measurement of an unpatterned OST-RAM multilayer for a magnetic field applied perpendicular to the plane. (b) Resistance of an OST-RAM device versus in-plane easy-axis magnetic field.

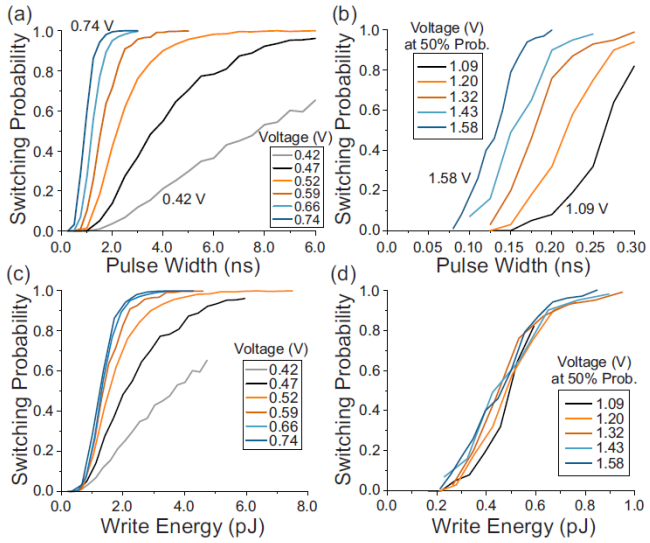

Fig. 3 Switching probability as a function of the applied voltage pulse duration and magnitude for (a) IST-RAM and (b) OST-RAM devices. Voltage labels for OST-RAM data are the values at 50% switching probability. Switching probability as a function of energy delivered to (c) IST-RAM and (d) OST-RAM devices.

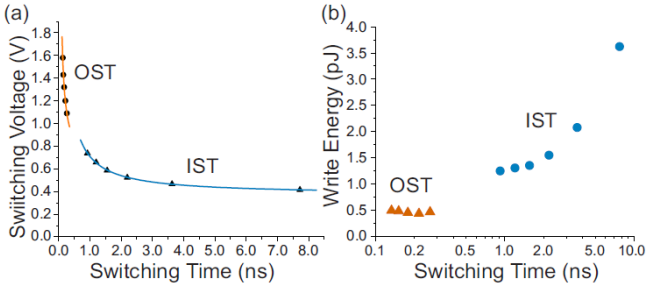

Fig. 4. (a) Switching voltage for IST-RAM and OST-RAM devices plotted as a function of pulse width at 50% switching probability, t_{50}. Solid lines are best fits described in the text. (b) Energy per write at 50% switching probability plotted as a function of switching time, t_{50}.

NanoMagnet Logic

Wolfgang Porod, Peng Li, Faisal Shah, Mohammad Siddiq, Edit Varga, Gyorgy Csaba, Vijay Sankar, Gary H. Bernstein, X. Sharon Hu, Michael Niemier, Joseph Nahas, and Alexei Orlov

Center for Nano Science and Technology, University of Notre Dame, IN 46556

We present recent results on implementing logic using physically- coupled nanomagnet arrays. The binary state of a bit is represented by the magnetization state of a single-domain nanomagnet element, and logic is accomplished through direct physical interactions between them. We refer to this approach as nanomagnet logic (NML). We have demonstrated that NML satisfies the requirements for digital logic, and offers performance advantages, primarily low power and non-volatility, as a potential post-CMOS technology.

A fully functional NML system comprises an electronic/magnetic interface to serve as data inputs, closely coupled magnetic devices that store and process information, a method for controlling the flow of data through the logic path, and an electronic readout mechanism. So far, all but the readout have been experimentally demonstrated at Notre Dame. The clocking field is generated by underlying copper wires whose magnetic field influences a large number of nanomagnets residing on its surface. We are investigating enhanced permeability dielectric (EPD) materials that are deposited over the nanomagnets that reside on the clock wire. The EPD concentrates the magnetic flux to the region occupied by the nanomagnets, thereby lowering the power required to create a sufficiently high field necessary to null the nanomagnets between clocking cycles. Various shapes of nanomagnets have been shown to enhance various aspects of the functionality of the nanomagnets within an NML system. For example, by appropriately shaping the nanomagnets so that they possess an internal bias, we have demonstrated that preferred ground states can be built into the gates, allowing them to provide yet more functionality with an even smaller footprint.

This talk will summarize the most recent work in several areas of NML development including nanomagnet lithography and fabrication, field-coupled input devices, recent progress developing multilayer magnetic stacks that use tunneling and spin torque to effect input and output devices, embedded clock line fabrication methods, EPD materials that show large enhancements in both permeability and saturation magnetization, and progress with larger NML circuits.

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Nanowire Phase Change Memory with Carbon Nanotube Electrodes

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Data storage based on phase change materials (PCMs) encodes information as the crystalline or amorphous state of the material bit, which have a resistivity ratio $>10^3$. PCM resistive storage is thought to be more scalable [1] than charge-based devices like Flash, which are prone to leakage at nanoscale dimensions. However, PCM technology has historically suffered from relatively high (~0.5 mA) programming currents [2] needed to change the phase of the material bit through Joule heating.

Here, we describe PCM nanowires (NWs) that are self-aligned with carbon nanotube (CNT) electrodes, achieving switching currents of the order ~1 μA, over two orders of magnitude below industrial state of the art. Such devices confine the PCM bit in three-dimensions, unlike previous efforts with CNT electrodes [3-5], and approach the fundamental scaling limits of this technology. To self-align NWs with CNTs without complex lithography, we first cover CNT devices with a thin (~50 nm) layer of PMMA (Figs. 1a-c). We flow current in the CNT such that its Joule heating [3] causes the PMMA covering it to evaporate [5], leaving behind a nanotrench (Figs. 1d-e). We create nanogaps in the exposed CNT by electrical breakdown (Fig. 1f) [4], sputter ~10 nm of $Ge_2Sb_2Te_5$ (GST) then lift-off the remaining PMMA; this leaves behind a PCM NW perfectly aligned with the two CNT electrodes (Figs. 1g-i).

Figure 2a shows current-voltage (*I-V*) characteristics of a typical device under dc current sweep, demonstrating SET switching from the high resistance amorphous phase of the bit (R_{OFF} ~ 2.5 GΩ) to the low-resistance crystalline state (R_{ON} ~ 1.3 MΩ). The SET switching is initiated at a threshold voltage (V_T) through a field-induced transition of the amorphous phase; Joule heating then heats up and crystallizes the bit (at ~150 ºC) into the conductive state. The V_T of our devices decreases by 20-30% after the first few switching cycles, such "burn-in" being consistent with previous reports [5]. Reversible memory switching is achieved with pulsed operation (Fig. 2b). The bit is re-amorphized (RESET) with a ~100 ns current pulse which heats up the crystalline GST to its melting point (~620 ºC) then quenches it back to a disordered amorphous GST state during the short falling edge of the pulse. A memory endurance test (Fig. 2c) shows that the device can be reversibly programmed for nearly 1500 cycles. We note that such devices are capped by a thin (~10 nm) layer of SiO_2, which protects the GST from oxidation; however, the capping and passivation of such devices are not yet optimized and could be improved.

We plot the R_{ON} and R_{OFF} of 102 self-aligned PCM NW devices against their respective V_T in Fig. 3. The mean ratio R_{OFF}/R_{ON} is ~ 900 for all measured devices. A few devices have off/on ratio ~2000, approaching the intrinsic switching limits of the GST material resistance. Such a high off/on ratio has not been previously achieved, and it is very promising for multilevel memory applications even at the most reduced bit dimensions. Figure 4 shows that the RESET and SET currents of our devices scale approximately with the electrode tip area, estimated as $\pi d^2/4$ where d is the CNT diameter. Here, the small diameter of the CNT electrodes and their high conductivity are essential for the ultra-low power operation.

In conclusion, we presented a novel technique to fabricate self-aligned PCM NW devices with CNT electrodes. The programming currents (~0.1 μA SET, ~1.6 μA RESET) and power dissipation of these devices are among the lowest reported to date. Such devices also offer outstanding R_{OFF}/R_{ON} ratio ($\sim 10^3$), approaching the intrinsic limits of the GST material. The powerful yet simple nanopatterning method could also be used to probe other nanomaterials by automatically aligning them with CNT electrodes.

[1] M. Wuttig et al, *Nat. Mat.* **6**, 824 (2007)
[2] G. Servalli et al, *IEEE IEDM Tech. Dig.* 113 (2009)
[3] F. Xiong et al, *Appl. Phys. Lett.* **95**, 243103 (2009)
[4] F. Xiong et al, *Science* **332**, 568 (2011)
[5] J. Liang et al, *IEEE Symp. VLSI Tech. Dig.* 100 (2011)
[6] C.Y. Jin et al, *Nano. Lett.* **11**, 4818 (2011)

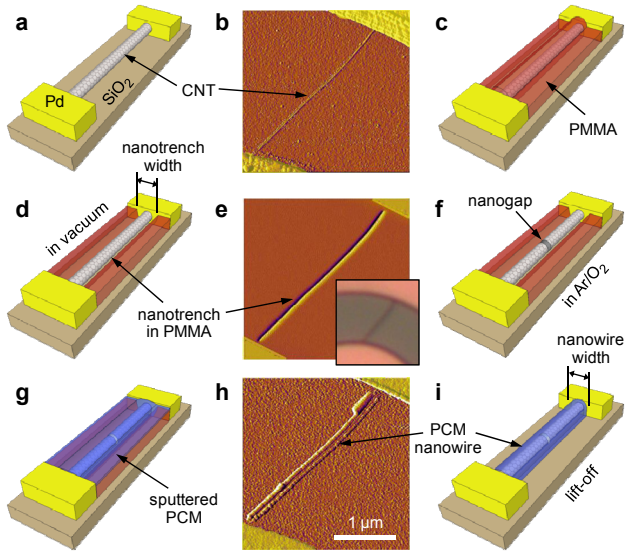

Fig. 1. Schematics and AFM imaging of self-aligned device. (**a**) CNT between two Pd electrodes. **(b)** AFM of a CNT with length $L \sim 3.1$ μm and diameter $d \sim 2.2$ nm. **(c)** The CNT device is covered with a thin layer (~50 nm) of PMMA. **(d)** Current flow in the CNT leads to Joule heating and nanotrench formation along it as the PMMA evaporates (in vacuum). **(e)** AFM imaging of nanotrench (~90 nm wide) in PMMA. Inset shows nanotrench is visible under the optical microscope, enabling quick detection. **(f)** CNT nanogap is formed by electrical cutting under Ar/O_2 flow. **(g)**, PCM deposition covers the device and fills the nanogap and nanotrench. **(h-i)** AFM imaging and schematic of self-aligned NW with CNT electrodes obtained after PMMA lift-off. Some devices were further encapsulated with a ~10-nm layer of evaporated SiO_2.

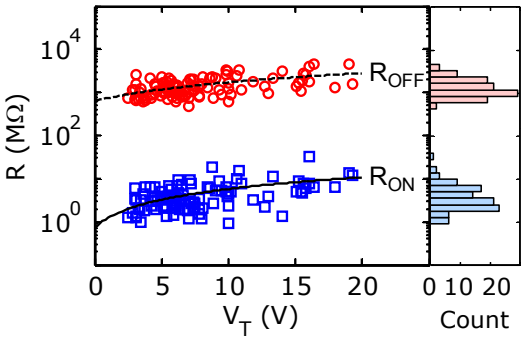

Fig. 3. Device statistics. On and off-state resistance of 102 self-aligned PCM NW devices, plotted against their threshold voltages V_T. The solid and dashed fits suggest approximately linear scaling between R and V_T, both governed by the bit size within the CNT nanogap. The average R_{OFF}/R_{ON} is ~ 900. The right panel shows a histogram of the same data set.

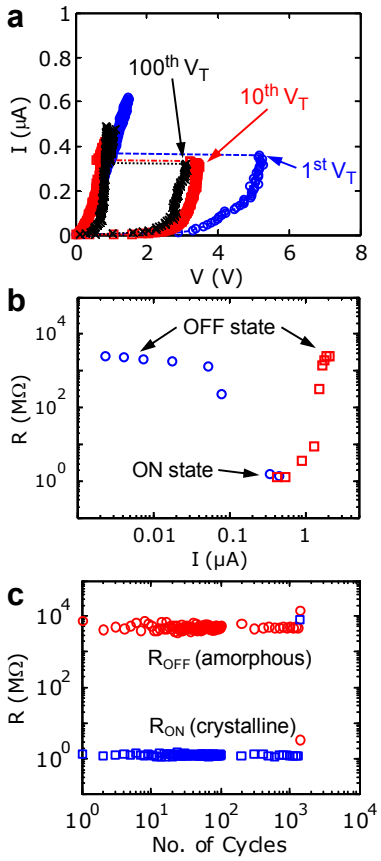

Fig. 2. Device electrical characteristics. (a) Electrical characteristics of the 1st, 10th and 100th SET switch of a typical self-aligned PCM NW device, showing V_T stabilizes at 3.2 V. **(b)** Resistance switching after a series of current pulses with increasing amplitude. SET (RESET) pulses have 300 ns (100 ns) width and rising (falling) edges of 50 ns (2 ns). The SET (RESET) current of this device is ~0.4 μA (~1.9 μA). The ratio R_{OFF}/R_{ON} is ~2000×. **(c)** Endurance test over nearly 1500 cycles of operation.

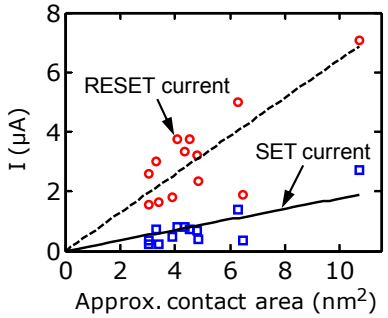

Fig. 4. Current scaling. SET and RESET programming currents of 13 self-aligned devices suggest pseudo-linear scaling as a function of CNT electrode tip area. The solid (dashed) line is a linear fit with a slope of 0.17 μA/nm^2 (0.64 μA/nm^2).

A very reliable multilevel YSZ resistive switching memory

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Resistive Random Access Memory (RRAM) has emerged as a candidate for scaled memories [1]. To date, even though several metal oxide systems have been shown to exhibit resistive switching characteristics [2], a few of them have multilevel programming (MP) capability. Yttria Stabilized Zirconia (YSZ) which is widely used in electrochemistry applications has been largely unstudied, which is surprising given its high ionic mobility and excellent stability. Here, we demonstrate RRAM cells based on YSZ showing excellent performance in all metrics and we show that these devices have very reliable MP capability and in addition we demonstrate the use of an incremental step pulse programming scheme (ISPP) to realize an excellent balance between programming window, lifetime, and endurance. Finally, we demonstrate that oxygen vacancy (OV) based memories have better reliability than metallic filament based devices and are more suitable for multilevel use.

The device structures used are shown in Fig. 1; Ti/YSZ cells are OV-based cells, while Cu/YSZ cells show metallic filamentary programming. The YSZ film thickness varies from 20nm to 3nm. The bottom Au electrode effective contact area ranges from 3600 um^2 to $4um^2$. Fig. 2 shows 300 cycles of DC I-V sweeps for a typical Ti/YSZ device, establishing excellent repeatability. The on-state resistance (R_{on}) in both Cu/YSZ and Ti/YSZ devices is determined by the current compliance, as shown in Figs. 3 and 4. For Cu/YSZ, CC $\times R_{on} \approx 0.3$, whereas this value is around 1 for Ti/YSZ. This indicates that Cu/YSZ is more power efficient due to the high diffusivity and high conductivity of Cu. As shown in Fig. 2 and Fig. 3, both types of devices shows a sharp transition in the SET stage. However, in contrast to Cu/YSZ, Ti/YSZ shows a very smooth transition during the RESET stage. This is further demonstrated in Fig. 5, where the ISPP is used (shown in the inset) and the duration of the programming pulse is set to 1μs. It can be seen that after a V_{RESET} threshold, the R_{off} of Ti/YSZ exponentially increases with applied voltage, whereas a steep transition occurs for Cu/YSZ and after that its resistance remains constant. Unlike Cu/YSZ, a smooth transition for Ti/YSZ offers the opportunity for implementation of MP. Even though Cu/YSZ can also achieve MP based on different CC levels as shown in Fig.4, it will be shown that such states are very noisy and not reliable. Fig. 6 shows the successful implementation of four programming levels for Ti/YSZ cells. The device has a low resistance state of ~8kΩ and three distinct high resistance states up to 2 MΩ. Such a large resistance ratio window makes MP clearly feasible. In addition, there is no programming error during one thousand cycles of programming. Furthermore, the retention of this multilevel device is very good as shown in Fig.7. The device does not show significant degradation for the entire testing period of 10^4 seconds at 80 ℃. By utilizing the aforementioned ISPP scheme, an excellent balance between programming window and device endurance can be achieved (Fig. 8). This technique guarantees a predefined resistance window between R_{on} and R_{off} that is satisfied during every cycle. For a given resistance window, the technique guarantees a minimum electrical stress applied to the device such that maximized device endurance can be attained. The traditional single pulse programming techniques, on the other hand, cause the ratio of R_{off}/R_{on} ratio to be statistically distributed at every cycle. In addition, it is difficult to get an optimized pulse magnitude. For example if the magnitude of V_{SET} is small, the SET process will become less effective as cycles increase (shown in Fig. 8); on the other hand if the pulse magnitude is too large, the device will breakdown quickly and lifetime seriously reduces. By using ISPP, we found that for *almost every device*, the endurance is greater than 10^4 cycles (limited by measurement time), which is a significant improvement compared to the single pulse scheme (Fig. 8). The relationship between V_{SET} and V_{RESET} during ISPP is shown in Fig. 9. It can be seen that the magnitude of V_{SET} and V_{RESET} are linearly dependent and the slope is ~1. Finally, the reliability of both types of devices is studied. Fig. 10 shows the resistance sampling for both Cu/YSZ and Ti/YSZ. Random telegraph noise (RTN) is clearly seen in Cu/YSZ device. At the same resistance level, Ti/YSZ has much lower noise than Cu/YSZ (Fig. 10 and 11). This can be explained by the fact that the conductivity of Cu filament is much larger than the conductivity of OV filament thus for a given resistance state the width of the metallic filament is much narrower than the OV filament. Therefore, the Cu-based devices are more vulnerable to the atomic motion of the Cu atoms at the edge of the filament. The noise goes worse when the resistance increase since the filament become narrower. This makes the Cu/YSZ improper for using in multilevel cells, unlike the Ti/YSZ cells, which show excellent multilevel cell behavior.

In summary, we demonstrate an excellent RRAM device based on YSZ. Robust multilevel operation is achieved using incremental step pulse programming. Using this scheme, we realize excellent reliability, and further, demonstrate that oxygen vacancy-based cells are superior to metallic filament cells for multilevel operation.

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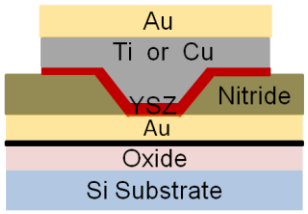

Fig.1: Device structure. YSZ film thickness varies from 20nm to 3nm. The bottom Au electrode effective contact area ranges from 3600 um^2 to $4um^2$

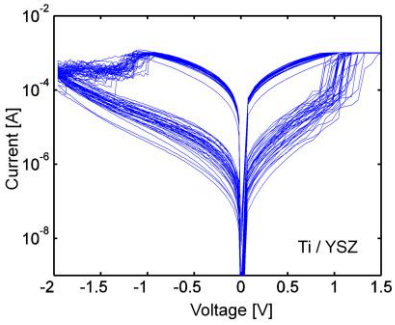

Fig. 2: 300 repetitive I-V sweeps for a typical Ti/YSZ device (The sweep count was limited by practical measurement times). YSZ film thickness 10nm. Device area 16um by 16um.

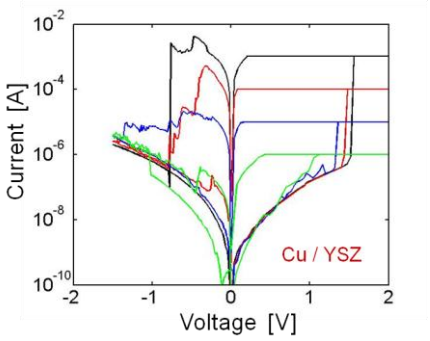

Fig. 3: The I-V characteristics of a typical Cu/YSZ device as a function of current compliance.

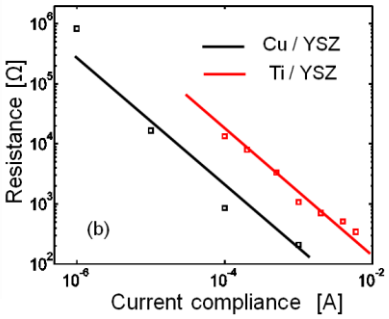

Fig. 4: The on state resistance R_{on} versus current compliance

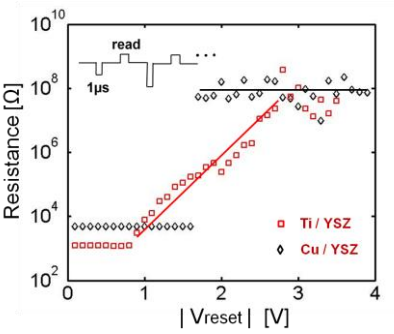

Fig. 5: Off state resistance versus the different V_{RESET} pulses with duration 1 μs. Inset shows the increment pulse programming technique.

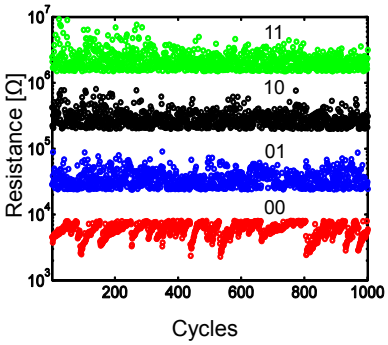

Fig. 6: Four level multilevel programming (MP) for Ti/YSZ devices.

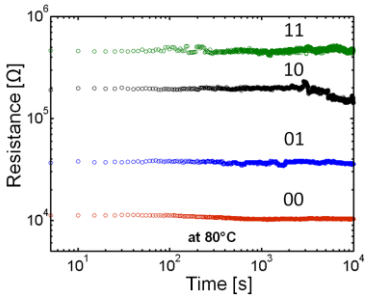

Fig. 7: Retention properties of the multi-level Ti/YSZ RRAM at 80 ℃ (The read voltage is 100mV).

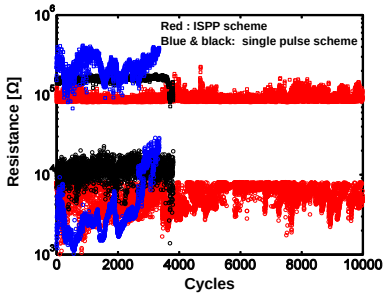

Fig.8: Endurance comparison between the single pulse programming scheme and incremental step pulse scheme.

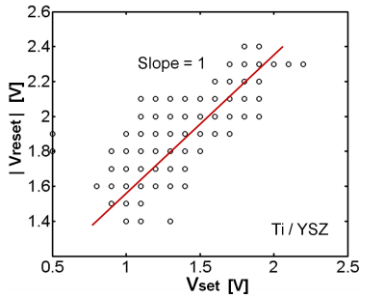

Fig. 9: The relationship between V_{SET} and V_{RESET} for an endurance test of 10^4 cycles.

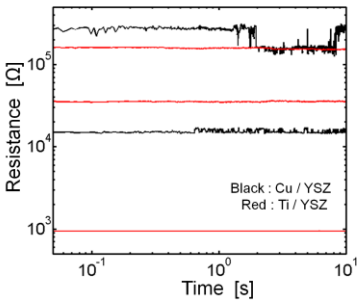

Fig. 10: Resistance sampling for both Cu/YSZ and Ti/YSZ devices at different resistance states.

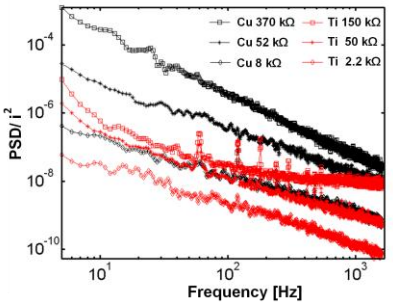

Fig. 11: Normalized noise power spectrum density for both types of devices at different resistance states.

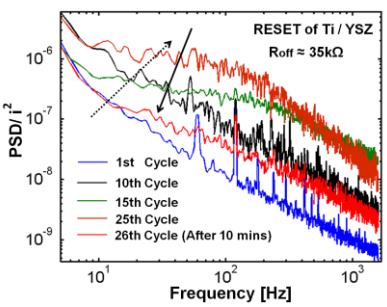

Fig. 12: The dependence of normalized noise spectrum on the switching cycles in the RESET stage.

A Comprehensive Model for Crossbar Memory Arrays

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Abstract

A crossbar array model with complete solutions for arbitrary memory and selector device behaviors (e.g., nonlinear, rectifying, *etc*.) is presented in this paper to analyze various array designs and device options. Voltage/current decay due to line resistance limits practical size of linear crossbar arrays below 10kbit. Less than 2% current reaches the end of a line in a small 1kbit array. Nonlinearity in memory characteristics and select diodes improve sensing margin from below 5% to above 30% in a 1kbit array. The voltage window between selected and unselected devices is increased from $<5\%V_{dd}$ to $>20\%V_{dd}$ by nonlinearity and $>40\%V_{dd}$ by select diodes. This model provides quantitative evaluation for crossbar array designs and enables statistical analysis of array characteristics.

Introduction

Crossbar arrays with switching devices built at junctions of wordlines (WL) and bitlines (BL) can achieve the smallest footprint of $4F^2$ and enable high-density memory design [1]. They have also been explored for novel applications, e.g., crossbar logic [2], reprogrammable circuits [3], neuromorphics [4], *etc*. Crossbar array has become an attractive architecture for emerging memories with two-terminal structures, including resistive random-access-memory (RRAM). However, the benefit of its simple and compact structures is often compromised by large number of leakage paths that degrade accessibility to specific devices in the array and operation efficiency. Reading crossbar arrays requires distinguishable output signals for a selected device in different states. Switching requires sufficient current and voltage to be delivered to a selected device. Both operations need to minimize disturbance on unselected devices and maximize power efficiency. This paper presents a comprehensive model for quantitative analysis of the design and performance of crossbar arrays based on matrix algebra.

Complete crossbar array solution based on matrix algebra

Fig. 1(a) illustrates the crossbar array and design parameters used in this model. Line resistance (R_L) is defined as the resistance between two adjacent devices along WLs (R_{WL}) or BLs (R_{BL}). Voltage sources can be applied on one side or two sides of WLs/BLs. WL/BL access resistance can be appropriately chosen for reading and writing operations. Extremely high access resistance is essentially equivalent to floating lines. A m×n crossbar array can be completely described by 2mn variables, i.e., junction voltage on the WL and BL planes: $V_{WL}(i,j)$, $V_{BL}(i,j)$, $1\le i\le m$, $1\le j\le n$. The Kirchhoof's law defines two constraints (along WL and BL) at every junction and therefore totally 2mn equations for these variables, as shown in Fig. 1(b). The 2mn equations can be solved using matrix algebra to obtain 2mn junction voltages $\{V_{WL}, V_{BL}\}$, from which all array performance parameters can be derived. Random resistance patterns can be generated for statistical analysis.

Line resistance (R_L) can cause significant voltage decay in large arrays (Fig. 2). Even for R_L as small as $10^{-4}R_{on}$, only $<80\%V_{dd}$ can be delivered beyond 100 devices along a selected WL. For a typical RRAM device with R_{on} = 10kΩ, this R_L value is only 1Ω. Partial bias schemes ("1/3 bias" and "1/2 bias") improve voltage delivery by raising unselected WL/BL voltage from 0, as shown in Fig. 2(b) and (c). Disturbance is a major challenge for crossbar arrays: the maximum voltage on unselected devices (i.e., disturbance) may exceed the voltage delivered to a selected device (Fig. 3). Partial bias schemes also reduce the disturbance; however, the "select-unselect voltage gap" diminishes eventually with increasing array size and R_L. Devices closest to voltage sources receive the best voltage delivery ("best corner"), but voltage to devices furthest from voltage sources ("worst corner") decays dramatically, as shown in the map of selected device voltage for every junction in a 1kbit array in Fig. 4(a). Applying voltages from both sides of WLs/BLs moves the worst corner into the array center and reduces voltage window between the best and worst corners (Fig. 4(b)). Two-side voltage sources are unusual in CMOS memory arrays due to high periphery overhead, but crossbar array may be stacked above CMOS periphery circuits and enable two-side sources without lowering array efficiency. The sensing margins at the best and worst corners follow opposite trend with increasing R_L (Fig. 5), because higher R_L helps to isolate the best corner from the rest of the array but makes the worst corner less accessible. Another design challenge for a crossbar array is the current decay (Fig. 6). Even for $R_L=10^{-4}R_{on}$ and a small 32×32 array, less than 2% of current from voltage sources reach the end of a line (i.e., current ratio ~ 50, Fig. 6 inset). The model can also incorporate device variation that is commonly observed in RRAM characteristics. By generating large number of array patterns, crossbar array performance can be evaluated statistically.

Arbitrary memory and selector device behaviors

Crossbar array of linear devices analyzed above has limited design flexibility and application space. Array performance may be improved with nonlinear memory devices or select diodes. Arbitrary device behaviors (e.g., nonlinear, rectifying, *etc*.) can be included in this model using iteration and convergence control, providing a fully functional crossbar array evaluation platform.

Fig. 7 shows significant improvement in sensing margin from linear to nonlinear device arrays, with a simple parabolic shape of nonlinearity: $I(V) = a\cdot V+b\cdot V^2$ (LRS and HRS have different a and b coefficients). Nonlinearity enlarges the select-unselect voltage gap (Fig. 8(a)) and improves power efficiency (Fig. 8(b)). Voltage decay is also reduced in nonlinear device arrays (Fig. 9). These improvements can be attributed to higher effective resistance of unselected devices due to voltage-dependent resistance. With the assumed parabolic nonlinearity, effective junction resistance increases by (2–6)× and the increase is more prominent further away from voltage sources where device voltages are lower (Fig. 10).

More improvement is achieved with select diodes. A simplified two-segment model is used here to describe diode characteristics: $R_{diode}=R_r$ ($>>R_{on}$) for $V<0$; $I(V)=\exp(qV/nkT)$ for $V>0$ (n is an ideality factor). Select diodes increase the sensing margin from ~5% to 17%–35% depending on R_r (Fig. 11). Both nonlinearity and select diode improve the voltage window between selected and unselected devices, from $<5\%V_{dd}$ to $>20\%V_{dd}$ and $>40\%V_{dd}$ respectively (Fig. 12). Nonlinearity increases junction resistance and makes R_L relatively smaller, which improves voltage delivery to selected devices. Diodes are more effective in reducing disturbance and provide an overall larger operation voltage window.

Summary

A novel crossbar array model capable of incorporating arbitrary device characteristics is proposed. It provides a comprehensive platform for the design and analysis of crossbar arrays in various applications. Leakage paths and line resistance limit practical crossbar array size. Nonlinearity and select diodes improve sensing margin, switching voltage, and power efficiency; however reliable nonlinear and rectifying devices are yet to be found in experiments. This model provides a useful tool to evaluate emerging memories and select devices for crossbar array architectures.

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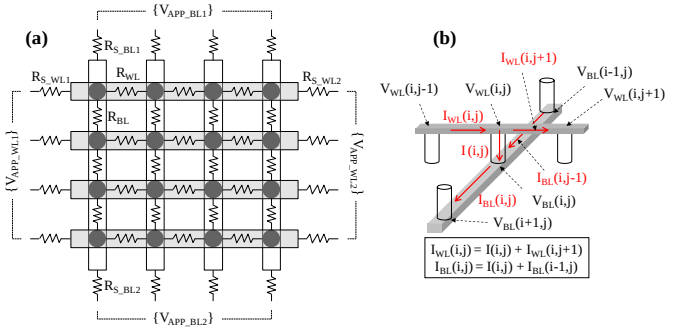

Fig. 1 (a) The crossbar array model and design parameters: WL/BL bias, line resistance, and access resistance from voltage sources; (b) Kirchhoff's law at each junction point.

Fig. 2 Voltage decay along a selected WL up to 512 devices for different line resistance (R_L = 10^{-6}, 10^{-5}, 10^{-4}, and 10^{-3}, normalized to R_{on}) in three bias schemes: (a) unselected WLs/BLs all grounded; (b) "1/3 bias scheme" where unselected WLs biased to $V_{dd}/3$ and unselected BLs biased to $2V_{dd}/3$; (c) "1/2 bias scheme" where unselected WLs/BLs biased to $V_{dd}/2$. (Selected WL = V_{dd}, selected BL = 0)

Fig. 3 Compare voltage delivered to a selected device at the end of WL (i.e., device 512) and the maximum voltage on unselected devices for the three bias schemes in Fig. 2.

Fig. 4 Map of voltage delivery in a 1kbit array (32×32) with (a) one-side voltage sources, (b) two-side voltage sources. Color represents magnitude of effective voltage reaching each junction when it is selected. Line resistance is exaggerated here (R_L=$10^{-2}R_{on}$) to illustrate the R_L-induced inhomogeneity of voltage delivery in crossbar arrays. Two-side voltage sources improve the voltage delivered to the worst corner (from ~$0.2V_{dd}$ to ~ $0.5V_{dd}$).

Fig. 5 The dependence of sensing margin on line resistance (R_L) for the reading of the best corner (blue) and the worst corner (red) in a 1kbit crossbar array.

Fig. 6 Current decay along a selected WL in a 1kbit array with 1/3 bias scheme. The inset shows current ratio (current at WL beginning over that at WL end) for R_L/R_{on} of 10^{-5} to 10^{-2}.

Fig. 7 Distribution of sensing margin for a 1kbit array of linear devices and nonlinear devices.

Fig. 8 Compare 1kbit array of linear and nonlinear devices on (a) the gap between selected device voltage and the maximum unselected device voltage, (b) power efficiency (on log-scale) for the selected device in LRS and HRS.

Fig. 9 Voltage decay along a selected WL up to 512 devices for linear devices (solid lines) and nonlinear devices (dashed lines) with different R_L.

Fig. 10 Ratio of effective resistance increase (from linear resistance at V_{dd}) due to nonlinearity in a 1kbit crossbar array. (One-side sources)

Fig. 11 Distributions of sensing margin of 1kbit arrays with linear devices, nonlinear devices, and memory with select diodes (with different diode reverse resistance R_r).

Fig. 12 Compare voltage of a selected device at the end of a 512-device WL and the maximum voltage on unselected devices for linear devices, nonlinear devices, and memory with select diodes.

Spin Neuron for Ultra Low Power Computational Hardware

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We propose a device model for neuron based on lateral spin valve (LSV) that constitutes of multiple input magnets, connected to an output magnet, using metal channels. The low-resistance, magneto-metallic neuron can operate at a small terminal voltage of ~20mV, while performing computation upon current-mode inputs. The spin-based neurons can be integrated with CMOS to realize ultra low-power data processing hardware, based on neural networks (NN), for different classes of applications like, cognitive computing, programmable Boolean/non-Boolean logic and analog and digital signal processing [1, 2]. In this work we present analog image acquisition and processing as an example. Results based on device-circuit co-simulation framework show that a spin-CMOS hybrid design, employing the proposed neuron, can achieve ~100x lower energy consumption per computation-frame, as compared to the state of art CMOS designs employing conventional analog circuits [13].

Fig.1 depicts two different LSV structures with 'decoupled-read-write' paths (DRW-LSV) that were explored for the neuron model. The device in fig.1a employs 'non-local' spin-torque for *nano-magnet* switching [4-7]. Spin-polarized charge-current is injected into the channel through the input magnet m_1. A fraction of 'spin-component' of the channel-current is absorbed by the output magnet m_2, while the rest flows out of the lead. Note that, there is no net charge current injection into m_2. It experiences spin torque due to 'spin-diffusion current' [6, 7]. Experimentally, ~20% efficiency for non-local spin injection (ratio of spin absorbed by the output magnet to the spin current injected into the channel) in LSV has been demonstrated [4, 7]. Fig. 1b shows a DRW-LSV structure that employs local injection. The top area of the output magnet m_2 is divided between read and write ports, separated by a spacer. Although, the input current flows only though a part of m_2, its small dimension ($60x20x1nm^3$) ensures mono-domain behavior and switching of the entire magnet is achieved. The proposed DRW-LSV with local spin injection can achieve higher spin injection efficiency, as the entire spin-component of the channel current flows through the output magnet. Both the structures in fig.1a-b can be represented by the symbol depicted in fig.1c. In both the DRW-LSV structures, the input currents flow along a low-resistance metallic path between the input terminals I_i, and the lead L. The terminal D is used to detect the state of the output magnet, m_2, through the associated magnetic tunnel junction (MTJ), with negligible static current injection into the high resistance tunnel-barrier (using dynamic CMOS latch discussed later).

Fig. 2 shows the device structure for neuron based on DRW-LSV. It constitutes of an output magnet m_1 with MTJ based read-port, and two anti-parallel input magnets m_2 and m_3, with their 'easy-axis' parallel to that of m_1. A preset-magnet m_4, with an orthogonal easy-axis, is used to implement current-mode Bennett-clocking (BC) [6]. A current pulse input through m_4, presets the output magnet, m_1, along its hard axis. The preset pulse is overlapped with the synchronous input current pulses received through the magnets m_2 and m_3. After removal of the preset pulse, m_1 switches back to its easy axis. The final spin-polarity of m_1 depends upon the sign of the difference ΔI, between the current inputs through m_2 and m_3. The lower limit on the magnitude of ΔI (hence, on current per-input for the neuron), for deterministic switching, is imposed by the thermal-noise in the output magnet, and, imprecision in Bennett-Clocking. The effects of these non-idealities have been included in device simulation (fig. 3).

Transfer-function of an artificial neuron can be expressed as the sign-function of weighted sum of inputs, where the individual weights can be either positive or negative. In the proposed device, the neuron functionality is realized by connecting all the positive-weight inputs (excitatory inputs) to its right-spin input-magnet and vice-versa. The output magnet, in effect, evaluates the sign function with the help of Bennett-clocking, where the right-spin state can be regarded as the 'firing state'. The latch shown in fig. 4a detects the state of the neuron MTJ in each cycle and drives a deep-triode-region current source (DTCS) transistor M_S, which in turn transmits current to the receiving neurons. In order to exploit the low voltage operation of the spin-based neurons, two supply levels V and V-ΔV are employed in the design (fig. 4a). The source terminal of the DTCS transistors are connected to V(~1V), whereas, lead terminals (L) of all the neurons are connected to V-ΔV. Hence, the static-current involved in inter-neuron signaling, flow through a small terminal voltage ΔV (~20mV). This reduces the static power consumption resulting from large number of synaptic communication per-cycle in a large network of neurons (fig. 4b). Magnitude of the current-mode signal flowing form output of a neuron to the input of another neuron can be weighted using different schemes. For instance, programmable conductive elements like TiO_2 memristor can be employed in a cross-bar architecture [1] or DTCS transistor dimensions can be varied according to the weight (as in the present work). Earlier, we also proposed the use of domain wall magnets as programmable 'spintronic' synapses for a multi-input, 'all-spin' neuron [2], while the inter-neuron connectivity was realized with the help of DTCS transistors.

The image processing architecture presented in this work is based on cellular neural network (CNN) with 3x3 neighborhoods (fig. 5) [8, 9]. Each neural Processor Element (PE) in the network is connected to its eight surrounding neighbors through a 3x3 feedback-weight template A. The weighted connectivity is realized by using separate weighted fingers (according to template A) for the DTCS transistor of the latch that transmit current-mode signals to the neighbors. A 3x3 feed-forward template B, determines the connectivity of a neuron to the neighborhood inputs (here, photo-sensor current). This can be implemented in a similar way, i.e., using a DTCS transistor with separate fingers for the nine neighbors, weighted according to the template B. In a CNN, each neuron evaluates the sign function of the weighted sum of its neighborhood inputs and outputs in a recursive manner, as expressed in the form of equations given in fig. 5. In each computation cycle, after, the preset signal goes low, the output magnet of a neuron settles to one of its stable states, depending upon the overal spin current received through its inputs and neighboring outputs (Fig. 6).

As mentioned earlier, the computation-current supplied by the DTCS transistors flows through a small terminal voltage ΔV (~20mV). Moreover, the static current flow is limited to small periods, corresponding to magnet switching time (which can be small as compared to the highest image processing frame-rates of practical interest [10]). Thus, the energy-cost of analog-mode computation, E_{comp}, which is generally high in most image sensing applications (based on conventional analog circuits), is greatly reduced and rendered comparable to the energy-component E_{read}, associated with dynamic power consumption in the digital circuits (used for reading-out the processed data from the sensor array) (fig. 9, table-1)[13] . Table-2 (fig. 9) compares the proposed design with some recent CMOS designs, for on-sensor feature extraction and digitization (using successive approximation register ADC, where the neuron acts as a comparator), (fig. 8), respectively, showing large benefits in terms of computation energy.

Fig.7 depicts the device-circuit co-simulation framework employed in this work. The neuron device has been characterized through four-component spin-circuit model [6, 7], which has been benchmarked with experimental data on LSV's. Stochastic Landau-Lifshitz-Gilbert (LLG) was employed in the device model to account for the thermal noise in the neuron magnet [6]. Effect of imprecise BC was modeled by introducing random deviations in the anisotropy of the hard axis magnet (fig. 3). Behavioral model for the neuron derived from the physics based equations, was used in SPICE simulations to assess system-level performance. In order to account for the CMOS process variation upon system performance, 15% 3σ variations in DTCS-transistor threshold was considered. Independent noise sources were added to the two supply lines corresponding to 0.1% peak-to-peak voltage fluctuation [12]. As long as input currents supplied by the DTCS transistors are large enough to overcome the impact of thermal noise in the neuron-magnet, the precision of computation achievable with the proposed scheme, is limited, mainly, by the supply noise [13]. Supply routing schemes need to be explored, that can exploit the dual voltage levels used in the design, to mitigate the impact of common-mode noise.

In conclusion, we proposed spin-based LSV devices that can model specific neuron behavior and are suitable for ultra low power data-procesing/neuromorphic-computation hardware. As an example we showed that, a spin-CMOS hybrid PE can handle analog processing functionality in a highly energy-efficient manner. It was shown that substituting some of the conventional analog processing units in an image acquisition and processing hardware, by the spintronic neuron, can achieve ultra low power computation.

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Reference: [1] Sharad et. al., DAC 2012, [2] Sharad et. al., TNANO 2012 [3] Sharad et. al., IJCNN, 2012,, [4] Kimura et. al, Phys. Rev. Lett. 2006 [5] Sun et. al., Appl. Phys. Lett. 2009. [6] Behin-Ain et. al., Nature Nano. 2010 [7] Behin-Ain et. al, Appl.Phys.Lett. 2011 [8] Cruz et. al, AICSP, 1998 [9] Harrer et. al.,CNNA, 1994. [10] Gamal et. al., IEEE CDM, 2005 [11] Berni et. al, JSSC, 2011, [12] Leung et. al , JSSC, 2003. [13] Sharad et. al., SRC Techcon 2012. [14] Jendernalik et al., BPAS, 2011, [15] Kong et.al, 2007, [16] Kim et. al., ETRI 2005, [17] Ozgun et al., ISCAS 2011, [18] Harpe et. al., ISSCC, 2007, [19] Craninckx et. al., ISSCC, 2007.

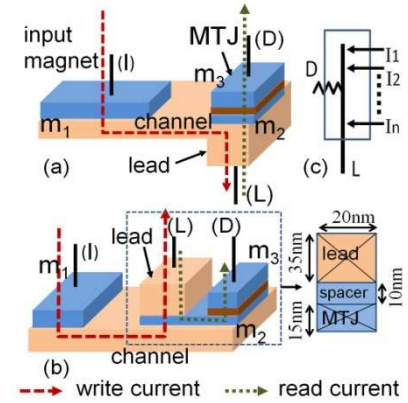


Fig.1 LSV with decoupled read and write paths with, (a) non-local STT and (b) local STT. (c) symbol for multi-input RWD-LSV

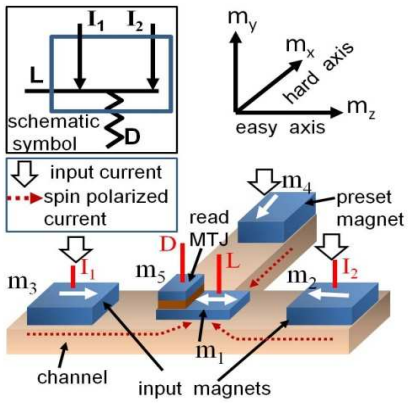


Fig.2 Spintronic neuron based on RWD-LSV and corresponding schematic model: The +ve and -ve inputs of the neuron connect to m_2 and m_3 respectively, m_1 detects the spin polarity of the combined current

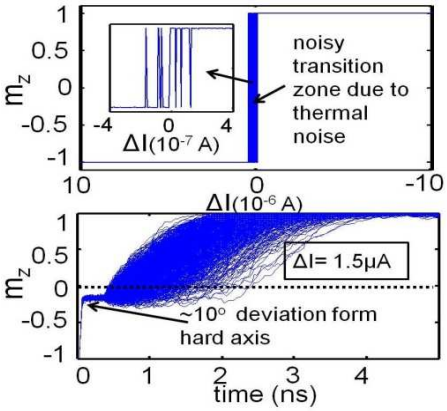


Fig.3 Due to noise in the neuron-magnet and imprecise BC (leading to $m_z \neq 0$ during preset), larger ΔI (hence, current for inter-neuron signaling) is required for correct switching, than the ideal case. Minimum inter-neuron signaling current can be determined on the basis of bit error rate (BER) resulting from these effects. (transients show correct switching for 10000 runs with ΔI =1.5μA for 60x20x1 nm^3 magnet, i.e., BER<0.01%).

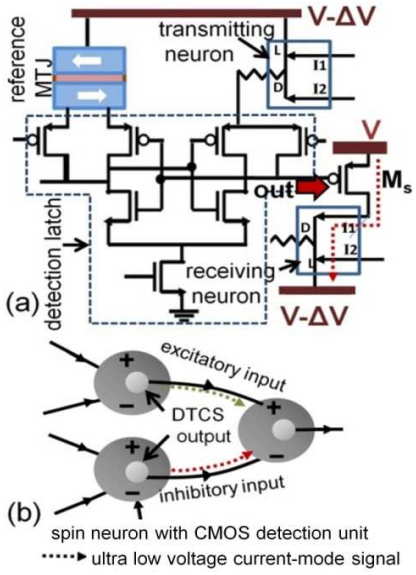
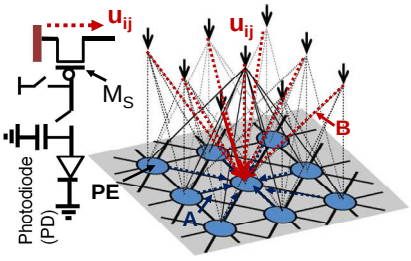


Fig.4 (a) CMOS latch detects the neuron-magnet's state and transmits current to other neurons through M_S. (b) The hybrid PE's (spin-neuron + CMOS latch) communicate using ultra low-voltage current-mode signals.



cell state equation for Discrete-Time CNN

$$x_{ij}(n) = \sum_{(k,l)\in N(i,j)} A(i,j;k,l).y_{kl}(n) + \sum_{(k,l)\in N(i,j)} B(i,j;k,l).u_{kl}(n) + z(i,j)$$

$$y_{ij}(n) = f(x_{ij}(n-1)) = \begin{cases} 1 & if\ x_{ij}(n-1)>0 \\ 0 & if\ x_{ij}(n-1)<0 \end{cases}$$

X(n) : cell state at n_{th} time step
A: 3x3 feedback template
B: 3x3 input template
U(n) :3x3 neighborhood input at T= n
Z : cell bias; y(n): cell output at T=n

Fig. 5 Near-neighborhood architecture of CNN and CNN cell state equation. The DTCS transistors used for supplying input current (proportional to V_{dd}-V_g, where V_g is sampled PD voltage) and for inter-neuron signaling, are weighted according to *A* and *B* template-elements.

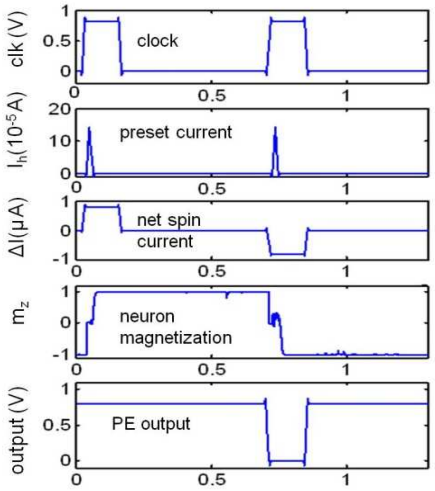


Fig. 6. Timing waveform for PE: Detection latch in each PE evaluates at clock pos-edge and gets locked for the cycle, following this the preset pulse triggers spin-mode evaluation in the neurons based on input currents received in the present cycle.

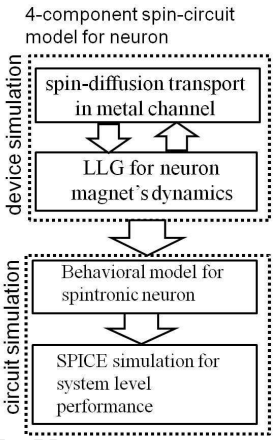


Fig. 7 Device-circuit co-simulation framework employed in this work

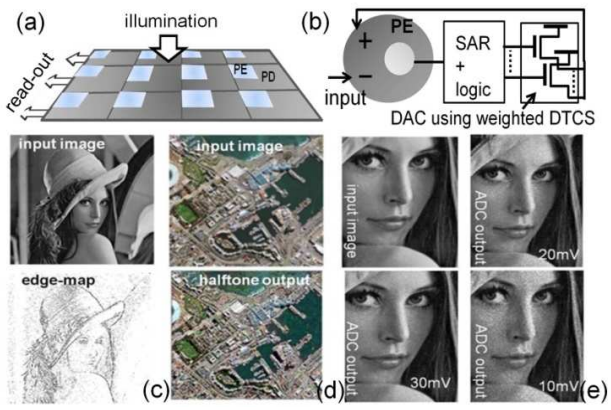


Fig. 8 (a) On sensor image processing architecture (b) SAR-ADC using spintronic neuron, and simulation results for (c) edge-detection, (d) half-toning, and (e) digitization (using spin-CMOS hybrid SAR-ADC : lowering ΔV increases % noise and hence degrades accuracy)

Table-I : Computation energy for 256x256 array

application	E_{comp} per-frame (avg.)	E_{comp} per-frame (avg.)	Power (10K Frames/ sec)
SAR ADC(8-b)	14nJ	8nJ	220μW
edge detection	4nJ	1nJ	50μW
half-toning	6nJ	1nJ	70μW

Table-II. CMOS vs. spin based feature detection IC

Ref	CMOS tech.	FOMR
[14]	0.35μ	253
[15]	0.35μ	560
[16]	0.25μ	470

Table-III. CMOS vs. spin based ADC

Ref	CMOS tech.	FOMR
[17]	0.18μ	133
[18]	0.90n	70
[19]	0.90n	72

FOM: S^2x(#PExF$_{ps}$)/(power) S: technology scale ratio
FOMR: FOM(spin)/FOM(ref)

Fig. 9. For the proposed design, E_{comp} is comparable to E_{read} .Table-2,3 provide the FOM ratio of the proposed design to the referred CMOS designs. FOM is based on computation energy per-frame, per-PE.

Rump Sessions

Tuesday PM, June 19th, 2012

8:30 PM (Penn Stater)
Wells vs. Sheets vs. Tubes

Session Organizers:
Joshua Robinson, Penn State
Debdeep Jena, University of Notre Dame

Panelists:
TBA

In the device (and materials) community there is an ever-increasing push for speed, power, and sensitivity. To meet this challenge, advances in materials and devices have led to novel, antimonide-based and nitride-based III-V semiconductor quantum well designs. The discovery of carbon nanotubes, graphene, and other semiconducting 2D crystals have lead to an explosion of device R&D that utilize low dimensional material systems to achieve the above challenges. These breakthroughs have opened up the possibility of exploring the fascinating properties of novel devices.

But scientists and engineers have made claims that each are the ideal candidate in multiple applications. In spite of excellent progress in nanofabrication techniques during the last decade, the scientific community has yet to reach a consensus the full potential of graphene and CNTs, leading to the questions:

- Where can the low dimensional carbon material systems out-perform their QW counterparts?
- In which applications are the claims of superior performance of QWs, graphene, or CNTs most appropriate?

Answering these questions and more will be the focus of the rump session.

8:30 PM (Penn Stater)
Compound semiconductors on Si: "A Happy Marriage" or "Keep Your Filthy Materials Out Of My Fab"?

Session Organizers:
Seth Bank, The University of Texas at Austin
Yanning Sun, IBM

Panelists:
TBA

While silicon is still the undisputed champion of the microelectronics world, performance and capabilities are still limited. Intrinsic material parameters offer an interesting set of tradeoffs (e.g. mobility vs. density of states) and compound semiconductors could offer the "best junction for the function." Compound semiconductors can also provide efficient light emitters not possible for silicon, and the potential for photonic integrated circuits. The integration of compound semiconductors on silicon has been proposed for decades, but there have been recent demonstrations of high-performance transistors, modest scale integrated circuits, and diode lasers based on compound semiconductors on silicon. Are compound semiconductor devices on silicon becoming a new universal reality, or will it remain a set of laboratory demonstrations and niche products?

(Dean's Hall I & II**)**

Plenary Session

Wednesday AM, June 20th, 2012

Joint DRC/EMC Plenary Session

8:20 AM Awards Ceremony

8:30 AM Plenary Paper
Nonpolar and Semipolar GaN Materials and Devices: The Journey So Far
James S. Speck, University of California, Santa Barbara

9:20 AM Break

Session VI.A (Dean's Hall I)

Transistor Modeling

Wednesday AM, June 20th, 2012

Session Chair(s): Siyu Koswatta, IBM and Avik Ghosh, University of Virginia

10:00 AM VI.A-1 Invited Paper
Dissipative Quantum Transport in Nanoscale Transistors
J. Guo, Department of ECE, University of Florida, Gainesville, Florida, USA

10:40 AM VI.A-2
Will Strong Quantum Confinement Effect Limit Low VCC Logic Application of III-V FINFETs?
A.Nidhi[1], V.Saripalli[1], V. Narayanan[1], Y. Kimura[2], R. Arghavani[2] and S. Datta[1], [1]The Pennsylvania State University, University Park, Pennsylvania, USA and [2]Lam Research, California, USA

11:00 AM VI.A-3
Exploration of Vertical MOSFET and Tunnel FET Device Architecture for Sub 10nm Node Applications
H. Liu, D. K. Mohata, A. Nidhi, V. Saripalli, V. Narayanan and S. Datta, The Pennsylvania State University, University Park, Pennsylvania, USA

11:20 AM VI.A-4
Late News

11:40 AM VI.A-5
Late News

Dissipative Quantum Transport in Nanoscale Transistors

Jing Guo
Department of ECE, University of Florida, Gainesville, FL, 32661

Abstract: We review our efforts on using numerical simulations to study essential physics of dissipative quantum transport in nanoscale field-effect transistors (FETs). Three types of nanoscale transistors are modeled as examples, (i) graphene nanoribbon (GNR) FETs with a quasi-one-dimensional (1D) channel, (ii) graphene FETs with a two-dimensional channel, and (iii) tunneling FETs with a strained GNR channel. In a quasi-1D channel, inelastic phonon scattering can increase the ballisticity at high drain biases considerably and partly offset the negative effect due to elastic scattering. Interplay between dissipative scattering processes and quantum phenomena, such as Klein tunneling in a graphene FET and band-to-band tunneling in a tunneling FET, play an important role on device characteristics. Coupling between far-from-equilibrium phonons and electrons and transport in the strong electron-phonon coupling regime remain as issues for further study.

Approach: The non-equilibrium Green's function (NEGF) method [1] is used in order to capture contact effects and Klein or band-to-band tunneling processes in nanoscale transistors. Electron-phonon interaction is treated within the self-consistent born approximation (SCBA), which captures the scattering process between and within the 1D modes. Parallel simulation codes have been developed to speed up the simulation and enable simulation of devices with a size of experimental relevance.

Results and Discussions: Figure 1 shows the simulated current spectrum in a GNRFET[2]. Figure 2 shows that in the absence of other scattering mechanisms, elastic scattering due to edge roughness has a large effect on the source-drain current of a GNR field-effect transistor due to its quasi-one-dimensional channel. In the presence of optical phonon scattering, the effect of elastic scattering is reduced. The coupling of inelastic, short mean free path optical phonon scattering to elastic scattering results in an increase rather than a decrease of the source-drain current[2, 3].

Figure 3 shows that that with local strain applied at the tunneling junction between the source and the channel in a GNR tunneling FET, the on-current can be significantly improved by over a factor of 10 with the same off-current, no matter at the ballistic limit or in the presence of inelastic phonon scattering[4]. Inelastic scattering degrades the subthreshold slope of a tunneling FET [5].

For graphene FETs, figure 4 shows that reducing the phonon energy degrades the ballisticity rapidly. High ballisticity at low drain bias and low ballisticity at high drain bias is observed in Fig. 5(b), and the dependency is more significant when the phonon energy is larger. This feature is qualitatively different from conventional MOSFETs and the GNRFET discussed above due to the interplay of Klein tunneling and scattering processes [6].

Acknowledgment: This work is supported by NSF and ONR.

References: [1] S. Datta, *Quantum Transport: Atom to Transistor*, Cambridge University Press (2005). [2] Y. Ouyang et al., *Appl. Phys. Lett*., 92, p. 243124 (2008). [3] Y. Yoon et al., *Appl. Phys. Lett*., 98, p. 204503 (2011). [4] Y. Lu et al., *Appl. Phys. Lett*. 97, p. 073105 (2010). [5] Koswatta et al., *Nano Lett*., 7, p. 1160 (2007). [6] Y. Lu et al., *IEDM Tech. Dig*., p. 263 (2011).

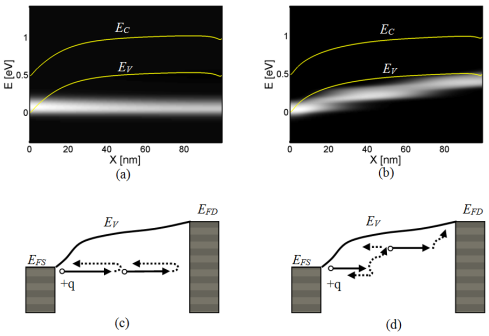


Fig. 1. Scattering in a GNRFET: The simulated local current spectrum as a function of the position and energy in the presence of (a) only elastic scattering and (b) both elastic scattering and OP scattering at V_D=-0.5V. The schematic sketches that explain carrier scattering process in the presence of (c) only elastic scattering and (d) both elastic scattering and OP scattering. The arrows indicate the direction of the hole flow.

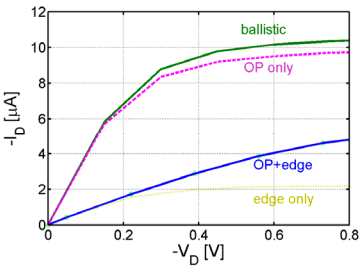


Fig.2 The I_D vs. V_D characteristics at the ballistic limit (solid line), and with scattering in a GNRFET.

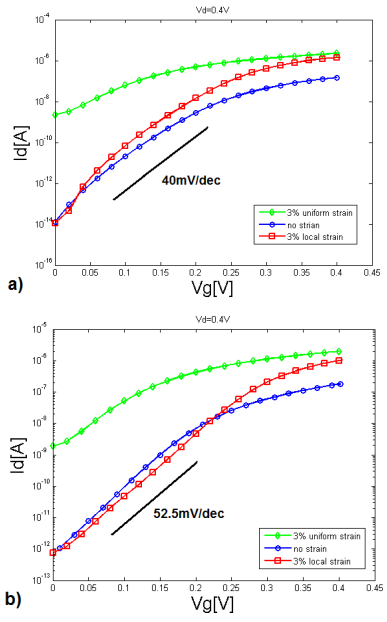


Fig. 3 A tunneling FET with a strained GNR channel: I_d versus V_g characteristics (a) in the ballistic limit and (b) in the presence of phonon scattering at V_d=0.4V for the GNR tunneling FET without strain (lines with circles), with 3% uniform strain throughout the source, channel, and drain regions (lines with diamonds), and with a local strain applied to the tunneling junction (lines with squares). A line with a subthreshold swing of 40mV/dec or 52.5mV/dec is plotted in (a) or (b), respectively, for reference.

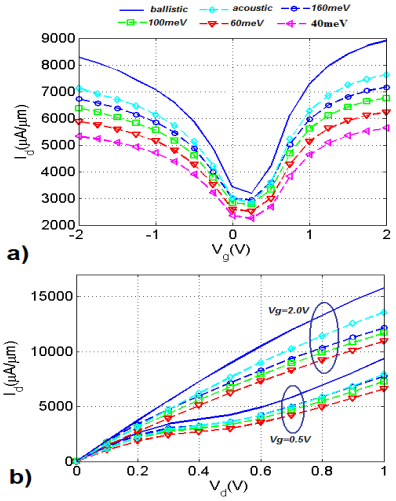


Fig.4 *I-V* characteristics of a graphene FET. a) I_d versus V_g with different phonon energy, V_d =0.5V. The curve in ballistic condition is added as a reference. As shown in the figure, low energy phonons degrade the current more compared to high energy phonons. b) I_d versus V_d for different phonon energy.

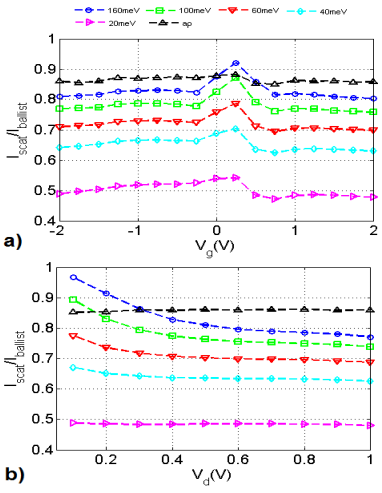


Fig.5 *DC Ballisticity as a function of terminal biases for a graphene FET.* a) V_g dependency at V_d =0.5V. b) V_d dependency at V_g =1.5V. For inelastic process, ballisticity decreases with a increasing drain voltage.

Will Strong Quantum Confinement Effect Limit Low V_{CC} Logic Application of III-V FINFETs?

A.Nidhi[1], V.Saripalli[1], V. Narayanan[1], Y. Kimura[2], R. Arghavani[2] and S. Datta[1]
[1]The Pennsylvania State University, University Park, PA 16802; [2]Lam Research, CA, USA

Introduction: FINFETs or Tri-Gate transistors have emerged as promising device architecture for 22nm node and beyond logic applications [1]. For sub-10nm node applications, high mobility III-V materials such as $In_{0.53}Ga_{0.47}As$ are under investigation to replace the Si channel in FINFETs to further enhance performance. The low electron effective mass results in strong quantum confinement effect in $In_{0.53}Ga_{0.47}As$ FINFETs, making them sensitive to fin width fluctuation and Fin Line Edge Roughness (LER) variation. Thus, it is imperative to quantify the sources of variation in $In_{0.53}Ga_{0.47}As$ FINFETs. In this work, we use self-consistent Schrodinger and Poisson equations to study the impact of Fin LER and L_G variations in Silicon and $In_{0.53}Ga_{0.47}As$ FINFETs. While the effect of quantum confinement makes $In_{0.53}Ga_{0.47}As$ FINFET more sensitive to Fin LER variation, the superior short channel effect in $In_{0.53}Ga_{0.47}As$ FINFETs make them less sensitive to L_G variations. The combined effect of Fin LER and L_G variations show that both Silicon and $In_{0.53}Ga_{0.47}As$ FINFETs experience the same level of variation at future technology node, with the latter still outperforming the former in terms of performance at lower supply voltage. We extend the device level variation to the circuit level by analyzing the read static noise margin (RSNM) variation of 100 Monte Carlo samples of 6T SRAM cells constructed with Si and $In_{0.53}Ga_{0.47}As$ FINFETs.

InGaAs FINFET device physics: A two-dimensional modified drift-diffusion TCAD framework is used for the simulations in this work. Fig. 1 shows the nominal device model and the physical and electrical parameters in Table 1 and 2 respectively. Drift-diffusion simulations using field-dependent mobility model (Caughey-Thomas [2]) have been calibrated and modified to include quasi-ballistic effects [3]. Fig. 2(a)-(b) depicts the transport properties of Silicon and $In_{0.53}Ga_{0.47}As$ FINFET models and compares the extracted sheet charge density, n_s and the effective velocity, v_{eff} of both the devices. At $0.5V_{CC}$, n_s of Si is 2 times higher while v_{eff} is about 4 times lower than that of $In_{0.53}Ga_{0.47}As$. The Id-Vg curves for 15nm L_G Si and $In_{0.53}Ga_{0.47}As$ FINFET are shown in Fig. 2(c). Fig. 2(c) also shows the percentage improvement in I_{ON} of $In_{0.53}Ga_{0.47}As$ with respect to Si FINFET. At $0.5V_{CC}$, we get 80% improvement in I_{ON} of $In_{0.53}Ga_{0.47}As$ over Si because of the higher effective velocity. Fig. 3(a) shows the quantum confinement effect in both the materials. $In_{0.53}Ga_{0.47}As$ being a low mass system experiences stronger confinement effects than Si. It can be seen from Fig. 3(a) that the 1st three subbands of Si participate in the transport while in $In_{0.53}Ga_{0.47}As$, the contribution comes from only the 1stsubband. The better electrostatics observed in $In_{0.53}Ga_{0.47}As$ is because of the lower S/D doping than Si (Table1) which, in turn, provides higher effective channel length (Fig.3(b)).

InGaAs FINFET variation study: Fig. 4 shows the algorithm used for LER implementation in the nominal double gate FINFET devices. Gaussian power spectral density (PSD) with RMS amplitude (Δ) of 2nm and correlation length (Λ) of 20nm is assumed for both Silicon and $In_{0.53}Ga_{0.47}As$ [4]. Apart from the Fin LER we have also included L_G variation effects (Gaussian distribution) in both the devices. Ensembles of 100 devices for each variation - Fin LER, L_G and Fin LER+L_G - are studied. Variation due to channel dopant fluctuation is ignored due to intrinsic channel doping employed in these devices. To quantify the variation impact on the electrical parameters, we performed a sensitivity analysis for Fin width (W_{FIN}) variation (without Fin LER) and L_G variation shown in Fig. 5. All the parameters show linear dependence on W_{FIN} and L_G variations. The normalized sensitivity numbers of the device parameters are given in Fig. 5. Fig. 6(a)-(c) shows the histograms of the electrical parameters of all these variant devices. Fig. 6(d) shows the σV_T for all the three cases. $In_{0.53}Ga_{0.47}As$ shows 2.3x higher σV_T for Fin LER, 2.1x lower σV_T for L_G and similar σV_T for Fin LER+L_G variations than Si. Fig. 6(e) shows the variation in the electrical transfer characteristics of both the devices with these variations. We also studied the impact of variation on the static read noise margin of the 6T SRAM cells implemented with Si and $In_{0.53}Ga_{0.47}As$ FINFETs. A cell ratio of 2 is chosen for the storage cells. Fig. 7(a) shows the best, nominal and worst case Read SNM values of Si and $In_{0.53}Ga_{0.47}As$ FINFET based SRAM cells at 300K. Fig. 7(b) shows histogram of the Read SNM values of a population of 100 6T SRAM cells with the same σRSNM (~18mV) obtained for both the devices. This implies that the variation impact on the stability of the SRAM arrays in III-V FINFETs is no worse than Si FINFETs.

Conclusion: We compared the impact of Fin LER and Lg variations in Si and $In_{0.53}Ga_{0.47}As$ FINFETs, for the first time. Better electrostatics in $In_{0.53}Ga_{0.47}As$ than in Si, due to higher effective channel length from lower SD doping in $In_{0.53}Ga_{0.47}As$, reduces Lg variation impact. Strong quantum confinement effects in $In_{0.53}Ga_{0.47}As$ FINFET make them more sensitive to Fin LER variation than Si. However, the lower sensitivity to L_G variation in $In_{0.53}Ga_{0.47}As$ FINFETs compensates for the increased variation from quantum confinement effect. Interestingly, by considering both Fin LER and L_G variations, both devices show similar sensitivity to variation. We conclude that tighter control of Fin LER in $In_{0.53}Ga_{0.47}As$ together with improved short channel immunity will make III-VFINFETs a promising device for 0.5V and below logic applications.

[1] Intel Press Release May, 2011 [2] Caughey & Thomas, Proc. of IEEE, 1967 [3] J.D.Bude, SISPAD 2000 [4] A.Asenov et al, IEEE TED 2003

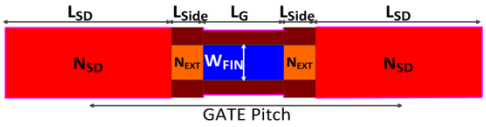


Table1: Physical Parameters of Simulation Model

Physical Parameters	Silicon	$In_{0.53}Ga_{0.47}As$
Gate Length, L_G(nm)	15	15
Fin Width, W_{FIN}(nm)	8	8
T_{OXEq}(nm)	0.7	0.7
GATE Pitch (nm)	50	50
SD Lengh, L_{SD}(nm)	25	28
L_{Side}(nm)	5	2
N_{SD}(cm^{-3})	**1e20**	**4e19**
N_{EXT}(cm^{-3})	**4e19**	**1e19**

Table2: Electrical Parameters of Simulation Model

Electrical Parameters	Silicon	$In_{0.53}Ga_{0.47}As$
I_{ON}(μA/μm)	380	690
I_{OFF}(nA/μm)	100	100
V_{TLin}(mV)	263	246
V_{TSat}(mV)	190	189
DIBL(mV)	162	125
SS(mV/dec)	84	82

Fig. 1: Physical and electrical parameters of the Nominal 2D device model. Lower SD doping in $In_{0.53}Ga_{0.47}As$ gives higher L_{eff} than Si (L_{SD} and L_{Side} adjusted to keep the Gate Pitch constant)

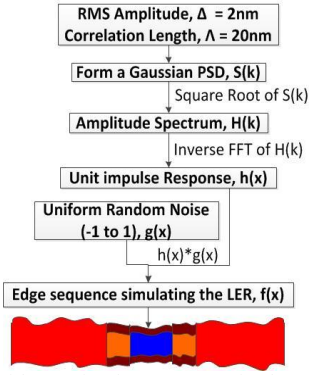


Fig. 4: Algorithm to implement LER in the 2D device model. Gaussian PSD with rms amplitude 2nm and correlation length 20nm is assumed for FinLER[4]. Gaussian distribution of 2nm rms amp. is assumed for L_G

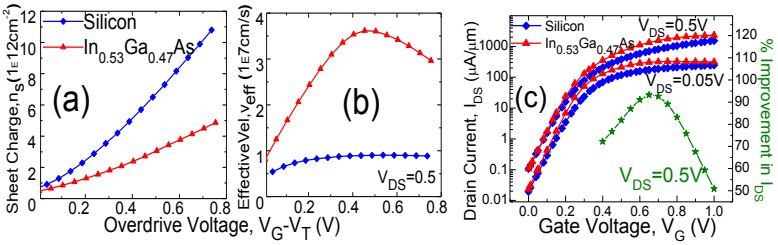


Fig. 2: (a) Sheet Charge density, n_s and (b) effective velocity, v_{eff} comparison. n_s of Si is twice of $In_{0.53}Ga_{0.47}As$ while v_{eff} of $In_{0.53}Ga_{0.47}As$ is 4 times of Si at V_{CC} of 0.5V, (c) IdVg characteristics of the 15nm Nominal device. At V_{CC} 0.5, $In_{0.53}Ga_{0.47}As$ gives 80% improvement in ON current because of higher veff.

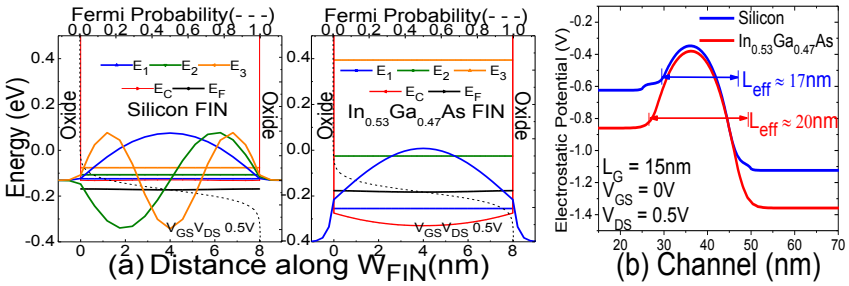


Fig 3: (a) Schrodinger-Poisson model used to capture Quantum Confinement & subband formation. At V_{GS} &V_{DS} 0.5V first 3 and 1st subband in Si and $In_{0.53}Ga_{0.47}As$ fins are occupied respectively. (b) Electrostatic Potential along the channel length shows higher effective channel length of $In_{0.53}Ga_{0.47}As$ than in Si.

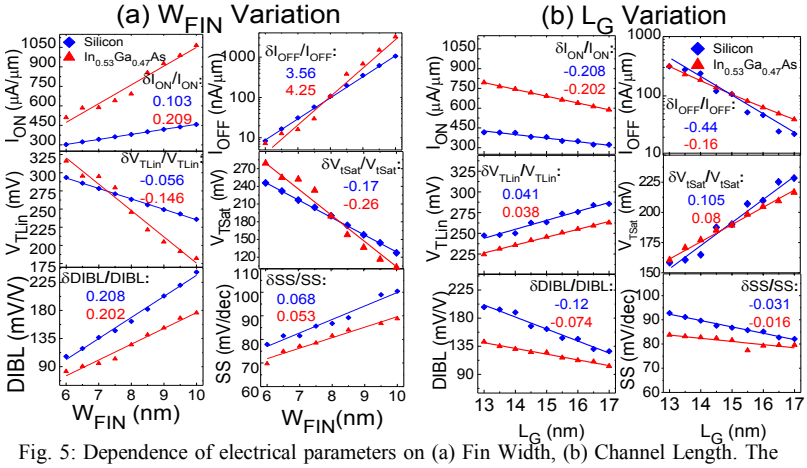


Fig. 5: Dependence of electrical parameters on (a) Fin Width, (b) Channel Length. The normalized sensitivity values are also given in the respective plots.

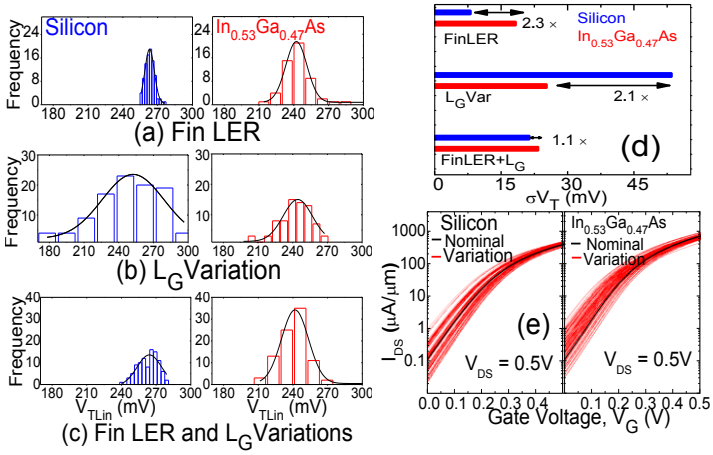


Fig. 6: Histograms of V_{TLin} of Monte Carlo samples each with (a)Fin LER, (b) L_G, (c) Both Fin LER and L_G variations (d) sigma V_T for all the three cases, (e) Variation in Id-Vg of Si and $In_{0.53}Ga_{0.47}As$. Interestingly, including both the variations gives similar sigma V_T in the two devices. This is because the lower sensitivity to L_G variation in $In_{0.53}Ga_{0.47}As$ FINFETs (2.1x) compensates for the increased variation from quantum confinement effect due to Fin LER (2.3x).

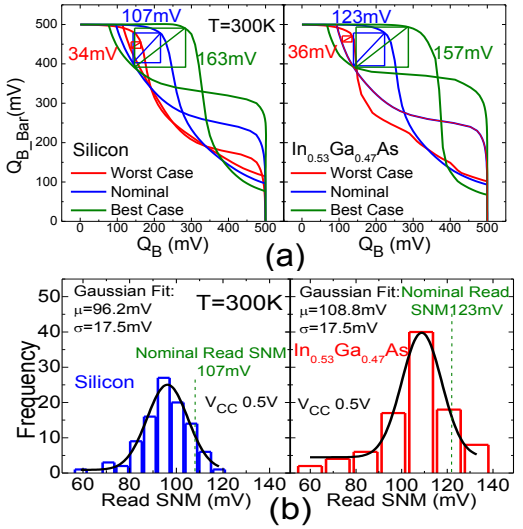


Fig.7:(a)Comparison of Read SNM of best, nominal and worst case 6T SRAM cell at 300K. (b) Histogram of RSNM. Sigma V_T due to variation of both Fin LER and L_G are same giving similar sigma of RSNM for both the devices.

Exploration of Vertical MOSFET and Tunnel FET Device Architecture for Sub 10nm Node Applications

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Introduction: With growing challenges in maintaining physical gate-length (L_g) scaling and device performance tradeoff, extending the technology roadmap with lateral devices to sub-10 nm technology node with 37nm contacted gate-pitch (L_{pitch}) is becoming increasingly difficult.[1] At or beyond this point, vertical device architecture can bring in new perspectives with regards to increasing device density and improving performance[2], simultaneously. Because vertical devices use side-gates which can be contacted outside the active region (Fig. 1), the contacted gate area can be reduced, resulting in ~40% density gain over lateral devices. However, vertical configuration brings additional gate-dielectric overlap for the gate, requires bottom source (or drain) extensions and metal plugs for the contacts, all of which increase the device parasitic elements. In this abstract, a double-gate vertical device architecture has been evaluated using TCAD simulations. Besides showing the area advantage, parasitics included energy efficiency and switching performance of vertical n-channel MOSFET and n-type Hetero-junction Tunnel FET (N-HTFET) are systematically compared for low operating power (LOP) logic applications. L_{pitch} of 37nm is used to target sub-10nm technology node, while L_g of 16nm is used to maintain short channel effects.

Vertical FET Physical Layout: The cascaded inverter layouts using planar CMOS, FinFETs and vertical FETs are shown in Fig. 1. The vertical FETs have source terminals connected at the bottom and eventually to the surface with metal plugs. The source region is recessed down to reduce the gate-to-source capacitance. FinFET inverters exhibit similar area as planar CMOS (10F×W), while the vertical FETs show ~40% area reduction (Table I).

Vertical FET Parasitics: For the evaluation of the parasitic components, the base structure of shared bottom-source is used as shown in Fig. 2(a). The device spacing (L_{pitch}) is 37nm. The total gate fringe capacitance $C_{g,fringe}$ comprises of side-gate to plug, side-gate to drain extension and side-gate to source extension capacitance due to fringe field through the low-k dielectric spacer. The total overlap capacitance, C_{ov} includes gate to source/drain overlap of 1 nm. The lateral gate-oxide extension ($L_{ox,ext}$) induced $C_{ox,ext}$ becomes part of $C_{g,fringe}$ because of the recess and low-k filling. Vertical HTFET and Si NMOS I_{DS}-V_{GS} characteristics are compared in Fig. 2(b). Minimum sub-threshold slope of 30mV is achieved in HTFET. With off-state current I_{OFF} <5nA/μm (LOP target) at V_{GS}=0V, on-state current I_{ON} of 403μA/μm and 397μA/um at V_{DD}=0.5V are obtained in vertical Si NMOS and III-V HTFET, respectively. Fig. 3 provides the parasitic extraction methods with small-signal simulation using vertical Si NMOS as an example. $C_{g,fringe}$ of 0.15fF/μm is extracted from ϵ_{ILD} variation. C_{ov} of 0.213fF/μm is obtained from $C_{g,total}$-$C_{g,fringe}$ extrapolation at $L_{g,eff}$=0nm. $C_{ox,ext}$ of 0.047fF/μm is extracted from $L_{ox,ext}$ variation on the 1st order estimation. The extension series resistance ($R_{SD,ext}$) of 35Ω-μm is extracted from Z parameter analysis.[3] $R_{S,plug}$ is below 0.5Ω-μm for plug height of 28nm with tungsten. Similar evaluations are performed for both Si NMOS and III-V HTFET at V_{DD}=0.3V and 0.5V.

Vertical FET Energy-Performance: As shown in Fig. 4, $C_{g,total}$ of III-V HTFET is dominated by C_{gd} at high V_{GS}, mainly due to the enhanced Miller capacitance.[4] When V_{GS} increases from 0 to V_{DD}, HTFETs offers smaller $C_{g,total}$ compared to Si NMOS (Fig. 5) due to (i) the lower density of states electron mass of III-V and (ii) the required lower drain doping to prevent ambipolar conduction, which also results in C_{ov} reduction, however with a penalty of increased $R_{D,ext}$. Fig. 6 shows the parasitic capacitance components comparison between HTFET and Si NMOS at different V_{DD}. $C_{g,fringe}$ is similar for both Si NMOS and III-V HTFET. Despite lower I_{ON}, the low $C_{g,total}$ in HTFET offers advantage in energy and delay reduction. Table III shows the device performance comparison. At V_{DD}=0.5V, intrinsic delay ($\tau_{intrinsic}$= $C_{g,total}$ × V_{DD}/I_{ON}) of 0.438ps for III-V HTFET and 0.714ps for Si NMOS can be obtained. Energy-delay figure of merit is then evaluated for FO1 (fan-out=1) inverter assuming symmetric PMOS performance with Miller effect considered (Fig.7). Si NMOS can achieve 1ps delay at V_{DD} >0.6V, while HTFET has superior energy efficiency below 0.6V. Fig. 8 shows the cut-off frequency (F_T) versus DC power relationship, considering the parasitics. III-V HTFET presents further advantages for low-power analog applications. Since the contact resistance (R_{co}) dominates the series resistance beyond 32nm technology node [1], the analysis of R_{co} effect is important (Fig. 9). Considering R_{co} of 100Ω (resistivity of 10^{-8} Ω-cm^2) for 1×0.01μm^2 contact, HTFET and Si NMOS show ~26% and ~40% I_{ON} degradation at V_{DD}=0.5V, respectively. R_{co} requires further improvement to maintain the performance.

Conclusions: A vertical device architecture having ~40% density improvement over planar for sub-10nm technology node has been evaluated for Si NMOS and III-V HTFET with L_g=16nm. For LOP applications including the effect of parasitic elements, the HTFET presents superior energy efficiency and desired low-power analog performance for V_{DD}<0.6V, while MOSFET is superior for V_{DD}>0.6V. To further improve MOSFET performance, I_{ON} needs to be improved with higher injection velocity materials (e.g. III-V). For delay reduction, the parasitic capacitances (C_{ov} and $C_{g,fringe}$) and contact resistance need to be further engineered for both MOSFETs and TFETs.

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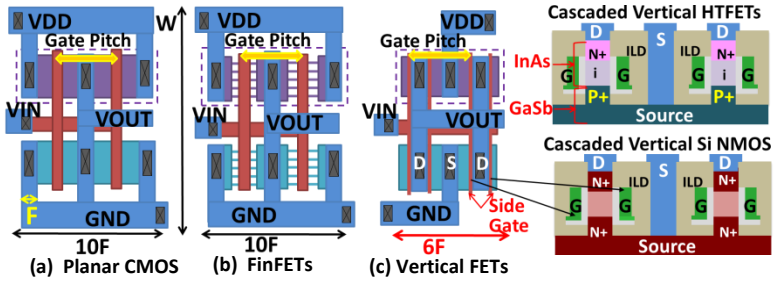

Fig. 1 Planar CMOS (a), FinFET (b) and vertical-FET (c) cascaded inverter layout example with illustrated gate-pitch and cascaded vertical NMOS and HTFETs cross-session. F is the minimum feature. The vertical FETs have reduced layout area.

Table I Normalized Area of Laterial/Vertical FETs

	Planar CMOS	FinFET	Vertical FET
Cascaded Inverter	100%	100%	~ 60%

Table II Parameters in Simulation Setup

L_{pitch}	37nm	L_{N+}	5nm
L_g	16nm	t_B	7nm
$L_{ox,ext}$	7nm	EOT	0.7
L_{ov}	1nm	t_G	5nm
L_{res}	5nm	$\varepsilon_{ILD}/\varepsilon_0$	2.3
$L_{s,ext}$	11nm	ρ_{gate}	5.64 Ω/□
L_{plug}	28nm	t_{plug}	8nm
Si NMOS S/D Doping		1e20 cm^{-3}	
N-HTFET Source Doping (GaSb)		2e17 cm^{-3}	
N-HTFET Drain Doping (InAs)		5e19 cm^{-3}	
For N-HTFET: $E_{g,GaSb}$=0.804eV, $E_{g,InAs}$=0.44eV, ΔEc=0.796eV			

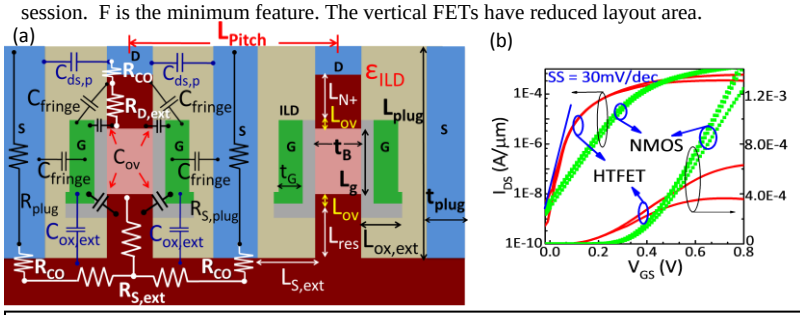

Fig. 2 (a) Simulated structure showing parasitic components. Lpitch=37nm for 10nm technology. (b) I_{DS}-V_{GS} at different V_{DS} of vertical Si NMOS and HTFET. I_{ON}=23 μA/μm, 403 μA/μm, 743 μA/μm for Si NMOS at V_{DD}=0.3V, 0.5V, 0.61V. I_{ON}=130 μA/μm, 398 μA/μm for HTFET at V_{DD}=0.3V, 0.5V.

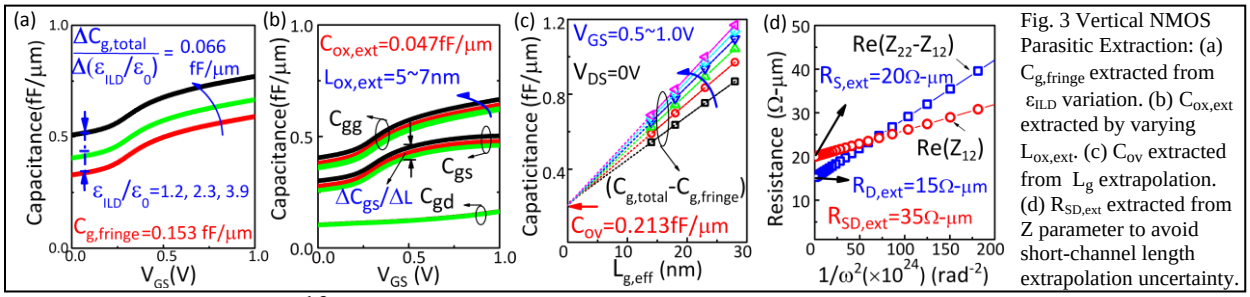

Fig. 3 Vertical NMOS Parasitic Extraction: (a) $C_{g,fringe}$ extracted from ε_{ILD} variation. (b) $C_{ox,ext}$ extracted by varying $L_{ox,ext}$. (c) C_{ov} extracted from L_g extrapolation. (d) $R_{SD,ext}$ extracted from Z parameter to avoid short-channel length extrapolation uncertainty.

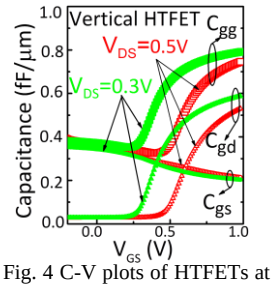

Fig. 4 C-V plots of HTFETs at V_{DS} = 0.3V, 0.5V. At low V_{GS}, C_{gg} is dominant by C_{gs}. As V_{GS} increases, C_{gd} dominates as on-state enhanced C_{miller}.

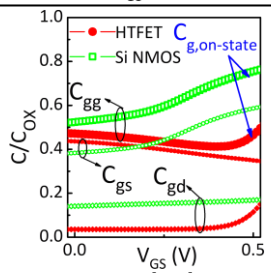

Fig. 5 Normalized capacitance comparison of vertical NMOS and HTFET at V_{DD}=0.5V. Lower C_g in HTFET comes from lower drain doping.

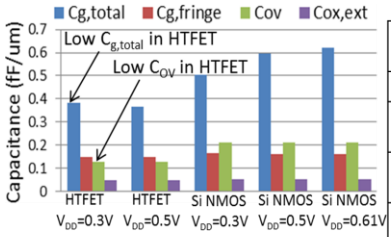

Fig. 6 $C_{g,total}$ and parasitic capacitance comparison of vertical HTFET and Si NMOS. HTFET presents lower $C_{g,total}$ and reduced C_{ov} compared to Si NMOS.

Table III Performance Comparison

	Vertical HTFET	Vertical NMOS
V_{DD} (V)	0.5	0.5
$C_{g,total}$ (fF/μm)	0.367	0.595
$C_{g,fringe}$ (fF/μm)	0.148	0.153
I_{OFF} (nA/μm)	5	5
I_{ON} (μA/μm)	398	403
$R_{SD,ext}$ (Ω-μm)	52	35
τ intrinsic (ps)	0.438	0.714

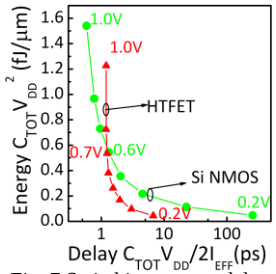

Fig. 7 Switching energy-delay for FO1 inverter using effective current (I_{EFF}) evaluation. Cross-over happens at V_{DD}=0.6V for NMOS. HTFET shows lower power advantage below 0.6V.

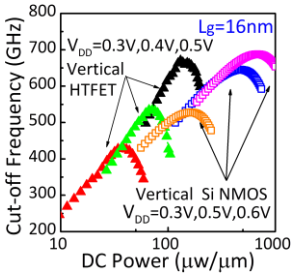

Fig. 8 F_T-DC power of vertical HTFET and Si NMOS of L_g=16nm. HTFET shows superior high frequency performance at low DC power.

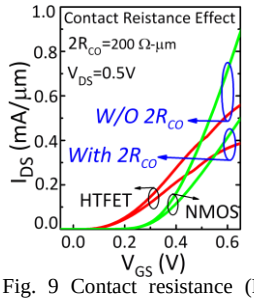

Fig. 9 Contact resistance (R_{CO}) effect on vertical HTFET and Si NMOS. HTFET shows lower current degradation (26%) with large R_{CO} than NMOS (40%) due to high tunneling resistance.

$$I_{EFF} = (I_H + I_L)/2$$

$$I_H = I_{DS}|(V_{GS} = V_{DD}, V_{DS} = 0.5V_{DD})$$

$$I_L = I_{DS}|(V_{DS} = V_{DD}, V_{GS} = 0.5V_{DD})$$

$$C_{TOT} = 2(C_{g,total} + C_{Miller})$$

$$C_{ox,ext} \approx \frac{\partial C_{gs,total}}{\partial L_{ox,ext}} L_{ox,ext}$$

$$C_{g,fringe} = \frac{\partial C_{g,total}}{\partial \epsilon_{ILD}} \epsilon_{ILD}$$

$$C_{ov} = \left(C_{g,total} - C_{g,fringe}\right)|_{L_{g,eff}=0}$$

$$R_{S,ext} = Re(Z_{12})|_{1/\omega^2=0}$$

$$R_{D,ext} = Re(Z_{22} - Z_{12})|_{1/\omega^2=0}$$

Session VI.B (Dean's Hall II)

Thin-Film Devices

Wednesday AM, June 20th, 2012

Session Chair(s): Jamie Phillips, University of Virginia and Yongtaek Hong, Seoul National University

10:00 AM VI.B-1 Invited Paper
Organic Thin-Film Transistors for Flexible Displays and Circuits
H. Klauk, Max Planck Institute for Solid State Research, Stuttgart, GERMANY

10:40 AM VI.B-2 Student Paper
Low-Voltage ZnO Double-Gate Thin Film Transistor Circuits
Y. V. Li[1,2], J. I. Ramirez[1,2], K. G. Sun[1,2] and T. N. Jackson[1,2], [1]Center for Thin Film Devices and Materials Research Institute and [2]Department of Electrical Engineering, Penn State University, University Park, Pennsylvania, USA

11:00 AM VI.B-3
High Performance Solution-Processed Thin-Film Transistors Based on In_2O_3 Nanocrystals
S. L. Swisher, S. Volkman, K. Braam, J. Jang, and V. Subramanian, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, California USA

11:20 AM VI.B-4
Characterization and Modeling of Metal-Insulator Transition (MIT) Based Tunnel Junctions
E. Freeman[1], A. Kar[1], N. Shukla[1], R. Misra[1], R. Engel-Herbert[1], D. Schlom[2], V. Gopalan[1], K. Rabe[3], and S.Datta[1], [1]Pennsylvania State University, Pennsylvania, USA, [2]Cornell University, Ithaca, New York, USA, and [3]Rutgers University, New Brunswick, New Jersey, USA

11:40 AM VI.B-5
Two-stage Model for Lifetime Prediction of Highly Stable Amorphous-Silicon Thin-Film Transistors under Low-Gate Field
T. Liu, S. Wagner and J. C. Sturm, Princeton Institute for the Science and Technology of Materials (PRISM), and Department of Electrical Engineering, Princeton University, Princeton, New Jersey, USA

Organic Thin-Film Transistors for Flexible Displays and Circuits

Hagen Klauk

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Unlike thin-film transistors (TFTs) based on hydrogenated amorphous silicon, polycrystalline silicon or metal oxides, which typically require process temperatures above 150 ºC, organic TFTs can often be fabricated at temperatures around 100 ºC or below and thus not only on glass or certain high-temperature-compatible types of plastics, such as polyimide or polyethersulfone, but also on less expensive plastics, such as polyethylene naphthalate (PEN) and polyethylene terephthalate (PET), and even on paper, making organic TFTs potentially useful for flexible active-matrix displays [1], flexible sensor arrays [2], and flexible integrated circuits [3].

Bulk carrier mobilities in organic semiconductor single-crystals measured by the time-of-flight technique can reach 30 cm^2/Vs at room temperature [4] and 100 cm^2/Vs at cryogenic temperatures [5]. Field-effect mobilities in organic TFTs are smaller, although they can reach (or even exceed) 10 cm^2/Vs for p-channel TFTs [6-8] and 1 cm^2/Vs (measured in air) for n-channel TFTs [9,10] (see also Fig. 1), provided the TFT channel length is sufficiently large (≥20 μm) to suppress the influence of the contact resistance on the effective mobility.

High-capacitance gate dielectrics (based on high-permittivity oxides, ultrathin insulators or polyelectrolytes) allow the realization of low-voltage (~1 to 5 V) organic TFTs that may be useful for portable, battery-powered applications. Field-effect mobilities in low-voltage organic TFTs are usually smaller by about a factor of two and can reach 6 cm^2/Vs in p-channel TFTs [11] and 0.5 cm^2/Vs in n-channel TFTs [12], with on/off ratios up to 10^8 and subthreshold swings as steep as 68 mV/decade on flexible plastic substrates [13].

The realization of integrated column drivers for active-matrix displays requires TFTs with a cutoff frequency of about 10 MHz, which in the case of organic TFTs implies lateral transistor dimensions (channel length, parasitic gate overlap) of 1 or 2 μm [14,15]. For such dimensions, the total device resistance will be strongly affected by the contact resistance, limiting the effective mobilities to about 1 cm^2/Vs in p-channel TFTs and 0.1 cm^2/Vs in n-channel TFTs. Nonetheless, by reducing the channel length to 1 or 2 μm, width-normalized transconductances up to 1 S/m in p-channel TFTs and up to 0.1 S/m in n-channel TFTs can be obtained (see Fig. 2), and the signal propagation delays measured in organic ring oscillators can be as short as 190 nsec per stage in unipolar (p-channel) ring oscillators [16] and as short as 30 μsec per stage in complementary ring oscillators [17]. A 6-bit digital-to-analog converter based on a current-steering design and organic p-channel TFTs with a channel length of 4 μm that operates with a sampling rate up to 100 kS/s has been reported [18].

The development of organic semiconductors with an inherent oxidation resistance has led to organic TFTs with greatly improved air stability [19] (see Fig. 3). A perhaps more serious issue is the bias-stress effect [20]. The amount by which the threshold voltage of low-voltage organic TFTs fabricated at a temperature of 100 °C on flexible plastic substrates is found to shift under continuous gate-bias stress is comparable to that observed in a-Si:H TFTs fabricated at 350 °C and metal oxide TFTs fabricated at 200 °C on glass substrates (see Fig. 4).

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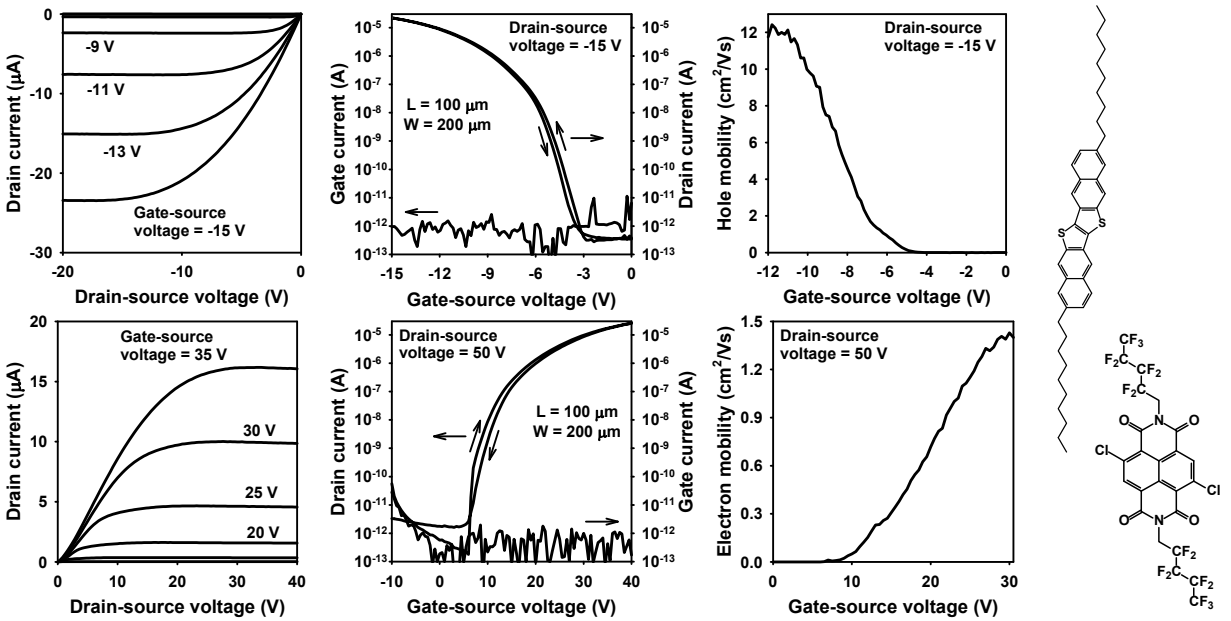


Fig. 1. Electrical characteristics of a p-channel TFT based on C_{10}-DNTT (top; see also ref. 7) and of an n-channel TFT based on NTCDI-Cl_2-$CH_2C_3F_7$ (bottom; see also ref. 9 and 12).

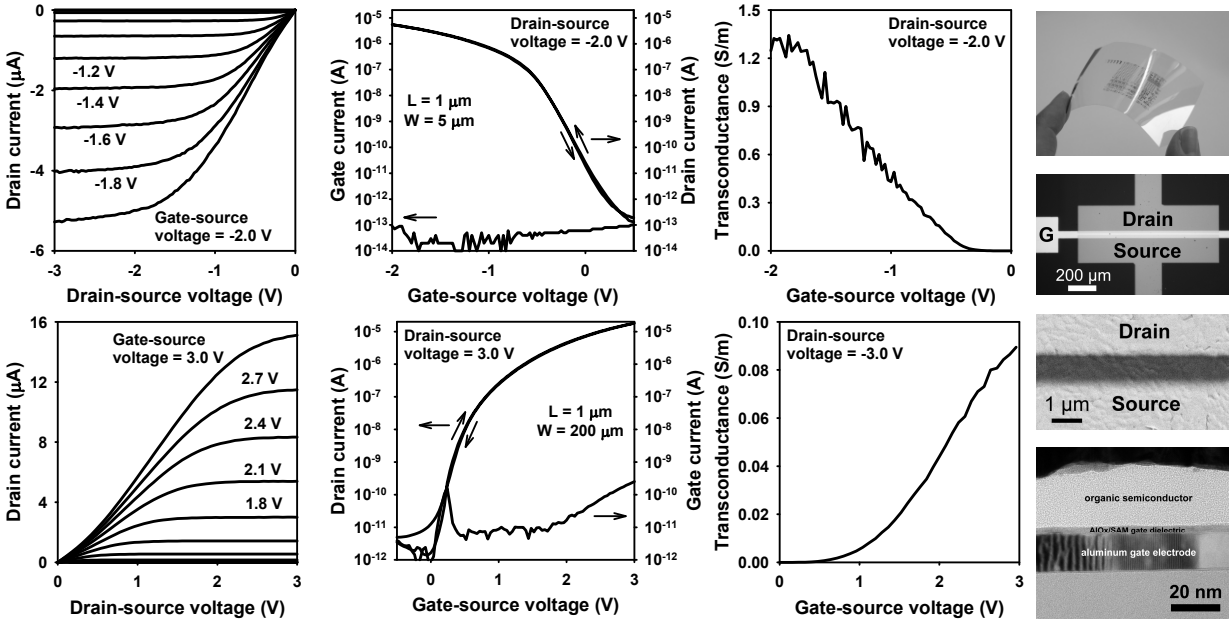


Fig. 2. Electrical characteristics of low-voltage organic TFTs with reduced gate-dielectric thickness (t_{diel} = 5.4 nm) and reduced channel length (L = 1 μm; see also ref. 15 and ref. 17).

Fig. 3. Shelf-life stability of p-channel organic TFTs based on two different organic semiconductors (top: DNTT; bottom: pentacene; see also ref. 19).

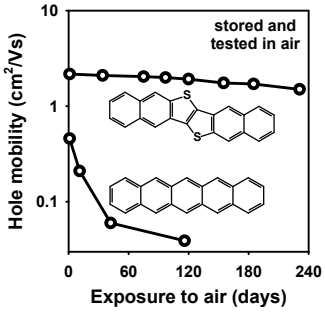
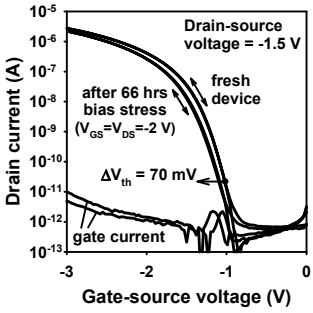


Fig. 4. Bias stress-induced threshold-voltage shift in a p-channel organic TFT fabricated on a flexible PEN substrate (see also ref. 19).



Low-Voltage ZnO Double-Gate Thin Film Transistor Circuits

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We report here double-gate ZnO thin film transistor (TFT) circuits with operation at low voltage. TFTs with low voltage operation have been reported previously, but often use very thin (few nm thick) gate dielectric which may limit manufacturability[1]. Oxide semiconductor-based TFTs have been extensively studied as competitive candidates for next-generation display technology and other large-area electronics. For many applications, operation at voltages compatible with low-voltage CMOS is important. Double-gate TFTs are of interest because they allow threshold voltage tuning, improved device performance, and circuit applications like mixers.[2,3] We have previously reported bottom-gate ZnO TFTs and circuits fabricated on glass and flexible polymeric substrates using plasma enhanced atomic layer deposition (PEALD)[4,5]. Here we report double-gate ZnO TFTs and circuits fabricated on glass substrates using PEALD with a maximum process temperature of 200 ˚C. Compared to bottom-gate ZnO TFTs, double-gate ZnO TFTs have higher mobility, and reduced substhreshold slope. In these devices, the top gate can be used to vary the bottom-gate threshold voltage by more than 4 V. This allows the logic transition point for circuits to be adjusted as desired and allows logic operation at low voltage. 15 stage double-gate ZnO TFT ring oscillators operate well with V_{DD} = 1.2 V, I_D = 32 μA, and propagation delay of 2.1 μs/stage.

Figure 1 shows a schematic cross-section of a double-gate ZnO TFT. To fabricate the devices, a 100 nm Cr layer was deposited on borosilicate glass by sputtering and patterned by wet etching to form the bottom gates. Next, 32 nm thick Al_2O_3 and 10 nm thick ZnO layers were deposited by PEALD and patterned by wet etching. Next, Ti source and drain contacts were deposited by sputtering and patterned by lift-off. An O_2 plasma step was used prior to Ti deposition to reduce contact resistance. Al_2O_3 (32 nm thick) deposited by ALD at 200 °C was used for the top-gate dielectric and patterned by wet etching. 100 nm thick Cr was deposited by sputtering and patterned by wet etching to form the top gates. Linear region I_D versus V_{GS} and I_D versus V_{DS} characteristics are shown in figure 1 for a TFT with L = 20 μm, W = 200 μm, $t_{oxbottom}$ = t_{oxtop} = 32 nm. Both bottom-gate with $V_{topgate}$ = 0 and top and bottom gates connected together device characteristics are shown in the figure. Bottom-gate operated TFTs have linear region mobility of 27 $cm^2/V{\cdot}s$; with top and bottom gates connected together the linear region mobility increases to 33 $cm^2/V{\cdot}s$. Figure 2 shows threshold voltage tuning of more than 4 V for bottom-gate TFT characteristics by varying the top-gate voltage from -3 V to 3V.

The schematic diagram and micrograph of a double-gate TFT inverter with L_{drive} = 5 μm, W_{drive} = 50 μm, L_{load} = 5 μm, W_{load} = 10 μm (β_{ratio} = 5) is shown in Figure 3. Top and bottom gates are connected together and to the source for the load TFT. The top gate of the drive TFT is varied to tune the bottom-gate TFT threshold voltage. Varying V_{TOP} from 3 V to -3 V shifts the logic transition from -3 V to 1 V, for V_{DD} = 5 V, also shown in figure 3. The maximum gain for this inverter is >100. 15-stage double-gate ZnO TFT ring oscillators using these inverters and a source/gate and drain/gate overlap of 2 μm oscillate at 15.9 kHz with a supply voltage of 1.2 V, I_{DD} = 32 μA, and top-gate voltage at -5 V, corresponding to a propagation delay of ~2.1 μsec/stage. Figure 4 shows a micrograph and the output signal of 15-stage ring oscillator. These results demonstrate that double-gate ZnO TFTs can provide circuits with improved gain and reduced voltage operation.

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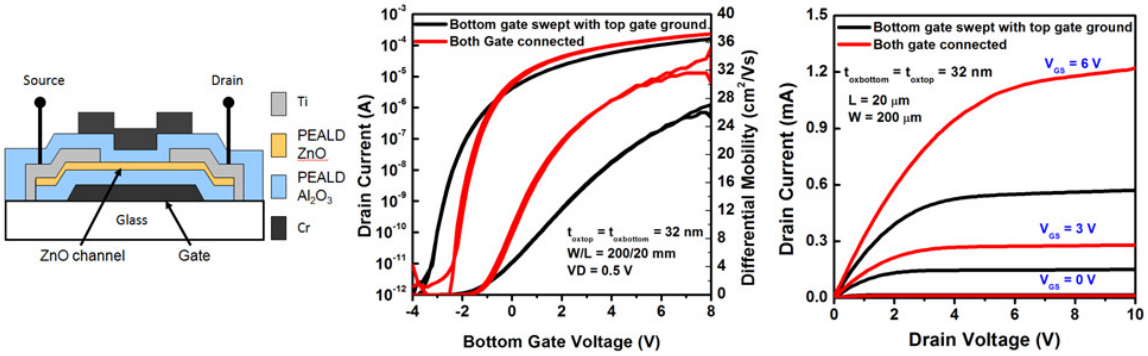

Fig. 1: (left) Double-gate TFT cross-section, (middle) linear region log(I_D) versus V_{GS} for double-gate TFT with $V_{GSbottom}$ varied and V_{GStop} = 0 V, and $V_{GSbottom}$ = V_{GStop} varied, (right) I_D versus V_{DS} for bottom-gate only varied and both gates connected and varied with V_G = 0, 3, 6 V (W/L = 200/20 µm, $t_{oxbottom}$ = t_{oxtop} =32 nm).

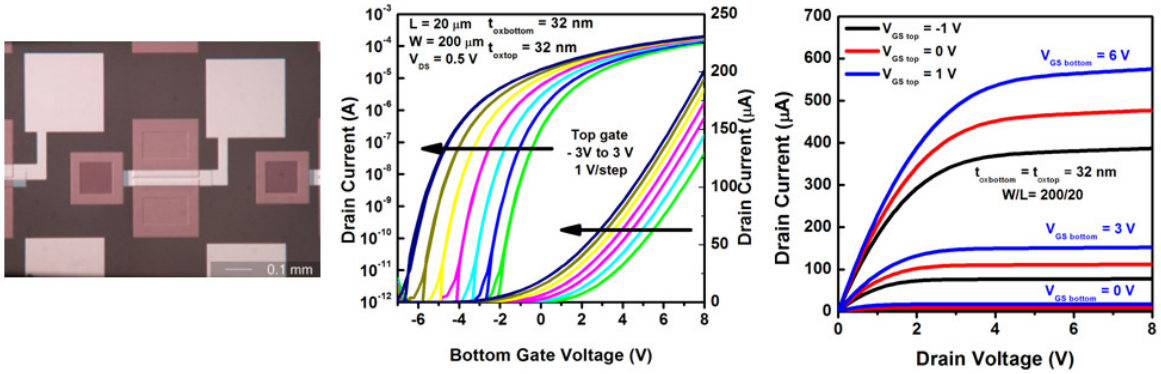

Fig. 2: (left) Microscope image of double-gate TFT, (middle) linear region log(I_D) versus $V_{GSbottom}$ with V_{GStop} = -3 to 3 V in 1 V steps, (right) I_D versus V_{DS} with $V_{GSbottom}$ = 3, 6, and 9 V and V_{GStop} = -1,0,1 V

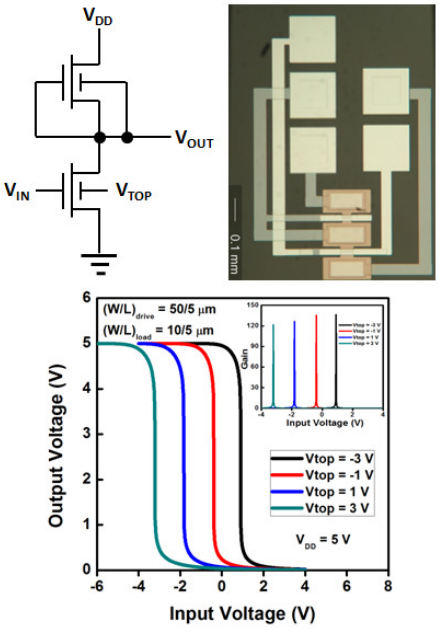

Fig. 3: (top) Double-gate inverter schematic diagram and microscope image of an inverter, (bottom) logic transition curve for an inverter with V_{DD} = 5 V at varies V_{TOP} = -3, -1, 1, 3 V (L_{drive} = L_{load} = 5 µm, W_{drive} = 50 µm, W_{load} = 10 µm, β_{ratio} = 5).

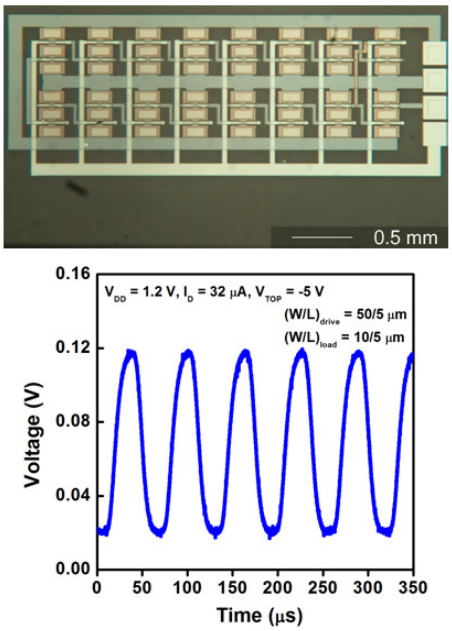

Fig. 4: (top) Microscope image of a 15-stage ring oscillator, (bottom) 15-stage ring oscillator output signal for V_{DD} = 1.2 V (L_{drive} = L_{load} = 5 µm, W_{drive} = 50 µm, W_{load} = 10 µm, β_{ratio} = 5, 2 µm source/gate and drain/gate overlap).

High Performance Solution-Processed Thin-Film Transistors Based on In_2O_3 Nanocrystals

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Metal-oxide semiconductors have received a great deal of focus in recent years as a means of realizing transparent electronics for next generation display applications; such materials are expected to enable the realization of transparent pixel transistors for display that do not block light, enabling realization of brighter displays with higher aperture ratio. In recent years, the demonstration of amorphous thin films of transition metal oxides with mobility an order of magnitude greater than that of amorphous silicon has resulted in dramatic interest and rapid advances in the field [1]. In particular, solution processable routes are considered particularly attractive since they may allow for low-cost fabrication techniques based on printing. There have been various reports of sol-gel based approaches to printable electronics based on these systems [2-4]; however, an approach utilizing colloidal semiconductor nanocrystals has several distinct advantages. First, the high temperature required for crystal nucleation and growth can occur during the synthesis phase, thus decoupling the high temperature crystallization step from the processing constraints of the substrate. Second, and possibly even more importantly, using nanocrystals as the starting point for inorganic semiconducting inks may provide better control over the stoichiometry of the material, more consistent film composition, and a pathway towards controlled doping of the channel material. Here we report a synthesis of indium oxide nanocrystals, and the fabrication conditions that result in high-performance TFTs based on the same.

We successfully synthesized soluble indium oxide nanocrystals utilizing a one-pot synthesis performed under argon atmosphere using standard air-free Schlenk line techniques. A solution of 1 mmol indium acetylacetonate and 40 mmol oleylamine was degassed at 70°C under vacuum for 30 minutes. The solution was then heated to 250°C under argon, and the reaction was allowed to proceed for 4 hours. After cooling, the flask was opened to air and 30 mL dichloromethane was added. The nanocrystals were precipitated by centrifugation with 120 mL ethanol. To remove excess surfactant, the particles were washed with ethanol and precipitated by centrifugation three times. Transmission electron micrographs (TEM) and the x-ray diffraction spectra (XRD) of the indium oxide nanocrystals synthesized for this work are shown in Figures 1 and 2, respectively. The particles are ~10 nm in diameter, and are easily dispersed in nonpolar organic solvents to form semiconductor inks.

Bottom-gate, top-contact TFT structures were fabricated utilizing the indium oxide nanocrystal solution as the channel material. For convenience and repeatability of testing, heavily doped silicon wafers with 100 nm thermally grown SiO_2 were used as the gate electrode and gate oxide, respectively. Indium oxide nanocrystals were spin-coated onto the SiO_2 at 5000 rpm for 60 seconds, followed by an oxygen anneal for 1 hour at 500°C; this temperature was selected to ensure compatibility with all major classes of display glass. The resulting In_2O_3 layer is ~ 60nm thick with surface roughness of 4 nm_{RMS}, measured by atomic force microscopy (AFM) and shown in Figure 3. Finally, aluminum source/drain electrodes (50 nm) were deposited by thermal evaporation through a shadow mask to produce TFTs with W/L = 200 um/40 um. All processing was performed in air.

Using the device structure illustrated schematically in Figure 4, we have achieved linear mobilities of 7 cm^2/Vsec, sub-threshold swing ~0.4 V/decade, and I_{ON}/I_{MIN} ratios of ~10^7 using SiO_2 as the gate dielectric (Figures 5-6). The mobility exhibited by these devices is among the highest reported in literature for solution-processed indium oxide on SiO_2. The devices operate in n-type depletion mode, with Vt ≈ -8V. It should be possible to alter the threshold voltage via control of oxygen vacancies through optimized annealing; this methodology, as well as the use of high-K dielectrics to reduce operating voltage has been widely used for these oxide systems. Note that the good swing and excellent saturation of the output characteristics attests the good electrostatic integrity of these devices and the excellent suppression of carriers in the off state, which is a critical requirement for display pixels to achieve fully saturated black pixels. The very high I_{on}/I_{min}, coupled with the high mobility and good swing thus make these excellent candidates for use as pixel transistors in both LCD and OLED applications.

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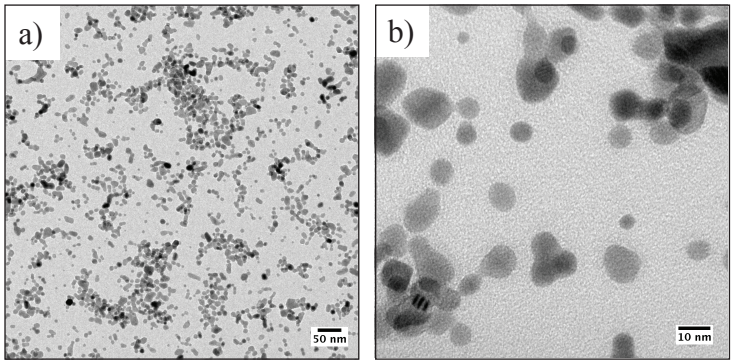

Fig. 1: TEM images of indium oxide nanocrystals, as synthesized. a) 15,000x and b) 97,000x magnification.

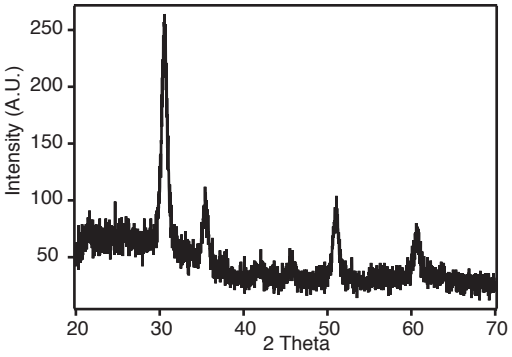

Fig. 2: XRD spectra obtained from indium oxide nanocrystals, as deposited.

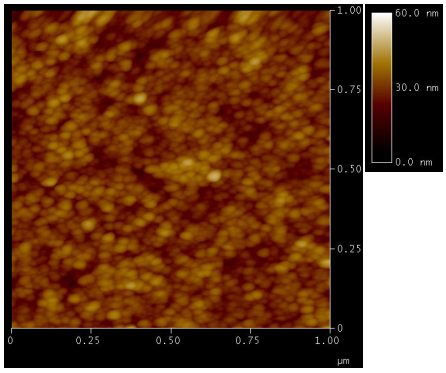

Fig. 3: AFM scan of the indium oxide film after spin-coating. Surface roughness = 4 nm_{RMS}.

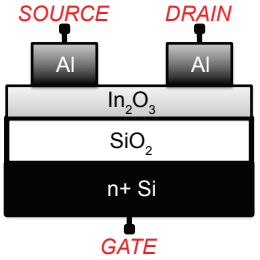

Fig. 4: Schematic cross-section of the TFT structure.

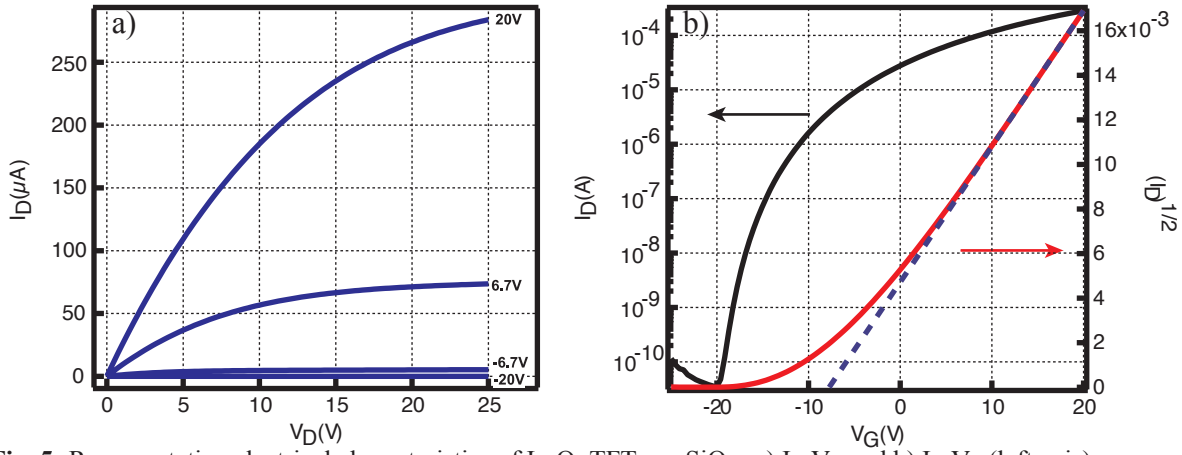

Fig. 5: Representative electrical characteristics of In_2O_3 TFTs on SiO_2. a) I_D-V_D and b) I_D-V_G (left axis) and sqrt(I_D)-V_G (right axis).

	μ_{LIN} [cm^2/Vsec]	μ_{SAT} [cm^2/Vsec]	Log (I_{ON}/I_{MIN})	Sub-threshold Swing [V/dec]
MEAN	6.30	4.37	5.53	0.78
STDEV	0.75	3.15	1.98	0.71
BEST	7.59	12.89	6.95	0.36

Fig. 6: Summary of indium oxide TFT parameters.

Characterization and Modeling of Metal-Insulator Transition (MIT) Based Tunnel Junctions

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Continued physical scaling will reduce power dissipation primarily through the reduction in device capacitance; however, a far greater benefit would result if the CMOS FET could be replaced by a fundamentally new device scheme that operates under very low supply voltages. Recently, semiconductor based inter-band tunnel field effect transistors (TFET) have been explored due to their potential to achieve sub k_BT/q steep switching swings, enabling low voltage operation [1]. In this work, we explore the abrupt metal to insulator transition (MIT) of vanadium dioxide (VO_2) based tunnel junction – a first step towards a correlated electron based steep switching TFET. As illustrated in Fig.1 the metal insulator transition MIT in materials with strong electron correlation can be utilized to modulate the tunnelling current by opening an energy gap around the Fermi level in the OFF-state, and a metal-insulator-metal tunnelling current by collapsing the gap in the ON-state.

Characterization of VO_2 Based MIT Tunnel Junctions:

Thermally and electrically induced MIT of ultrathin VO_2 films is shown in Fig.2. VO_2 films of 3.8 nm thickness were grown by MBE on $TiO_2(001)$ substrate. The MIT transition temperature shifted to lower values (T_{MIT}=300K) due to residual strain in the film. Two samples were fabricated: one with the the HfO_2 tunel barrier and one without it. The band diagrams for the fabricated devices are illustrated in Fig.3, where a Mott-Hubbard gap of 0.6 eV is expected to exist in the OFF-state [2]. The contact resistivity is extracted from CTLM pads, schematically shown in Fig.4. For VO_2 in the metallic state the contact resistivity $\rho_{tunnel}=2.2\text{x}10^{-4}$ Ω-cm^2 (R_{tunnel} = 11 Ω) and $\rho_{tunnel}=3.1\text{x}10^{-5}$ Ω-cm^2 (R_{tunnel} = 2.8 Ω) is extracted for devices with 1.6 nm ALD grown HfO_2 and no insulating barrier, respectively (Fig.5). Driving the device thermally across the MIT, the contact resistivities ρ_{tunnel} changed to $2.6\text{x}10^{-3}$ Ω-cm^2 (R_{tunnel} = 1097 Ω) and $7.63\text{x}10^{-3}$ Ω-cm^2 (R_{tunnel} = 850 Ω) with and without tunnel barrier, respectively. These order of magnitude changes in the electron transfer characteristics demonstrate the feasibility to realize tunnel junctions based on correlated electron materials. This corresponds to an on state tunnel conductance ratio of 3.55 taking into account differences in VO_2 sheet resistance. Fig.6 illustrates the simulated J-V curves of a Pd/HfO_2/VO_2 stack assuming metal-insulator-metal and metal-insulator-semiconductor structures for the ON and OFF states, respectively. Reasonable agreement with the experimental data is achieved.

Determination of Underlying Switching Mechanism in VO_2 Based MIT Tunnel Junctions:

The underlying physical origin of the coupled first order phase transition in VO_2 is still debated and is believed to be either a charge induced phase transition (Mott-Hubbard) or structurally driven (Peierls transition). Time dependent characteristics of the electric field induced MIT of VO_2/TiO_2 devices was studied to separate electric field driven (Mott-Hubbard) from temperature induced structural (Peierls) effects. The transient response (1 kHz) of the device is shown in Fig.7a. Further, frequency dependent switching experiments reveal that the MIT is irreversible at or beyond 20 kHz for the same applied voltage, and the MIT device doesn't reversibly switch off (Fig.7b). A delay time of 80-110 μs is observed in Fig.7a before the device transitions, albeit with considerable jitter. The current flow through the resistor is 2 mA and the volume of the device is $1.33\text{x}10^{-11}$ cm^3, therefore the number of carriers injected is approximately $7.5\text{x}10^{22}$-$9.4\text{x}10^{22}$ cm^{-3} as plotted in Fig.8. The carrier density needed to drive the semiconducting VO_2 into the metallic state is given by the Mott criterion $n_c \approx (0.25/\alpha_H)^3$ and $\alpha_H = \hbar^2\varepsilon/m^*q^2$ where $\hbar$ is the reduced Plancks constant, ε is the permittivity of VO_2 in the insulating state (ε ~40) and m* the electron effective mass (~4m_e) resulting in a critical carrier density n_c of $2.1\text{x}10^{23}$ cm^{-3} close to the value extracted from the measurement. Fig.8 shows a rise time (T_{Rise}) of 192 ns; this rise time is limited by the RC in the system and is not the intrinsic transition time of the MIT process in VO_2.

To further investigate the effect of joule heating we employed a 3D multiphysics finite element simulator (COMSOL) to perform heat transfer simulations using the actual device geometry. The increase in the steady state device temperature needed for switching was simulated for various heat pulse widths. The experimentally determined transition voltage and current of 15.21 V and 2.1 mA (OFF state) was used to estimate dissipated power density, yielding Q~$4.9\text{x}10^{14}$ W/m^3. Other constants for VO_2 used were density (4340 kg/m^3), specific heat capacity (690 J/K-kg), heat transfer coefficient (20 W/K-m^2) and thermal conductivity (6 W/K-m). The model is beyond a simple one-dimensional heat transfer model [3] and further takes heat dissipation into the contact and substrate into account. The equations and boundary conditions used are given in Table I. Fig.10 shows the simulated temperature distribution in an 8μm experimental device for various supply voltage pulse widths. In Fig.11 the simulated temperature-change (ΔT) in the VO_2 film of the 8μm experimental device is plotted as a function of pulse widths applied. It can be seen that the steady state ΔT achieved for the heat supplied is only 2.98K for a pulse width of 600 μs and ΔT saturates at ~2.9K for all pulse widths > 200 μs. It is also shown in Fig.11 that for an applied pulse width which equals to the field induced OFF to ON state switching time (T_{Rise}=192 ns), the ΔT is only 0.10K. Additionally, the steady state temperature change of ΔT=2.98K for longer pulse width durations is insufficient to cause a phase transition thermally. This suggests that the predominant switching mechanism in the MIT tunnel junction is likely due to charge filling of the conduction band and that Joule heating plays a negligible role in this transition.

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Conductance Modulation in MIT Tunnel Junction

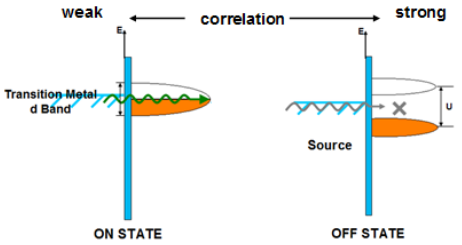


Fig. 1: Schematic band diagram of MIT material controlling tunneling in ON (metallic) and OFF (insulating) state.

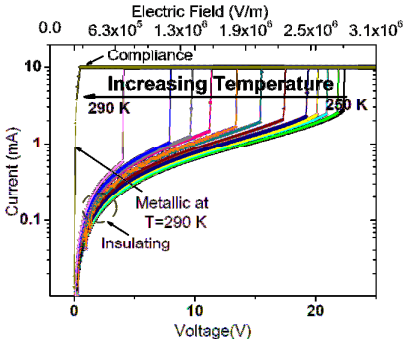


Fig. 2: Thermal and field induced transitions observed.

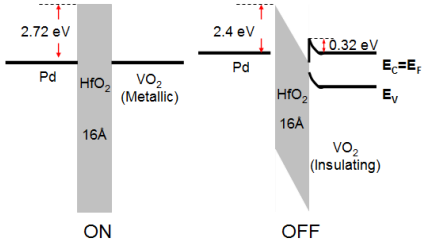


Fig. 3: Equilibrium energy band diagram of $Pd/HfO_2/VO_2$, in ON-state and OFF-state.

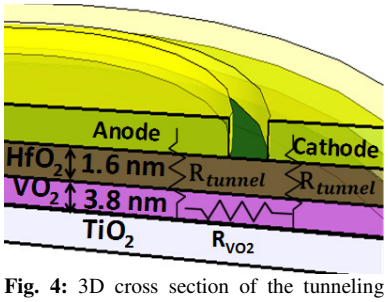


Fig. 4: 3D cross section of the tunneling structure. R_{Tunnel} refers to tunneling resistivity and R_{VO2} is the VO_2 sheet resistance.

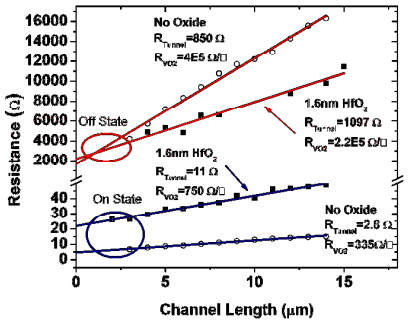


Fig. 5: CTLM data showing a change in contact resistance due to the presence of HfO_2 tunnel barrier.

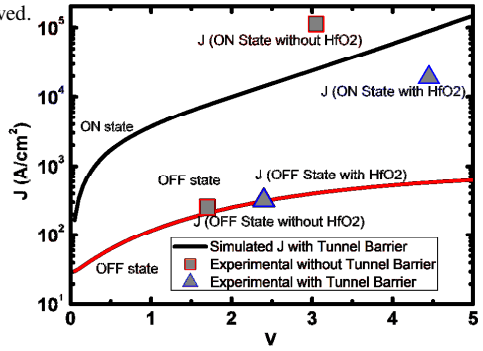


Fig. 6: Simulated current voltage characteristic and experimental conductance ratio in the ON and OFF state.

Switching Mechanism in VO_2: Electric Field Driven vs. Thermally Induced MIT.

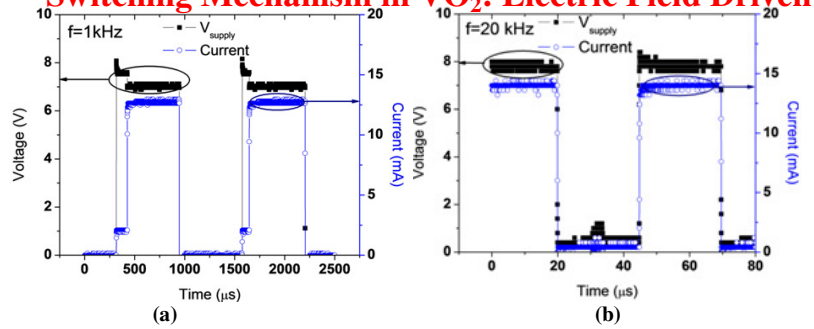


Fig. 7: Frequency dependent switching (FDS) at 275K analysis of non-tunneling device for (a) 1 kHz (b) 20 kHz. Device does not turn OFF beyond 20 kHz.

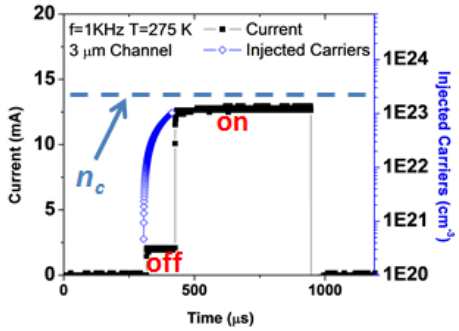
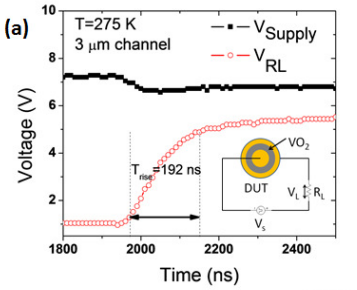


Fig. 8: Injected carrier density in ON state at f=1 kHz is close to Mott carrier density $n_c=2.1x10^{23}/cm^3$ indicating **field induced transition**.



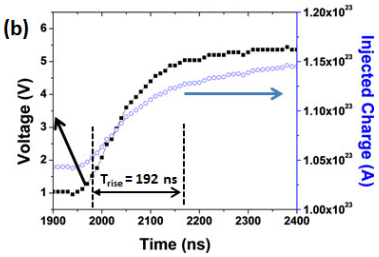


Fig. 9: (a) MIT transition time after the critical density has been achieved is 192 ns, for an R_L of 500 Ω. (b) At the start of the transition ~$1x10^{23}$ carriers are injected, close to the critical Mott carrier density of $2.1x10^{23}/cm^3$.

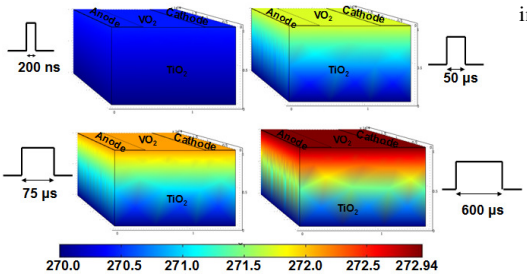


Fig. 10: 3D device simulation of temperature rise for various heat ~~heat~~ pulse widths applied indicate insufficient Joule heating to cause switching.

Thermal Conduction Model:	$\delta_{Ts}\rho C_p \frac{\partial T}{\partial t} - \nabla(K\nabla T) = Q$
Air/interface boundary conditions using convective heat transfer:	$n.(K\nabla T) = h(T - T_O)$
VO_2/TiO_2 & VO_2/Electrode boundary condition:	$n.(K_1\nabla T_1 - K_2\nabla T_2) = h(T_O - T)$

Table I: Heat balancing equations used for COMSOL.

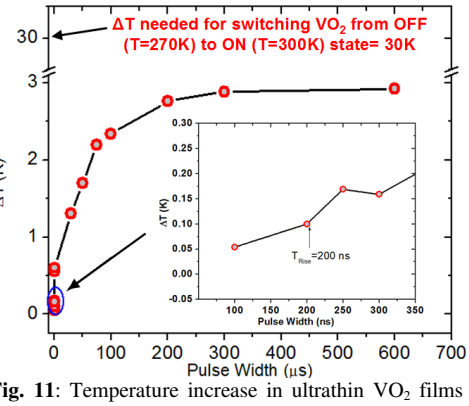


Fig. 11: Temperature increase in ultrathin VO_2 films during FDS measurements. The max temperature increase is one order of magntiude smaller than needed to thermally trigger the phase transition.

Two-stage Model for Lifetime Prediction of Highly Stable Amorphous-Silicon Thin-Film Transistors under Low-Gate Field

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Highly stable a-Si TFTs reported recently with extremely long operating lifetimes under DC gate bias are attractive for analog drivers of the OLEDs in AMOLED displays [1]. At room temperature, the time for the DC saturation current to drop to 50% is predicted to be 100 to 1,000 years. However, the lifetimes were extrapolated with a stretched-exponential model for defect creation in a-Si, based on only month-long room temperature tests. In this study, we present a two-stage threshold voltage shift model for lifetime prediction from temperature dependent measurements. We find that (i) a "unified stretched exponential fit" models the drain current degradation from 60°C to 140°; and (ii) there is a second instability mechanism that initially dominates up to hours or days at low temperatures, so that tests conducted only at room temperature may not predict lifetime accurately.

Highly stable back-channel passivated (BCP) a-Si TFTs were fabricated with a standard bottom-gate non-self-aligned process. The TFTs were biased in the saturation regime with a constant gate voltage of 5V (a gate field of 2.0×10^5V/cm) and a constant drain voltage of 7.5V. The positive threshold voltage shift of a-Si TFTs under gate bias leads to reduced drain current and thereby reduced OLED brightness in AMOLED displays.

At low-gate field, electrons in the channel of a-Si cause weak Si-Si bonds to break into dangling bonds, and the resulting electron trapping raises the threshold voltage (Fig. 1) [1-3]. The density of weak bonds with barrier-to-break energy E_b is usually modeled with an exponential function $n(E) \propto e^{E_b/kT_0}$ [2], where the characteristic temperature T_0 reflects the density distribution in bond energy of weak bonds. Thus, the threshold voltage shift vs. time can be characterized with the stretched exponential expression [2], with weaker bonds breaking first and stronger bonds later, and exhibiting a strong temperature dependence.

With fixed gate and drain bias, we measured drain current vs. time at temperatures from 20°C to 140°C in steps of 20°C, with a fresh TFT measured at each temperature (Fig. 2). Through a "thermalization energy" $E_{th} = kT\ln(\nu t)$ [3] and the current-voltage equation in saturation, we show that a "unified stretched exponential fit" to normalized drain current degradation $I_{D,nor} \equiv \frac{I_D(t)}{I_D(t=0)}$ can be obtained [4] (Fig. 3), with $I_{D,nor}(E_{th}) = \exp\left\{-2\exp\left[\frac{E_{th}-E_{act}}{kT_0}\right]\right\}$. Combination with the expression for thermalization energy enables a three parameter (ν, E_{act}, T_0) fit of drain current vs. time (Fig. 2). The fit agrees well with the experimental data in the temperature range from 80°C to 140°C. At lower temperatures (20°C to 60°C), the drain current degradation approaches the model only at long times. The short time degradation suggests that a second instability mechanism contributes in the beginning (Stage I), in addition to the above model (Stage II).

By subtracting the threshold voltage shift of the "unified stretched exponential fit" from the total threshold voltage shift data at 20°C, one finds that the stage I mechanism is fast and saturates around 0.1V in ~10^3 seconds (Fig. 4). A two-stage fit by adding Stage I to Stage II agrees well with the experimental data of the threshold voltage (Fig. 4) and normalized drain current (Fig. 5) over the entire measurement time for all temperatures from 20°C to 140°C. Clearly, using 20°C data for times less than 10^6 seconds does not accurately predict long term (Stage II) performance.

In summary, the drain current degradation has a strong temperature dependence and therefore is accelerated by raising temperature. However, initial fast mechanism needs to be identified and separated from the mechanism that dominates stage II for accurate lifetime prediction. Such a two-stage model will enable engineers to determine a-Si TFT operating lifetimes and stability with much greater confidence.

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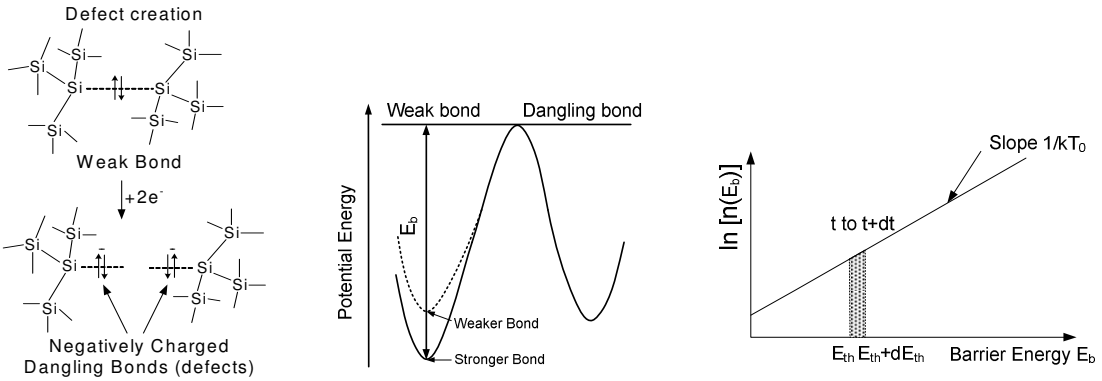

Fig. 1 Defect creation in a-Si TFTs. (a) Defect creation mechanism; (b) configuration coordinate diagram of defect creation and (c) density of weak bonds with barrier energy E_b modeled with $n(E) \propto e^{E_b/kT_0}$. From time t to $t + dt$, we approximate that weak bonds with barrier energies from E_{th} to $E_{th} + dE_{th}$ all break into dangling bonds (shaded area).

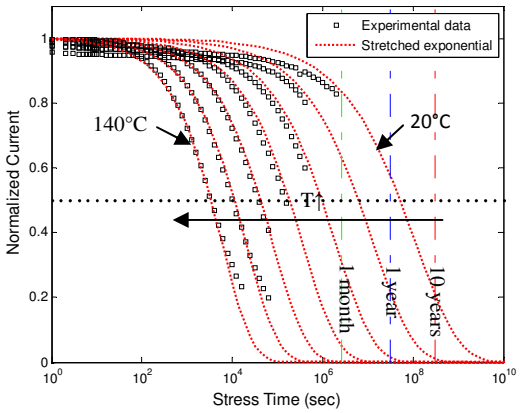

Fig. 2 Current degradation measured from 20°C to 140°C in steps of 20°C, and unified stretched exponential fit to experimental data.

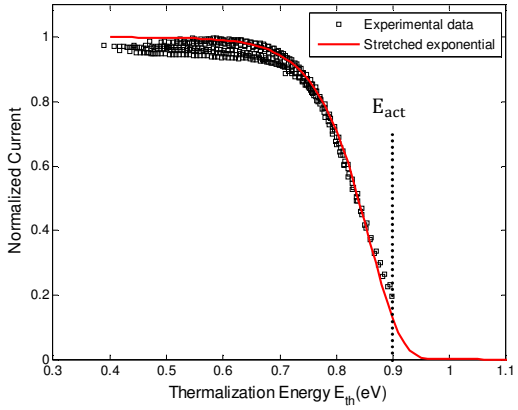

Fig. 3 Normalized drain current unified with thermalization energy $E_{th} = kT\ln(\nu t)$, where $\nu = 5\times10^6$ Hz, $E_{act} = 0.9$eV and $T_0 = 643$K.

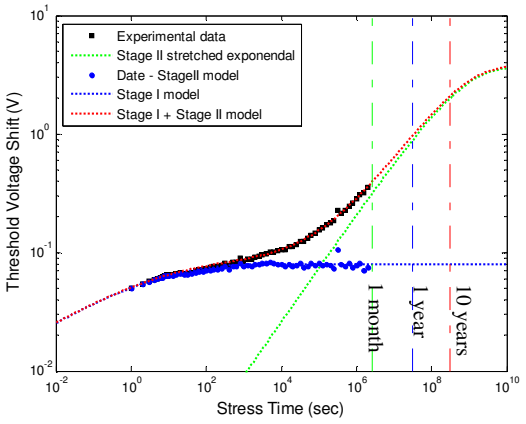

Fig. 4 Two-stage fit to threshold voltage shift vs. time at 20°C. The blue squares for Stage I "data" result from subtracting the Stage II model (determined by high temperature experiments) from the experimental data

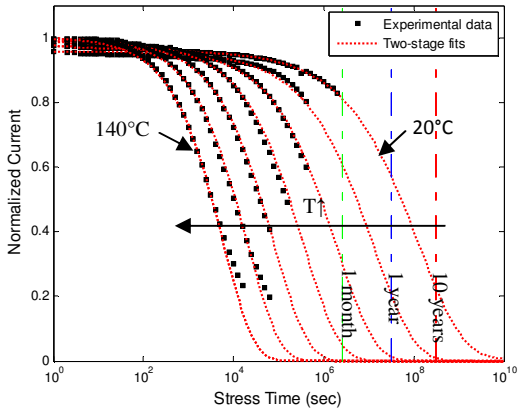

Fig. 5 Two-stage (Stage I + Stage II) fits to drain current degradation from 20°C to 140°C.

Session VII.A (Dean's Hall I)

Optoelectronic Devices

Wednesday PM, June 20th, 2012

Session Chair(s): Seth Bank, University of Texas Austin

1:30 PM VII.A-1
Tunnel Injection GaN/AlN Quantum Dot UV LED
J. Verma, P. K. Kandaswamy, V. Protasenko, A. Verma, H. Xing and D. Jena, Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA

1:50 PM VII.A-2
Characterization and Impact of Traps in Lattice-Matched and Strain-Compensated In1-xGaxAs/GaAs1-ySby Multiple Quantum Well Photodiodes
W. Chen[1], B. Chen[2], J. Yuan[2], A. Holmes[2], and P. Fay[1], [1]University of Notre Dame, Notre Dame, Indiana, USA and [2]University of Virginia, Charlottesville, Virginia, USA

2:10 PM VII.A-3
InAs Avalanche Photodiode with Improved Electric Field Uniformity
S. J. Maddox[1], W. Sun[2], Z. Lu[2], H. P. Nair[1], J. C. Campbell[2], and S. R. Bank[2], [1]Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, Texas, USA and [2]Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, Virginia, USA

2:30 PM VII.A-4
<278 nm Deep Ultraviolet LEDs with 11% External Quantum Efficiency
M. Shatalov[1], W. Sun[1], A. Lunev[1], X. Hu[1], A. Dobrinsky[1], Y. Bilenko[1], J. Yang[1], M. Shur[2], R. Gaska[1], C. Moe[3], G. Garrett[3], and M. Wraback[3], [1]Sensor Electronic Technology, Inc., Columbia, South Carolina, USA, [2]Department of Electrical, Computer, and Systems Engineering and Center of Integrated Electronics, Rensselaer Polytechnic Institute, New York, USA, and [3]U.S. Army Research Laboratory, Adelphi, Maryland, USA

2:50 PM VII.A-5
Unipolar Barrier-Integrated HgCdTe Infrared Detectors
A. M. Itsuno[1], J. D. Phillips[1], and S. Velicu[2], [1]Department of Electrical Engineering, University of Michigan-Ann Arbor, Ann Arbor, Michigan, USA and[2]EPIR Technologies, Inc., Bolingbrook, Illinois, USA

3:10 PM VII.A-6
Late News

Tunnel Injection GaN/AlN Quantum Dot UV LED

Jai Verma, Prem Kumar Kandaswamy, Vladimir Protasenko, Amit Verma, Huili (Grace) Xing and Debdeep Jena

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Light weight and robust ultraviolet (UV) light emitting sources find multitude of uses, for example in water purification, sterilization, bio sensors, solid state lighting and lithography. Direct bandgap III-Nitride semiconductors exhibit bandgap energies extending upto 6.2 eV (210 nm, deep UV). Thus, III-Nitrides are potential candidates for fabricating UV LEDs. But as we move to higher Al compositions to reach shorter wavelengths the internal quantum efficiency (IQE) severely degrades due to factors such as the valence band asymmetry, high threading dislocation densities, quantum confined Stark effect and inefficient n- and p-type doping. To mitigate the adverse effects of such factors and boost the IQE, we propose and demonstrate a new design which incorporates GaN quantum dots (QDs) in AlN barriers and uses tunneling to inject and transfer carriers through the active region.

Quantum dots (QDs) are 0 dimensional nanostructures which provide 3-dimensional confinement of carriers leading to improved radiative recombination efficiency and thus allows low threshold light emitting diodes (LEDs) and lasers. III-Nitride (InAlGaN) QDs, grown by Stranski-Krastanov (SK) and anti-surfactant methods, have been shown to emit in the ultra violet(UV) [1] as well as visible region [2] of the electromagnetic spectrum. Due to strong confinement QDs favor significant increase in emission energy with decrease in the size of the QDs for relatively less content of Al, than in quantum wells. In our design, the spatial distribution of electron and hole wavefunctions in pyramidal GaN QDs [3] as well as the thin AlN barrier promotes tunneling transport of carriers (electrons and holes) despite the large effective mass of holes, because confinement shifts the wavefunctions to higher energies, which in turn extends deep into the barriers. Since tunneling is the mode of transport, we need n- and p- type contact regions which absorb just above the emission wavelength of the QDs, leading to a relatively low composition AlGaN layers resulting in improved doping. Besides, the much speculated phonon bottle neck [4] problem associated with QD systems can be overcome, as the carriers are injected directly into the lowest energy state of the QD. Therefore, as a consequence of QDs in the active region most of the issues associated with high Al content in UV LEDs could be solved.

In this work, we report on electroluminescence from 8 period self-assembled GaN QDs embedded in AlN barriers (Figure 1) grown by plasma assisted molecular beam epitaxy (PAMBE), in SK growth mode, on commercially available AlN/sapphire templates. Heavily Si and Mg doped $Al_{0.45}Ga_{0.55}N$ layers were used as n-type and p-type contact layers respectively. From Z-contrast Scanning Transmission Electron Micrograph (Figure 1(b)) the QD and AlN barrier thickness was found to be 0.55 nm and 2.8 nm respectively. The Atomic Force Microscopy (AFM) scan of uncapped QDs shows a QD densitiy of ~3 x 10^{11} cm^{-2}. Electron beam deposited Ti/Al/Ni/Au and Ni/Au were used as n-and p-type contacts respectively. Thereafter the UV LED was characterized for room temperature electroluminescence. The spectrum showed peak emission at 341 nm at injection current of 25 A/cm^2. On increasing the injection current to 62 A/cm^2, emission was obtained at three different peak wavelengths: 341nm, 301nm and 261nm. The 341nm peak is attributed to emission from ground state of the QDs, the intense 301 nm emission is due to bandfilling effects at high injection currents and 261 nm appears when carriers recombine in the AlGaN contact region resulting from carrier spillover. The low voltage threshold for emission in QD incorporated structures paves way for efficient LEDs and laser diodes (LDs).

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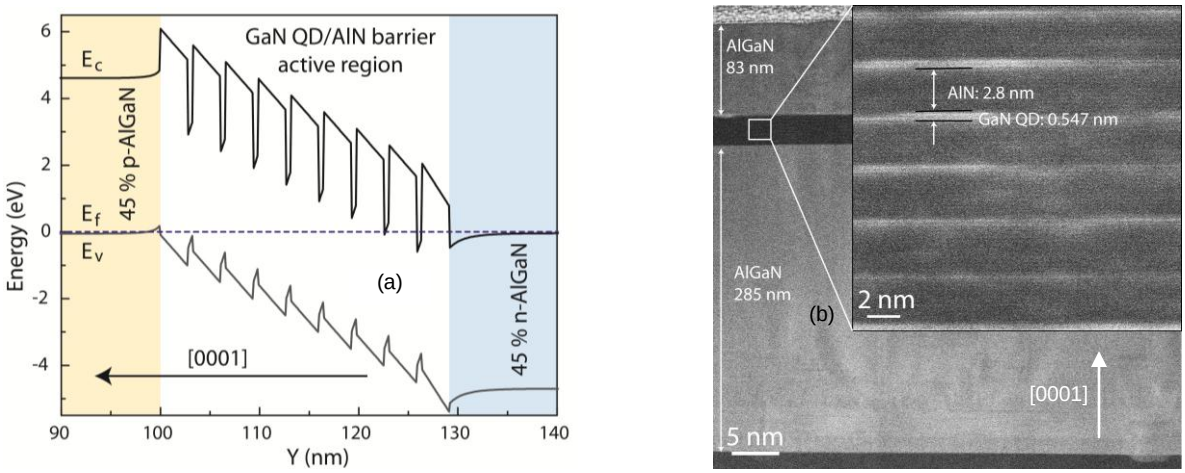

Fig 1. (a) Simulated energy band diagram of GaN/AlN quantum dot LED structure (b) Z-contrast Scanning Transmission Electron Micrograph of GaN/AlN QD LED strcuture showing the QD height and barrier thickness.

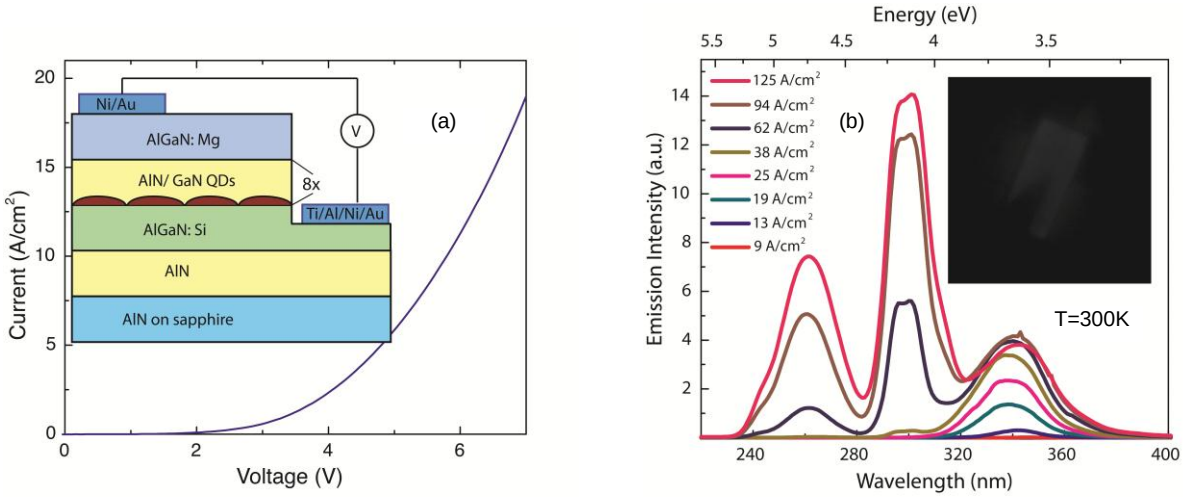

Fig 2. Experimental device characteristics of a MBE-grown GaN/AlN QD UV LED structure using tunnel transport of carriers. (a) The current-voltage characteristics indicate threshold voltage less than the GaN bandgap; (b) The electroluminescence spectrum indicates a peak at 340 nm at lower current densities. At higher current densities three different peak wavelengths: 341nm, 301nm and 261nm are observed. The illuminated LED is shown in the inset.

Characterization and Impact of Traps in Lattice-Matched and Strain-Compensated $In_{1-x}Ga_xAs/GaAs_{1-y}Sb_y$ Multiple Quantum Well Photodiodes

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InP-based multiple quantum well (MQW) photodiodes in the InGaAs/GaAsSb material system are promising for mid-infrared detection [1]; by including strain in these devices, the detection wavelength has been extended to beyond 3 μm [2]. However, owing to the relative immaturity of these materials, there have been few reports of the characteristics of defects in this system and their impact on device performance, especially under strain and at material compositions appropriate for MQW detectors. In this work, $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ (lattice-matched) and $In_{0.34}Ga_{0.66}As/GaAs_{0.25}Sb_{0.75}$ (strain-compensated) MQW photodiodes are evaluated using low-frequency noise spectroscopy (LFNS) and deep level transient spectroscopy (DLTS) to detect and extract the properties of defect levels, and their impact on dark current and noise performance of the photodiodes is evaluated.

The epitaxial structures of the lattice-matched and strain-compensated MQW photodiodes are illustrated in Fig. 1. The active regions consist of 100 pairs of type-II InGaAs/GaAsSb heterojunctions; Fig. 2 shows the corresponding band alignments under flatband conditions. Devices were mesa isolated using wet chemical etching using 3% Br:CH_3OH and H_3PO_4: H_2O_2:H_2O (1:1:10), and were passivated with 200 nm of PECVD SiO_2. Cr/Au n- and p-type contacts were formed by liftoff in a single evaporation.

Trap characterization for both types of photodiodes was performed using LFNS. In this technique, low-frequency noise spectra are measured as a function of bias and temperature; generation-recombination centers are manifested by Lorentzian features superimposed on a 1/f background. By scanning the temperature from 100 K to 300 K, trap lifetimes were extracted from the Lorentzian peaks in the measured spectra. Fig. 3 shows typical measured and fitted noise spectra (multiplied by frequency to accentuate the G-R component over the 1/f background) over the temperature and frequency ranges. Three traps were identified for both the lattice-matched and strain-compensated photodiodes, as summarized in the Arrhenius plot in Fig. 4. For the lattice-matched detectors, traps with activation energies of 0.14 eV, 0.34 eV and 0.43 eV and corresponding capture cross sections of 4.33×10^{-17} cm^2, 2.12×10^{-14} cm^2 and 1.13×10^{-14} cm^2, respectively, were obtained. For the strain-compensated devices, nearly identical activation energies of 0.12 eV, 0.33 eV and 0.43 eV were extracted; however, the capture cross sections were found to be considerably different, with corresponding values of 2.14×10^{-18} cm^2, 2.83×10^{-15} cm^2 and 3.75×10^{-15} cm^2, respectively. The similarity of the trap energies between the two device structures suggests that strain does not play a strong role in governing the structure of the traps, but does play a role in their apparent cross-section. Prior studies have shown traps at 0.11-0.13 eV in both bulk $In_{0.53}Ga_{0.47}As$ and $GaAs_{0.5}Sb_{0.5}$ [3], a trap at 0.38-0.4 eV has been previously observed in bulk $GaAs_{0.5}Sb_{0.5}$ [4], and a trap at 0.37 eV was observed to relate with $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ interfaces grown by MBE [3].

To determine the spatial location of these observed traps, DLTS was used. Typical observed capacitance transients for a lattice-matched detector are shown in Fig. 5 for the electron trap at 0.13 eV with capture cross section of 2.07×10^{-18} cm^2 (data included in Fig. 4). From the bias dependence of the DLTS transients, the spatial distribution was extracted [5] and is shown in Fig. 6; similar results were found for the strain-compensated structure. The apparent trap density peaks at approximately 1.26 μm above the n-InP/undoped InP interface, in the 25 nm undoped InGaAs transition layer at the anode.

These trap levels have a significant impact on device performance; Fig. 7 shows the measured dark I-V characteristics for both device types over temperature. At 300 K, these structures have measured responsivities at 2.6 μm of 0.18 A/W and 0.30 A/W with bias of -0.5 V [6]; this corresponds to a dark-current limited D* of 4.7×10^9 cm $Hz^{1/2}$/W and 6.3×10^9 cm $Hz^{1/2}$/W, respectively. The differences in the dark currents are attributed to the substantial differences in trap cross-sections observed. Extrapolation of the dark currents to the thermally-limited (defect-free) performance suggests the D* could be improved by about 40× (lattice matched) and 900× (strain compensated) compared to these current structures, highlighting the role of defects in these heterostructures.

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[6] B. Chen et al., *IEEE J. Quant. Elect*., vol. 47, pp. 1244, 2011

500 nm p-InP	500 nm p-InP
25 nm U.I.D. InP	25 nm U.I.D. InP
25 nm U.I.D. $In_{0.53}Ga_{0.47}As$	25 nm U.I.D. $In_{0.53}Ga_{0.47}As$
100 pairs 7nm $In_{0.53}Ga_{0.47}As$ /5nm $GaAs_{0.5}Sb_{0.5}$ QWs	100 pairs 7nm $In_{0.34}Ga_{0.66}As$ /5nm $GaAs_{0.25}Sb_{0.75}$ QWs
50 nm U.I.D. $In_{0.53}Ga_{0.47}As$	50 nm U.I.D. InP
500 nm n-InP	500 nm n-InP
Substrate n-InP	Substrate n-InP
(a)	(b)

Fig. 1. Device structures of (a) lattice-matched and (b) strain-compensated MQW photodiodes.

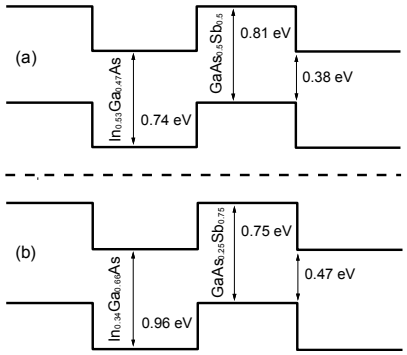

Fig. 2. Band alignment illustration for (a) lattice-matched and (b) strain-compensated photodiodes.

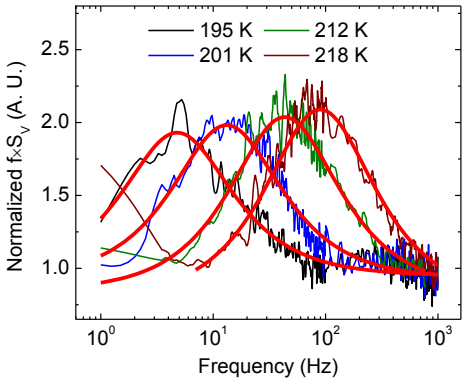

Fig. 3. Typical measured and fitted $f \times S_V$ (normalized) versus frequency, showing the Lorentzian shifts observed with temperature.

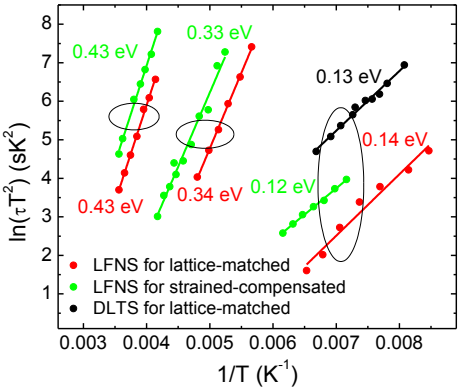

Fig. 4. Arrhenius plot of traps found by LFNS and DLTS.

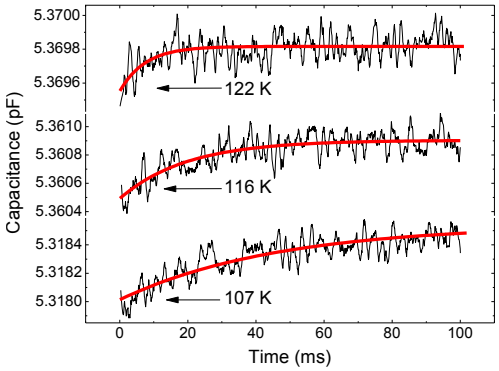

Fig. 5. Typical measured and fitted capacitance transients for a lattice-matched photodiode.

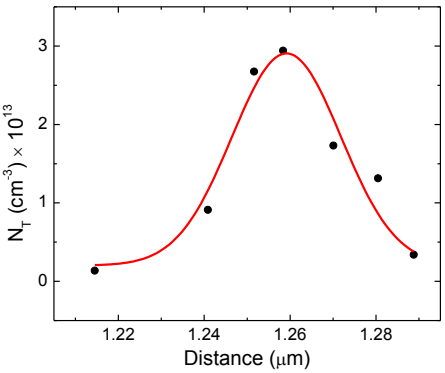

Fig. 6. Spatial profile extracted by DLTS of the 0.13 eV trap in a typical lattice-matched device.

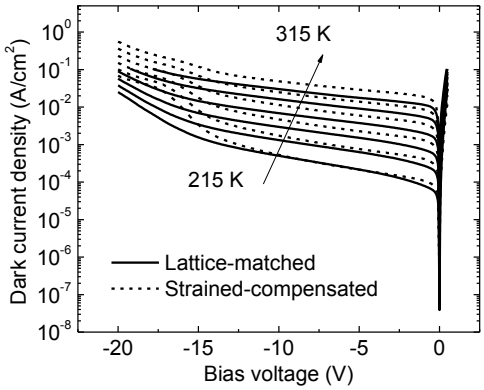

Fig. 7. Measured dark I-V characteristics for lattice-matched and strain-compensated detectors.

InAs Avalanche Photodiode with Improved Electric Field Uniformity

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A new class of avalanche photodiodes (APD) characterized by exclusive electron impact ionization and known as electron avalanche photodiodes (e-APD), have received considerable attention recently due to their ideal gain and excess noise characteristics. HgCdTe, the first material system in which exclusive electron impact ionization was demonstrated, has been the subject of substantial research and development for applications requiring mid and long wavelength infrared photodetectors with high sensitivity, including remote gas sensing, light detection and ranging (LIDAR), and both active and passive imaging. More recently, InAs has also been shown to demonstrate exclusive electron impact ionization and has subsequently come under intense study. Although InAs APD's have not yet reached the multiplication gains achievable in HgCdTe, the advantages inherent to III-V materials, including mature device fabrication and improved compositional uniformity, make InAs APD's particularly attractive for mid-infrared focal plane arrays (FPA). Here, we report a significant, ~5x, increase in the room temperature multiplication gain for InAs APD's, as compared to the state-of-the-art at 10 V reverse bias.

One of the biggest impediments to further improving the performance of InAs APDs appears to be the high unintentional background doping inherent to InAs, which results in a non-uniform electric field strength in the multiplication region. Simulated electric field profiles (Fig. 1) show a strong dependence on background doping concentration; even for an optimistic dopant concentration of $5x10^{14}$ cm^{-3}, the field is highly non-uniform. Such field non-uniformity limits the amount of gain that is achievable before undesirable band-to-band tunneling current begins to dominate. Background doping in InAs has previously been reported to be n-type even when SIMS data showed an order of magnitude more acceptor impurities than donor impurities.[1] We attribute the anomalous n-type doping to amphoteric native defects, which act as multiply ionizable donors in undoped InAs.[2] In order to mitigate the undesirable effects of this background doping, we present a proof-of-concept layer structure (Fig. 2) with a graded p-type doping profile designed to improve the electric field uniformity (Fig. 3), resulting in an increased multiplication gain by a factor of ~5 at 9.25 V reverse bias; further optimization of the doping profile should allow for even higher multiplication gains.

All samples were grown by solid-source molecular beam epitaxy (MBE) in an EPI Mod. Gen II system on n-type sulfur doped (100) InAs substrates. Mesa diodes ranging in diameter from 50 to 350 μm were defined by wet etching using H_3PO_4:H_2O_2:H_2O (1:1:1), followed by a 30 second dip in H_2SO_4:H_2O_2:H_2O (1:8:80) and subsequent passivation with SU-8 to reduce surface leakage current.[3,4] Bulk dominated dark current was verified by measuring dark current for various diode sizes and observing a linear dependence on area. Due to the extremely small band-gap of InAs, good Ohmic contacts were formed using unannealed Ti/Au (20/150 nm). Phase-sensitive detection, similar to ref. 5, is used to measure the multiplication gain and excess noise factor.

By leveraging an improved doping profile and the reduced background doping achievable with MBE growth, we demonstrate devices with minimal excess noise (Fig. 4) and a representative multiplication gain (Fig. 5) of ~70 at 9.25 V reverse bias – the highest gain reported thus far by a factor of ~5 for an InAs APD operated below 10 V reverse bias.

[1] A. Marshall, et al., 6th EMRS DTC Technical Conference (2009).
[2] W. Walukiewicz, J. Vac. Sci. Technol., B **6**, 1257 (1988).
[3] A. Marshall, et al., 4th EMRS DTC Technical Conference (2007).
[4] H.S. Kim, et al., Appl. Phys. Lett. **96**, 033502 (2010).
[5] K.S. Lau, et al., Meas. Sci. Technol. **17**, 1941–1946 (2006).

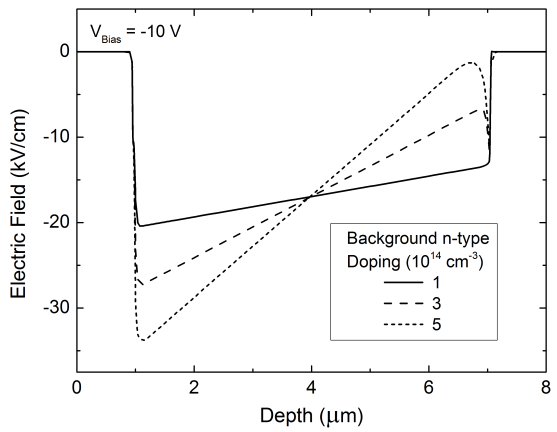

Fig. 1. Simulated electric field profiles for three different background doping concentrations at a reverse bias of 10V. Even for an optimistic background doping of $5x10^{14}$ cm^{-3}, the electric field profile is highly non-uniform.

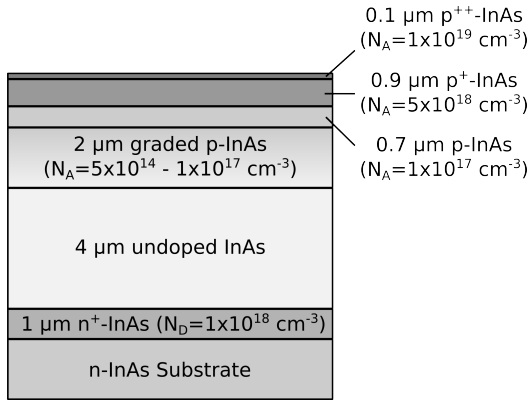

Fig. 2. Proof-of-principle InAs APD layer structure. The graded p-type doping profile is designed to improve electric field uniformity in the multiplication region.

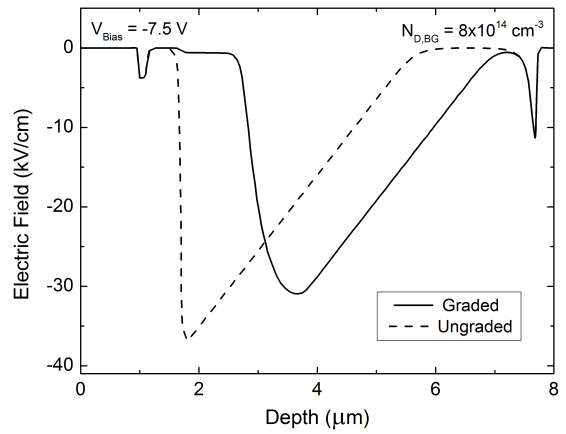

Fig. 3. Simulated electric field profiles at a reverse bias of 7.5V for the layer structure shown in Fig. 2, and a similar structure without the graded p-type doping. The background doping is taken to be n-type with a concentration of $8x10^{14}$ cm^{-3}. Further improvement to the electric field uniformity could be achieved by optimization of the graded p-type doping layer.

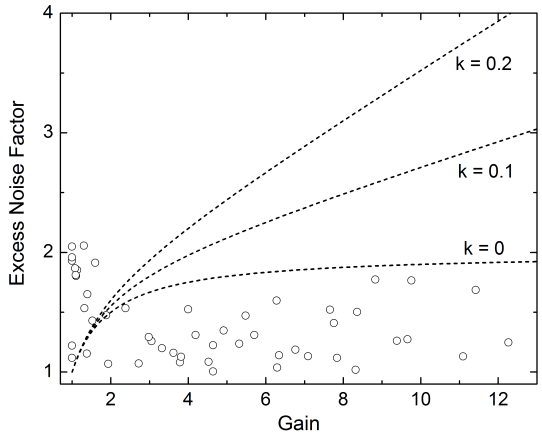

Fig. 4. Excess noise factor measured at room temperature on 70 μm diameter diodes with the layer structure shown in Fig. 2. The dashed lines represents McIntyre's local field model for different values of k, the hole to electron ionization coefficient ratio.

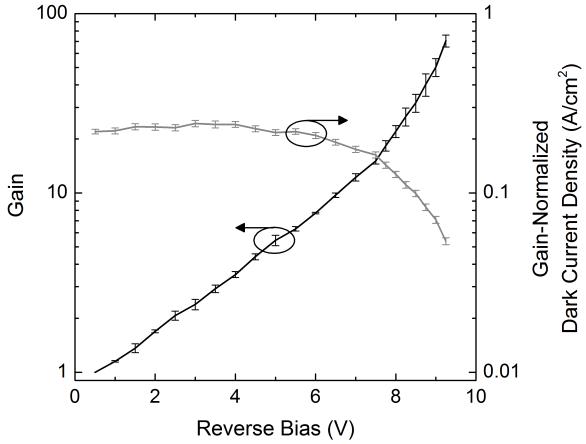

Fig. 5. Avalanche gain (black line) and gain-normalized dark current density (grey line) measured at room temperature on 70 μm diameter diodes with the layer structure shown in Fig. 2. The values shown are the average from multiple devices, and the error bars represent the sample standard deviation. A gain of ~70 is realized at the record low reverse bias of 9.25V for an InAs APD.

278 nm Deep Ultraviolet LEDs with 11% External Quantum Efficiency

Max Shatalov, Wenhong Sun, Alex Lunev, Xuhong Hu, Alex Dobrinsky, Yuri Bilenko, Jinwei Yang, Michael Shur,[1] Remis Gaska, Craig Moe,[2] Gregory Garrett,[2] Michael Wraback[2]

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III-Nitride based deep ultraviolet (DUV) light emitting diodes (LEDs) offer smaller size, wider choice of peak emission wavelengths, lower power consumption and reduced cost compared to mercury vapor lamps and other UV light sources. Increasing efficiency of DUV LEDs accelerates their applications in bio-agent detection, analytical instrumentation, phototherapy, disinfection, biotechnology and sensing. We report on 278 nm DUV LEDs with external quantum efficiency exceeding 10 % achieved by improvements of material quality and light extraction.

The DUV LED structure used in this work consisted of very high quality AlN, n^+-AlGaN clad layers, AlGaN MQW active region, Mg-doped p-AlGaN clad, and p^+-AlInGaN contact layers, which were grown over (0001) sapphire substrates using combination of conventional MOCVD and proprietary MEMOCVD® process. Optimized MEMOCVD® growth process resulted threading dislocation density in the MQW of $2x10^8$ cm^{-2}, which is more than one order of magnitude less than typical value achieved before. Photoluminescence (PL) studies confirmed that the MQW structures grown on high quality templates provided internal quantum efficiencies (IQE) up to 55% at carrier density of $5x10^{17}$ cm^{-3}. Significant increase of IQE from 15 % to 53% was measured at low carrier density ($5x10^{16}$ cm^{-3}) for epitaxial structures with $2x10^9$ cm^{-2} and $2x10^8$ cm^{-2} densities of dislocations in the active region.

Following the wafer growth, square geometry DUV LEDs were fabricated using standard RIE mesa etching and e-beam metallization. For high efficiency LED structures, transparent p-AlGaN layer were used to facilitate multiple pass light extraction using highly DUV reflecting p-contact metal. To further increase light extraction, LED dies were encapsulated with index matching UV-stable and -transparent polymer. According to ray tracing simulations the combination of multiple pass extraction and encapsulation provided more than a 2.5× increase in the light extraction efficiency. Devices with a junction area of $0.035mm^2$ and $0.5mm^2$ were fabricated for comparison.

L-I characteristics of packaged small and large devices are included in Fig. 1. Output power measured for devices with different areas are nearly the same despite significantly different current densities. This agrees well with measurements of the IQE, which varies very slightly with the carrier density and is indicative of a reduced density of nonradiative defects. The emission spectra of DUV LED at several CW currents included in Fig. 2 show emission peak at 278 nm. External quantum efficiency (EQE) and wall plug efficiency (WPE) of two DUV LEDs are shown in Fig. 3 and Fig. 4, respectively. EQE reached 10.4 % and 10.9 % for small and large die size devices, respectively. WPE of 7.8% was measured for larger device due to lower forward voltage, whereas WPE of 5.5 % was achieved for small chip design. These results represent the highest EQE and WPE reported for sub-300 nm wavelength semiconductor light sources.

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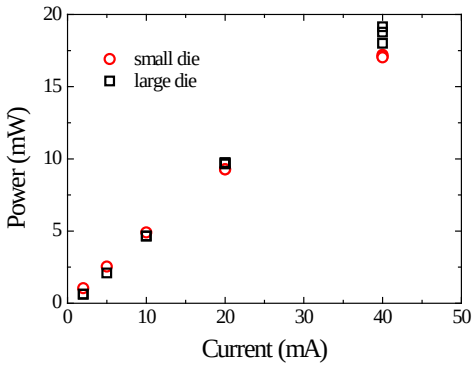

Figure 1. CW L-I characteristics of DUV LEDs with different junction area.

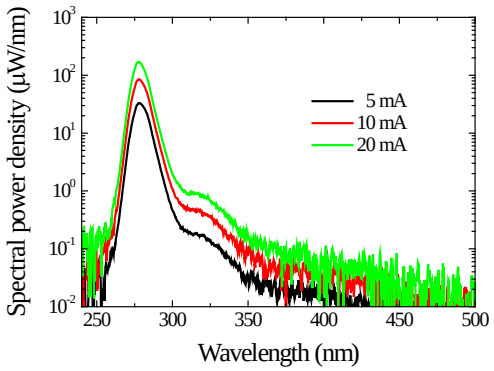

Figure 2. Emission spectra of small DUV LED at different drive currents.

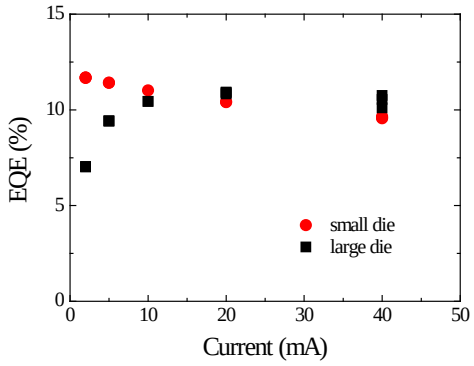

Figure 3. EQE as a function of drive current for two DUV LED devices.

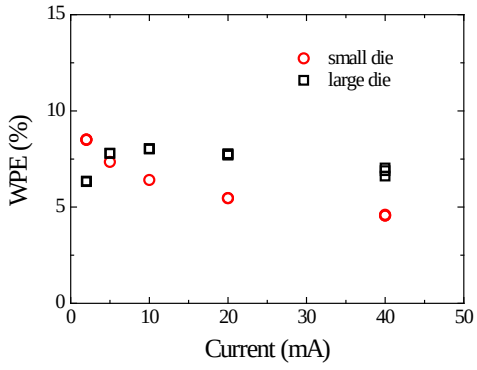

Figure 4. WPE as a function of current for DUV LEDs with different junction area.

Unipolar Barrier-Integrated HgCdTe Infrared Detectors

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HgCdTe-based infrared (IR) detectors remain the front-runner for high performance IR focal plane array (FPA) applications due to their favorable material and optical properties. While state-of-the-art HgCdTe *p-n* junction technology such as the double layer planar heterostructure (DLPH) devices can achieve near theoretical performance in the mid-wave and long-wave infrared (MWIR, LWIR) spectral ranges, the cryogenic cooling requirements to suppress dark current are still much greater than desired. HgCdTe material growth by molecular beam epitaxy (MBE) provides the accurate control over alloy composition and doping required to achieve future detector architectures that may serve to reduce dark current for enhanced operation. However, controllable *in situ p*-type doping of HgCdTe by MBE is still problematic. As a potential solution to address these issues, we propose a unipolar, type-I barrier-integrated HgCdTe nBn IR detector based on similar principles to the type-II nBn structure used in III-V materials [1] with the intent that it may serve as a basis for advanced HgCdTe-based architectures for reduced cooling requirements.

Our initial theoretical work examined optimized structural designs for unipolar HgCdTe nBn detectors [2], which are predicted to achieve comparable performance to conventional DLPH detectors with the added advantage of an all *n*-type architecture. We used these design parameters as the basis for fabricating MWIR and LWIR unipolar single element nBn detectors from MBE HgCdTe epilayers. The HgCdTe nBn detectors exhibit unique measured current-voltage (I-V) and photoresponse characteristics predicted by numerical simulations. Unlike type-II III-V nBn structures, the HgCdTe-based devices exhibit a non-zero valence band offset ΔE_v resulting in distinct barrier-influenced behaviors that warrant examination. Temperature dependent dark current density measurements exhibit behavior limited by perimeter leakage mechanisms and comparisons between planar-mesa and mesa device configurations reveal unique I-V characteristics. 'Turn-on' threshold bias ranges of -0.5 to -1.0 V (MWIR) and -0.2 to -0.6 V (LWIR) were observed for different device configurations due to differences in the valence band offset. Relative response measurements exhibited barrier-influenced behavior corresponding to bias-dependent band-edge alignment. We made strategic modifications to the MWIR nBn structure following the analysis of the first-iteration HgCdTe nBn devices to improve dark current density and reduce the threshold bias voltage, resulting in measured dark current density values ~10^5 A/cm^2 lower than those observed in previous comparable devices and a lower turn-on bias of roughly -0.2 V. With further structural modifications and optimization, we expect to see increased improvements in the HgCdTe nBn detector performance.

Our study of the HgCdTe nBn device illustrates the feasibility of a barrier-integrated, all *n*-type HgCdTe IR detector structure, and we propose the unipolar NBvN architecture which is a hybrid of the Auger-suppressed high operating temperature (HOT) structure [3] and the nBn detector. Numerical simulations of the NBvN detector exhibit lower dark current densities and higher detectivity values compared to the nBn and conventional DLPH structures for both MWIR and LWIR spectral ranges at similar temperatures which confirm the ideal design is conducive to higher temperature operation. The results suggest the HgCdTe nBn and NBvN devices are potentially viable alternative solutions for achieving next-generation devices, addressing the limitations faced by conventional *p-n* junction technology.

[1] S. Maimon and G. W. Wicks, *Appl. Phys. Lett.* **89**, 151109-1 (2006).
[2] A.M. Itsuno, J.D. Phillips, and S. Velicu, *J. Electron. Mater.* **40**(8), 1624 (2011).
[3] T. Ashley and C.T. Elliott, *Electron. Lett.*, **21**(10), 451 (1985).

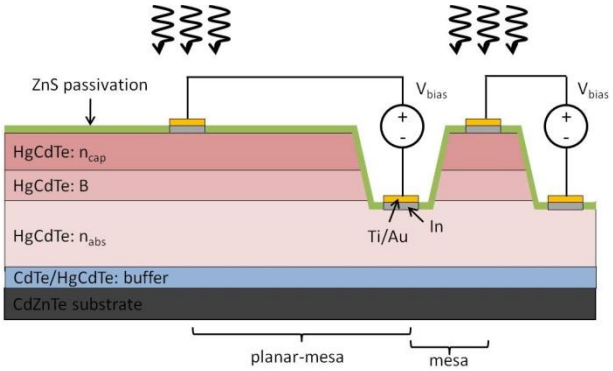

Fig.1: Cross-sectional schematic of HgCdTe nBn structure.

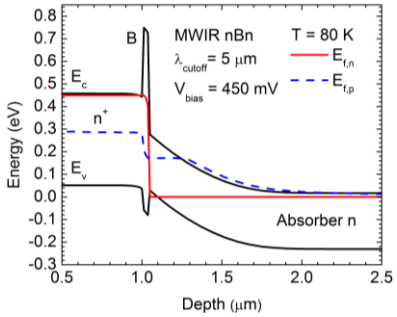

Fig. 2: Calculated band diagram of ideal optimized MWIR nBn structure under bias.

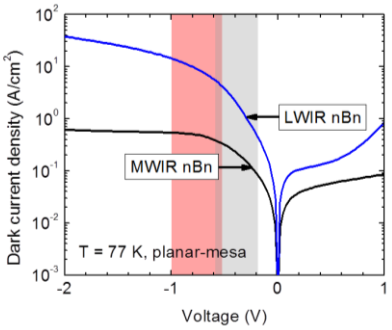

Fig. 3: Measured I-V curves of nBn devices. Turn-on bias ranges indicated in red (MWIR) and gray (LWIR).

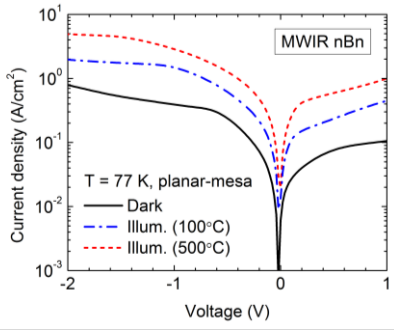

Fig. 4: Dark and blackbody illuminated I-V curves of MWIR HgCdTe nBn devices.

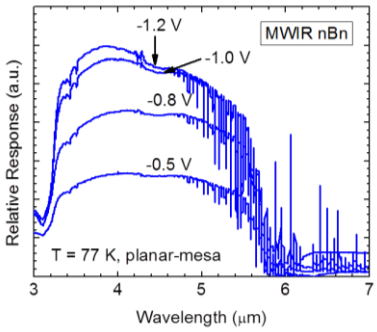

Fig. 5: Barrier-influenced relative response measurements of MWIR planar-mesa nBn structure.

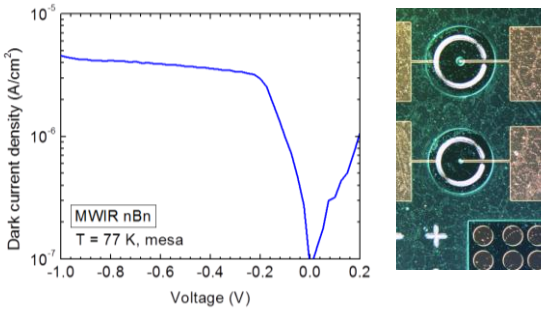

Fig. 6: I-Vcharacteristic of modified MWIR nBn structure and top view of fabricated mesa devices.

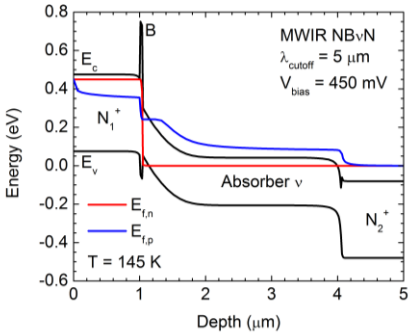

Fig. 7: Calculated band diagram of a proposed unipolar MWIR NBνN structure under bias.

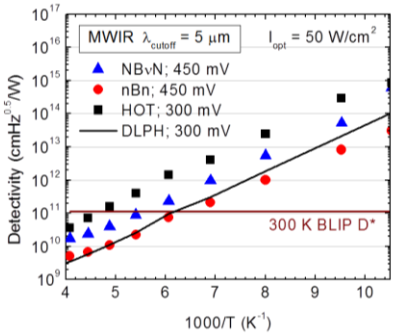

Fig. 8: Calculated detectivity values for MWIR DLPH, nBn, HOT, and hybrid NBνN detectors.

Session VII.A (Dean's Hall I)

Optoelectronic Devices

Wednesday PM, June 20th, 2012

Session Chair(s): Seth Bank, University of Texas Austin

1:30 PM VII.A-1
Tunnel Injection GaN/AlN Quantum Dot UV LED
J. Verma, P. K. Kandaswamy, V. Protasenko, A. Verma, H. Xing and D. Jena, Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana, USA

1:50 PM VII.A-2
Characterization and Impact of Traps in Lattice-Matched and Strain-Compensated In1-xGaxAs/GaAs1-ySby Multiple Quantum Well Photodiodes
W. Chen[1], B. Chen[2], J. Yuan[2], A. Holmes[2], and P. Fay[1], [1]University of Notre Dame, Notre Dame, Indiana, USA and [2]University of Virginia, Charlottesville, Virginia, USA

2:10 PM VII.A-3
InAs Avalanche Photodiode with Improved Electric Field Uniformity
S. J. Maddox[1], W. Sun[2], Z. Lu[2], H. P. Nair[1], J. C. Campbell[2], and S. R. Bank[2], [1]Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, Texas, USA and [2]Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, Virginia, USA

2:30 PM VII.A-4
<278 nm Deep Ultraviolet LEDs with 11% External Quantum Efficiency
M. Shatalov[1], W. Sun[1], A. Lunev[1], X. Hu[1], A. Dobrinsky[1], Y. Bilenko[1], J. Yang[1], M. Shur[2], R. Gaska[1], C. Moe[3], G. Garrett[3], and M. Wraback[3], [1]Sensor Electronic Technology, Inc., Columbia, South Carolina, USA, [2]Department of Electrical, Computer, and Systems Engineering and Center of Integrated Electronics, Rensselaer Polytechnic Institute, New York, USA, and [3]U.S. Army Research Laboratory, Adelphi, Maryland, USA

2:50 PM VII.A-5
Unipolar Barrier-Integrated HgCdTe Infrared Detectors
A. M. Itsuno[1], J. D. Phillips[1], and S. Velicu[2], [1]Department of Electrical Engineering, University of Michigan-Ann Arbor, Ann Arbor, Michigan, USA and [2]EPIR Technologies, Inc., Bolingbrook, Illinois, USA

3:10 PM VII.A-6
Late News

Physics and Scaling Prospects of pH-Based Genome Sequencers

Jonghyun Go and Muhammad A. Alam
School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907, USA

Motivation/Background The sensitive/precise detection of biomolecules is essential for clinical diagnosis, personalized medicine, environmental monitoring, etc. Specifically for personalized medicine, a key goal is to decode human genome by reading DNA base-pairs so as to discover genetic variation and genome-related diseases. Over the years, several Gen-II sequencing technologies have decreased costs and improved sequencings speed [1]. Most of these techniques however rely on bulky optical detection schemes, incompatible with the requirements for low-cost, point-of-care diagnosis. Recently, however, Ion Torrent [2] has addressed this concern by demonstrating a pH-based sequencer on a CMOS platform: The sequencer consists of millions of MOSFETs whose top layer is covered micro-meter size wells covered with a thin layer polymer (Fig. 1). Since it detects the sequences of fragmented DNA strands by capturing the voltage signal induced by protons (H^+), a byproduct from DNA hybridization (Fig. 1c), each cell behaves like a simple ion-sensitive FET (ISFET) [3]. Sequencing cost has dropped dramatically, and further cost reduction is promised. Since the performance and cost are directly correlated to the number of wells in a single chip (1-100M wells), its scalability is a critical issue. In this paper, we explore the operation of these devices by sophisticated and experimentally calibrated models and explain the challenge to scalability due to ISFET channel noise and well-to-well cross-talk.

Model The following equations define the response of a sensor: (i) transient proton distribution inside a well is described by proton diffusion equation (See Table I) wherein H^+ is injected from the bead surface following hybridization. The transient increase of H^+ at the oxide-electrolyte interface is coupled self-consistently with the Poisson-Boltzmann equation and the surface binding model to solve the electrostatic potential (Ψ)/ carrier distribution (n) in the channel [4]. Finally, we compute the channel current $I_{DS} = \mu n(W/L)V_{DS}$ − where μ, W and L is the mobility, width and length of the channel, respectively.

Results/Discussions Fig. 2 shows the temporal distribution of proton inside the well and the polymer layer (the diffusion coefficient of protons in electrolyte and polymer is $D_{free}= 9.31\times10^{-5}$ and $D_{poly}= 4\times10^{-8}$ cm^2/s, respectively). The calculated voltage shift (ΔV) in MOSFET successfully explains the experiment data with two different sizes of wells and beads, as shown in Fig. 3. As we scale the microwells by a factor of κ, the sensitivity remains constant: this is because the number of protons released from bead is proportional to the bead area ($\sim\kappa^{-2}$) and the sensor surface area is also scaled by a factor of κ^{-2}. Since the surface group charge on the oxide surface changes linearly with proton density while the amount excess protons is much smaller than that in the well, the voltage signal remains constant.

To estimate the minimum detectable pH change per base-pair exchange (~0.02 in Ref. [2]), we need to consider the scaling of 1/f noise, the dominant noise source in ISFET [5]. The integrated noise (δV) for a given frequency range (f_1-f_2) is summarized in Table I. Fig. 4 shows two scenarios in noise scaling (blue curves): (i) *coupled scaling*: the MOSFETs (W and L) are scaled by the same factor as the sensor well, or (ii) *decoupled case*: the wells are scaled, but ISFET is not. For a given noise threshold (e.g., 1/3 of sensitivity signal), we conclude that full scaling is difficult, as the signal is corrupted by the noise even for $\kappa\sim2$. In the best case, the technology is scalable, but MOSFET density will set the upper limit. Finally, regarding the implication of cross-talks between neighboring wells, the Fig. 5 shows the distribution of protons in a two-well system with microfluidic chamber. Fig. 6 shows the ratio of responses in two wells and allows us to conclude that the corruption due to cross-talk negligible even for scales technology and thus not a not scaling concern.

Reference: [1] M. L. Metzker, Nat. Rev. Genetics, 11, p.31 (2009). [2] J. M. Rothberg et al., Nature 475, p. 348 (2011). [3] P. Bergveld, IEEE Trans. Biomed. Eng., BME-17, p. 70 (1970). [4] J. Go et al., IEDM (2010). [5] Deen et al., J. Appl. Phys., 100, 074703 (2006).

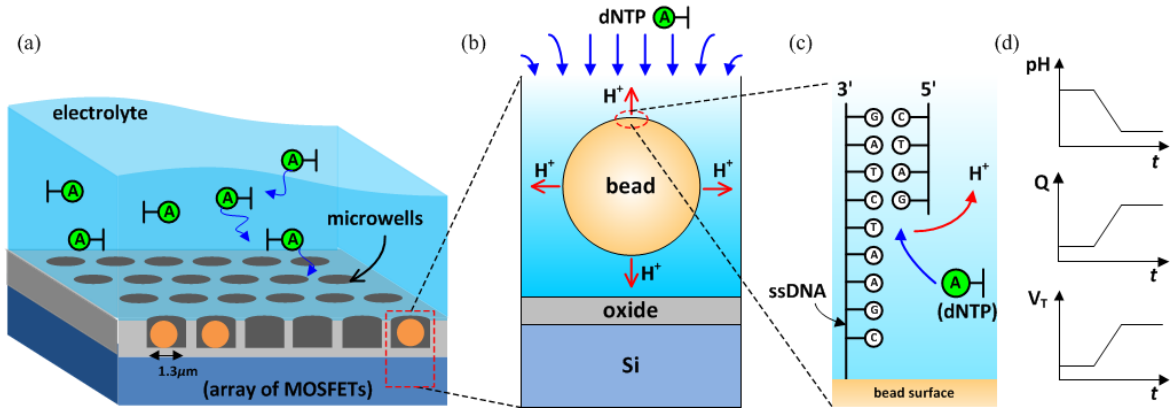

Fig. 1 (a) A schematic of pH-based genome sequencer. The array of MOSFETs is covered by sensing membrane consisting of millions of microwells, individually loaded with microbeads. (b) The surface of the beads is predecorated by single-stranded DNA (ssDNA) as shown in (c). Once the introduced dNTP (illustrated as 'A') molecules diffuse in electrolyte and arrive at the bead surface, the hybridization event releases a proton (H^+). The protons so generated modulate the local pH inside the wall. In response, the net charge of surface group on the oxide surface changes, which is translated to modulation of MOSFET conductance and its threshold voltage (V_T) in (d).

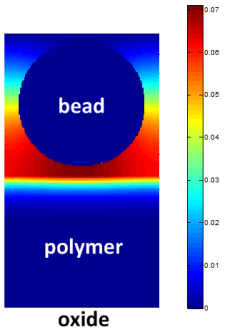

Fig. 2 A proton diffusion profile at a given time inside a microwell. The protons released from the bead surface diffuses through the polymer layer to reach electrolyte/oxide surface.

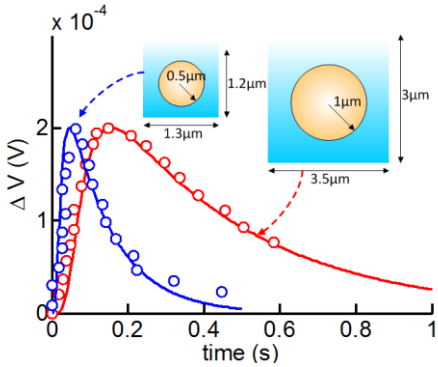

Fig. 3 The comparison between experiment data (circles) [2] and numerical simulation (solid lines) for a larger (red) and a smaller well (blue). The polymer layers have been scaled correspondingly.

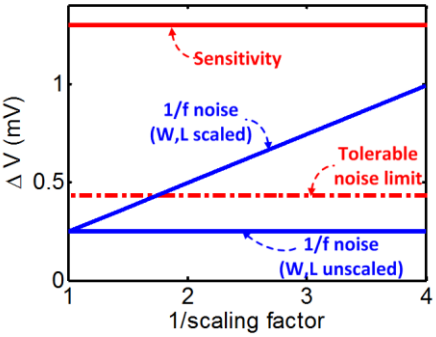

Fig. 4 The scaling of sensitivity, its tolerable noise limit (dashed line). The 1/f noise from MOSFET is calculated for two scenarios: (i) when MOSFET scales by the same factor as the microwell, (ii) when the well is scaled, but the MOSFET is not.

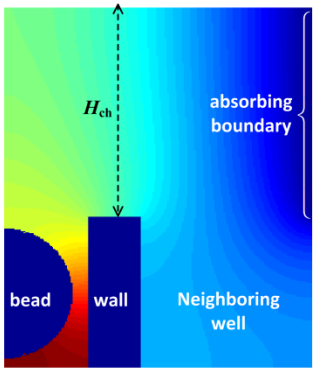

Fig. 5 Proton profile at a given instant of time. The cross-talk between the well containing the bead and a neighboring well is determined by integrating the proton profile over time. The absorbing boundary represents the effect of microfluidic channel that removes the protons from the system.

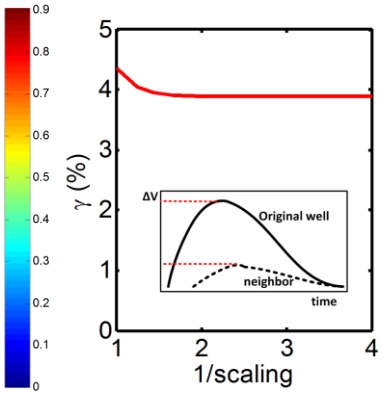

Fig. 6 The scaling relationship of the ratio of peaks (γ) for the responses of an original well and its neighbor. The effect of crosstalk quickly saturates and is negligible compared to the original signal. Here the chamber height (H_{ch}) is assumed to be 1.7μm.

	equations
Proton diffusion	$\frac{d\rho(x,y,t)}{dt} = D\nabla^2\rho(x,y,t)$
Poisson-Boltzmann	$-\nabla\bullet(\varepsilon\nabla\Psi) = \rho$
Surface binding model	$\sigma_{OH} = qN_s \frac{\frac{10^{pK_a-pH}}{\exp(\beta\psi_0)} - \frac{10^{pH-pK_b}}{\exp(-\beta\psi_0)}}{1+\frac{10^{pK_a-pH}}{\exp(\beta\psi_0)} - \frac{10^{pH-pK_b}}{\exp(-\beta\psi_0)}}$
MOSFET 1/f noise [5]	$S_{V_{FB}} = \frac{q^2kTN_t\lambda}{fWLC_{eff}^2}$ $\delta V = \sqrt{S_{V_{FB}}\left[1+\left(\alpha\mu_{eff}C_{eff}\frac{I_{DS}}{g_m}\right)\right]^2 \log\frac{f_2}{f_1}}$

Table I The equations for calculating transient response of proton detection and the1/f noise model in MOSFET. The pH-dependent charge on oxide surface follows the surface binding model.

Biologically-inspired Learning Device using Three-terminal Ferroelectric Memristor

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A simple synaptic device with a spike-timing-dependent synaptic plasticity (STDP) learning function is a key device that can realize a brain-like processor. STDP is a learning mechanism of synapses in mammalian brains [1]. A memristor [2, 3] is a promising candidate for synaptic devices. However, since the conventional memristor is a two-terminal electric element and the signal magnitude at learning exceeds the processing, it is difficult to realize STDP learning by simultaneously processing the signal. We proposed a unique three-terminal memristor using a ferroelectric thin film [4]. Its three-terminal device structure enables the STDP function without disturbing the signal processing between neurons (Fig. 1). This all oxide memristor (OxiM) has a ferroelectric gate field-effect transistor structure (Fig. 2). Since the polarization of $Pb(Zr,Ti)O_3$ film is changed by applying gate voltage (V_G), the channel conductance at the ZnO / $Pr(Zr,Ti)O_3$ interface can be modulated (Fig. 3). Memorized conductance can be maintained without fluctuation [4]. In addition, ferroelectric polarization can be modulated by changing the height and the width of the applied voltage pulse to the gate electrode. Fig. 4 shows the conduction change after applying pulse voltages.

A multi-valued memorization characteristic is needed for neuromorphic devices [5]. In the STDP learning rule, the relative time between pre-synaptic and post-synaptic neurons defines the synapse weight. Since brains can learn and function with many synapses by adjusting their synapse weight, the STDP function is crucial. Using OxiM, we can realize this function by a simple control circuit. As shown in Fig. 5, non-linear voltage (V_{PRE1}) is applied to the gate electrode of OxiM while the selector is switched to the V_{PRE1} node by the pulse voltage (V_{POST}). The timing relation between V_{PRE1} and V_{POST} is shown in Figs. 6(a) and (b). Here, time difference (Δt) is defined as the difference of the center of voltage waves V_{PRE1} and V_{POST}. By changing Δt, V_G was changed (Fig. 6(c)). Applying V_G to the gate electrode, conductance modulation was realized based on the characteristics shown in Fig. 4. As shown in Fig. 7, the conductance changed based on Δt and STDP modulation was realized, which is thousands of times faster than the nerve system.

We fabricated a neuron circuit by wiring the current output from OxiM to the analog integrator composed of an op-amp (Fig. 5). Fig. 8 shows the output voltage (V_{OUT}) from the neuron circuit. Controlled by the pulse voltage (V_{PRE2}), the switching transistor was turned ON for 15 μsec and OFF for 25 μsec. When the transistor was turned ON, the current through OxiM was input to the analog integrator and V_{OUT} increased based on the integration of the charge flow. Since the current was regulated by the conductance of OxiM, the behaviors of V_{OUT} changed based on the OxiM conductance. Before STDP learning ($t < 0$ μsec), V_{OUT} showed the same trajectory, which means the conductance was identical in each case. Around $t = 0$ μsec, STDP modulation was generated by time difference Δt between applying V_{PRE1} and V_{POST}. The influence of the charge generation by applying V_{POST} was eliminated by the refractory period of 100 μsec. For $\Delta t = 1$ μsec, as the conductance became larger than that before learning ($t < 0$ μsec), the peak voltage of V_{OUT} also became larger than that at $t < 0$ μsec. The peak voltage of V_{OUT} at $\Delta t = -6$ μsec became smaller. For $\Delta t = 12$ μsec, since $|\Delta t|$ was too large, V_{OUT} did not change very much, which was consistent with the slight conductance change at $\Delta t = 12$ μsec (Fig. 7).

We successfully modulated the neuron output by real-time STDP. Since OxiM is a three-terminal electric element, the conductance can be modulated by the gate voltage regardless of the signal flow through the channel. These characteristics make it possible to learn new input patterns without aborting the signal processing. This means we can simultaneously realize pattern recognition and pattern learning like a brain. By using OxiM, a biological learning device is promising. Integrating OxiMs will realize a brain-like processor, which is operated in a different architecture from conventional Von Neumann machines.

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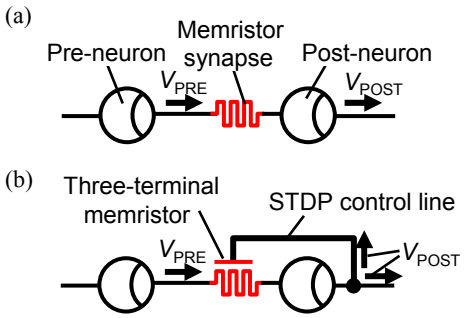

Fig. 1 Control flow of synapse composed of (a) conventional memristor and (b) three-terminal memristor

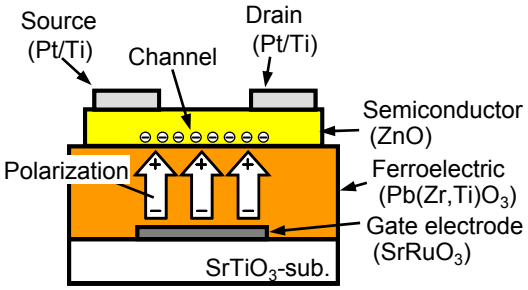

Fig. 2 Schematic image of ferroelectric memristor (OxiM)

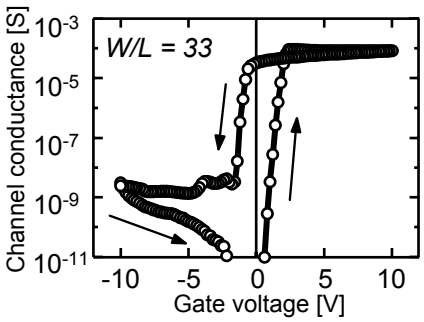

Fig. 3 Conductance-gate voltage characteristics of OxiM

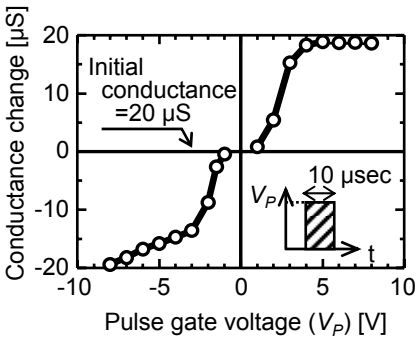

Fig. 4 Relation between pulse voltage (V_P) and change of channel conductance

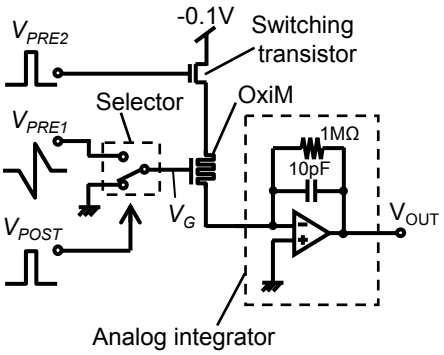

Fig. 5 Schematic image of a neuron circuit

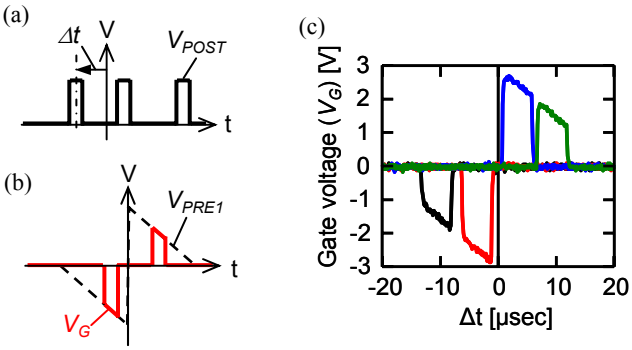

Fig. 6 Waveform of (a) V_{POST} and (b) V_{PRE1}. (c) Measured V_G for different Δt.

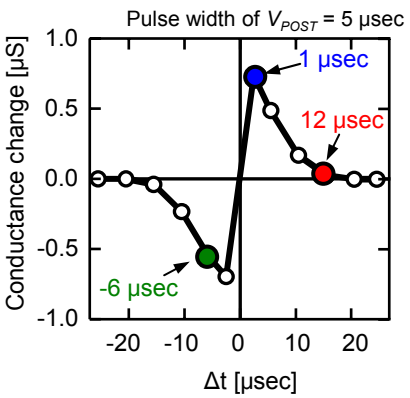

Fig. 7 Experimental result of STDP modulation

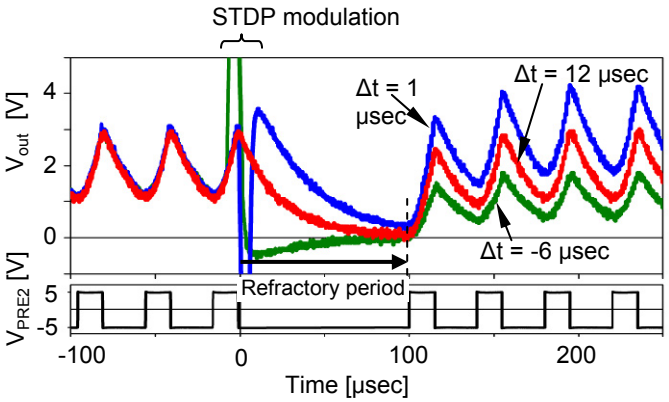

Fig. 8 Examination results of real-time STDP modulation. STDP modulation was applied at time = 0. V_{OUT} trajectories changed by Δt values.

Fabrication and Characterization of Field Effect Reconfigurable Nanofluidic Ionic Diodes: Towards Digitally-Programmed Manipulation of Biomolecules

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Analogous to a solid-state semiconductor diode for regulating the flow of electrons/holes to one preferential direction, nanofluidic diodes are being developed to achieve the rectified ionic transport. Such rectification effect is of great importance due to its relevance to biological ion channels. Moreover, ionic diodes, together with ionic transistors represent the key building blocks for ionic circuits, mimicking voltage-gated ion channels in a variety of biological systems. Several nanofluidic platforms based on nanopores and nanochannels were reported to produce ionic current rectification. Nevertheless, it has not been possible to change the predefined rectifying properties obtained by these approaches once the devices are made. We here report a field effect reconfigurable ionic diode (FERD) by asymmetrically modulating the cation/anion ratios along the nanochannel. A key feature of our device [1]is that it allows the post-fabrication reconfiguration of the diode functions, such as the forward/reverse directions as well as the rectification degrees. These results may lead to the creation of reconfigurable ionic circuits, an ionic counterpart of the electronic field-programmable gate array (FPGA).

Fig. 1 illustrates the schematic FERD structure. The FERD is a three terminal device that has a similar structure to a nanofluidic FET[2], yet with a critical difference that the gate electrode of FERD is asymmetrically located near one of the microfluidic reservoirs. The control devices with gate electrodes sitting symmetrically along the nanochannel were also fabricated on the same silicon wafer. We used a sacrificial layer method to produce the nanochannels (8-20 nm in height). The native surface charge density was found out to be ~-2 mC/m^2 (Fig. 2).

After verifying that the device conductance is indeed governed by the ion transport in the nanochannels (instead of leakage paths), we went on to investigate the field effect tunability of the three-terminal FERD devices using electrical configurations shown in Fig. 3a. The channel current as a function of Cis to Trans voltage (V_{CT}) was measured under various gate voltages (V_G). Fig. 3b shows the representative current-voltage (I-V) curves obtained with V_G of different polarities, using a 100 μM KCl solution. A clear gate voltage controlled rectifying property is observed. On the contrary, no rectifying features are observed for the control device with symmetrically placed gate electrodes (Fig. 3c), which exhibits a symmetric I-V relationship for all V_G polarities (Fig. 3d). We conclude from the comparison that the asymmetric gate location is responsible for the rectifying behavior, a novel mechanism of nanofluidic control that has never been shown before.

To understand the asymmetrical-gate controlled nanofluidic diodes, we developed a qualitative interpretation by looking at the change of the transient drift current of both cations and anions inside the nanochannel immediately after V_{CT} bias is applied with different V_G polarities (Fig. 4a). Furthermore, we carried out the quantitative analysis by concurrently solving the coupled Poisson-Nernst-Planck equations. The calculated concentration profiles under different V_G and V_{CT} polarities are shown in Fig. 4b. The quantitative steady state ion profile in Fig. 4b agrees well with the qualitative transient analysis in Fig. 4a.

The field effect reconfigurable rectifying behavior shows a strong dependence on ionic concentrations. The voltage tunability (i.e., the slope of the R-V_G plot in Fig.5a) of the FERD devices becomes less prominent at both high and low KCl concentrations (Fig. 5). Moreover, the highest rectifying degree at a fixed gate voltage occurs at the intermediate rather than the lowest concentration regime where surface charge governed ion conduction dominates.

To maximize the tunability effect, an ideal structure would be dual split-gates and a sub-10 nm nanochannel of a reduced surface charge. We fabricated devices with a split-gate structure and reduced the nanochannel native surface charge by chemical modification. This device shows a tremendously improved rectification behavior (Fig. 6).

In conclusion, we demonstrated a field effect reconfigurable nanofluidic diode. This general concept could conceivably be applied to similar thin-body solid-state devices. FERD represents a fundamentally novel system and may function as the building block to create an on-demand, reconfigurable, large-scale integrated nanofluidic circuits for digitally-programmed manipulation of biomolecules such as polynucleotides and proteins.

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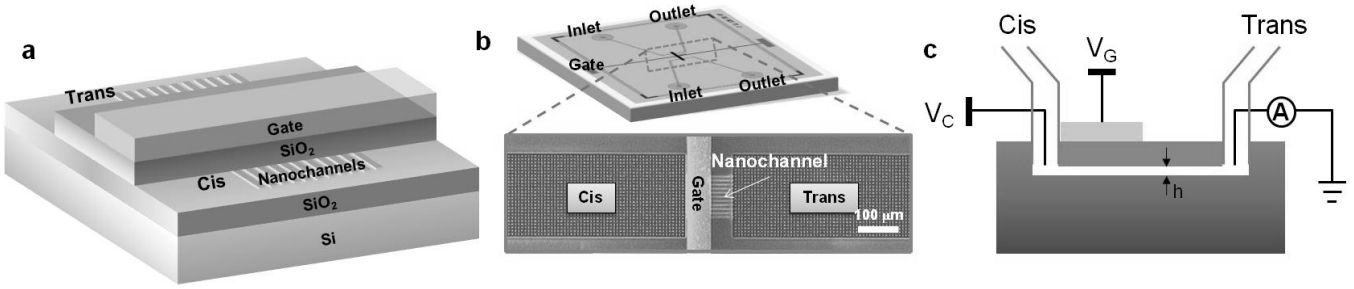

Fig. 1. Device structure and experimental setup. (a) Schematic of the nanofluidic field effect reconfigurable diodes (FERD). (b) Sketch of the planar layout for the assembled device. (c) Schematic of the electrical and fluidic connection configurations.

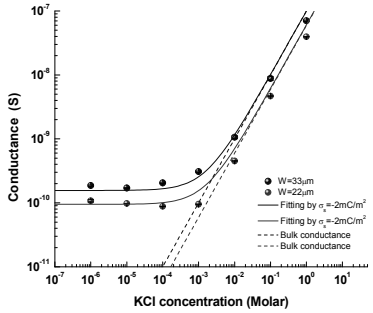

Fig. 2. Measured conductance as a function of KCl concentrations for two devices fabricated using the identical process on a same wafer with gate terminal floating.

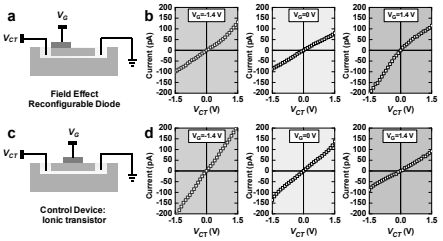

Fig. 3. Current-voltage (I-V) curves for the FERD devices (top row) as well as the control devices (bottom row) with different gate voltage (V_G) polarities.

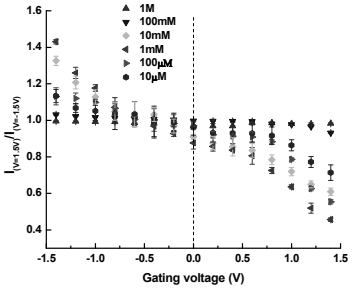

Fig. 4. Effect of the salt concentrations on the rectifying degree under various gate potentials.

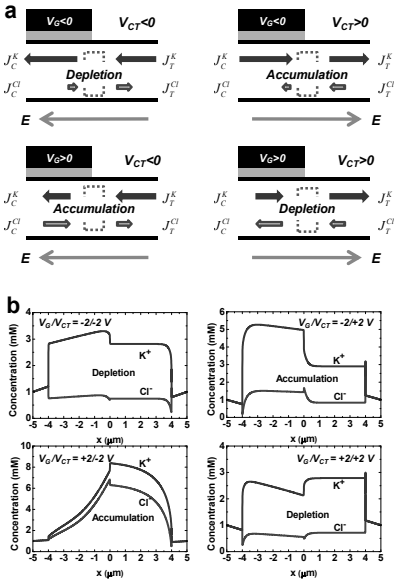

Fig. 5. Qualitative (a) and quantitative (b) analysis of the nanofluidic field effect reconfigurable diodes.

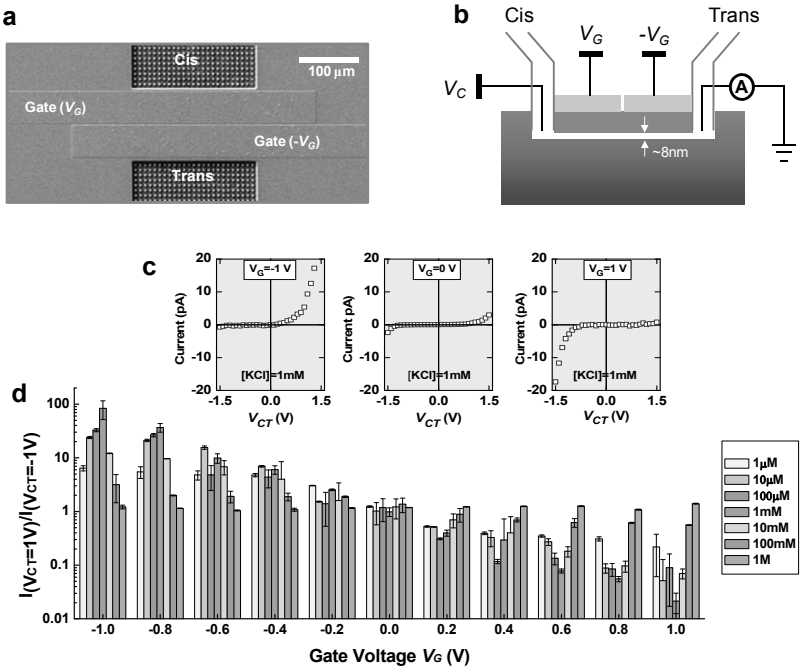

Fig. 6. Improved field effect tunability over the ionic diode property with devices of a dual split-gate structure.

Transparent Diamond-based Electrolyzer for Integration with Solar Cell

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Abstract

Hydrogen generated by photo-induced water electrolysis is considered to be a promising fuel and energy carrier for the future. Such a system contains usually a solar cell and electrolyser for water splitting. Preferably the solar cell material surface should also serve directly as electrolyser. However the semiconductor materials in question (Si, III-V and III.Nitrides) are not highly corrosion resistant in aqueous solutions. Thus, another choice would be to use a solar cell coating as electrolyzer material. However, in general inert materials like Pt are not transparent and metal oxides are limited in their corrosion resistance to the use of specific electrolytes. Thus, the requirements for solar cell and electrolyzer integration are highly conflicting.

In this approach, a transparent and highly corrosion resistant CVD diamond electrode with metallic microdots is evaluated as a possible electrolyzer suitable for vertical integration with a GaN-based solar cell (see fig. 1). GaN may not be the only materials basis for the solar cell part, but is at present the only semiconductor base, which may eventually allow combined growth of the entire material stack [1].

CVD diamond is the only semiconductor material used in harsh environmental electrochemistry like in waste water purification [2]. But at the same time diamond displays a wide potential window for water dissociation of approx. 3.5 V, which is much higher than in the case of metal electrodes like Pt (approx.. 1.8 V), making water splitting rather inefficient. A possible solution could be the deposition of stable metallic microdots, covering only a small fraction of the surface area and thus not affecting the transparency (see fig.2).

For this purpose nanocrystalline diamond (NCD) films have been grown by bias-enhanced nucleation (BEN) on an ultrathin Si/SiC-based interlayer deposited by sputtering onto a sapphire substrate, providing excellent adhesion through covalent bonding. This is followed by outgrowth with hot-filament chemical vapor deposition (HFCVD) to a total thickness of approx. 500 nm with a 300 nm thick boron doped ($P \approx 3x10^{20}$ cm^{-3}) top layer, providing the background electrode conductivity. Ti/Pt microdots of 2 µm in diameter with 40 µm separation (surface coverage approx. 0.3 %) have been deposited and annealed at 650 °C, improving the adhesion of the microdots by interfacial Ti-carbide phase formation. The potential window for water splitting should thus essentially be that of Pt electrodes, but the transparency that of diamond.

Fig. 3 shows such cyclic voltammetry (I-V) measurement of the fabricated electrolyzer in comparison with a Pt electrode and a bare NCD electrode in the mA/cm^2 range. The Ti/Pt microdots lead already to a limited reduction of the onset potential for the hydrogen evolution reaction. But the structure still needs further optimization to reduce the potential window down to that of the Pt-level by optimization of the microdot array and its feed resistances. However, even with the low surface coverage of metallic microdots of only 0.3 %, high current densities and therefore strong hydrogen gas production could be observed, as shown in the micrograph of fig. 4. The current density was approx. 8 mA/cm^2 related to the total electrode surface area, corresponding to approx. 3 A/cm^2 for the microdot area. Assuming that the total current results in hydrogen generation, the above current density corresponds to a hydrogen generation rate of about 0.3 ml/s and cm^2 active electrode area. In this first experiment, no degradation in performance (no detaching of the microdots) was observed during three hours of operation.

The optical transparency of the electrolyzer system is illustrated with fig. 5, showing the transmittance spectrum of, the sapphire/diamond electrolyzer stack in air and that of the stack in the liquid under various levels of H-evolution. The transparency of the electrolyzer in the visible range can be as high as 50 %. Sources for absorption are scattering in the NCD film, absorption due to boron doping and due to remaining Si or SiC nucleation clusters. Further improvements, especially in the UV regime seem however possible (for a first step see fig. 6). Under strong hydrogen evolution, the transparency is significantly reduced further by up to 50 % in the case shown. Thus, additional surface structuring needs to be included for better control of the gas evolution pattern.

In this study a concept of an electrolyzer operating in rather aggressive solutions (and potentially salt water) and with the potential of monolithic integration with a solar cell structure has been presented. The electrolyzer structure is based on a metal dot modified CVD diamond electrode structure grown by HFCVD, a technique which can be scaled to large surface areas. Presently, only the III-Nitride semiconductor materials system seems compatible with the growth conditions required for high-quality NCD electrode material. However, here the incorporation of low bandgap InGaN quantum well structures would be needed, but is still outstanding.

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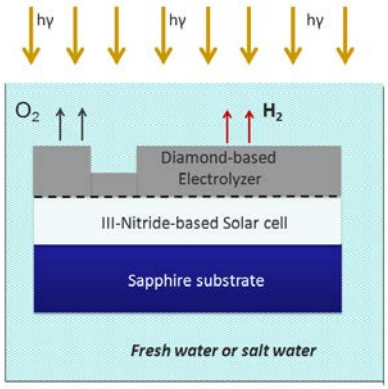

Fig. 1: Concept of a diamond-based electrolyzer integrated with a III-nitride-based solar cell

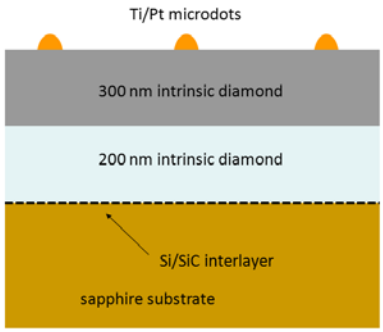

Fig. 2: Diamond-based electrolyzer structure withTi/Pt microdots on transparent sapphire

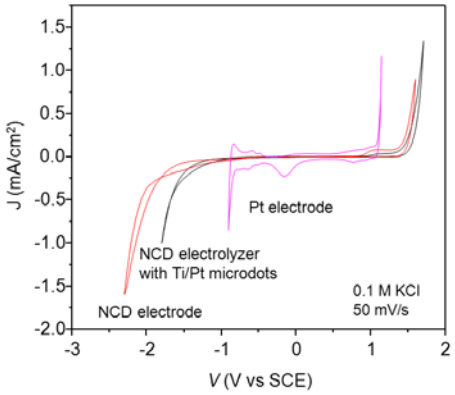

Fig. 3: Cyclic voltammograms of a Pt electrode, a NCD electrode and the NCD electroyzer with Ti/Pt microdots. The water splitting potential window itself is 1.23 eV.

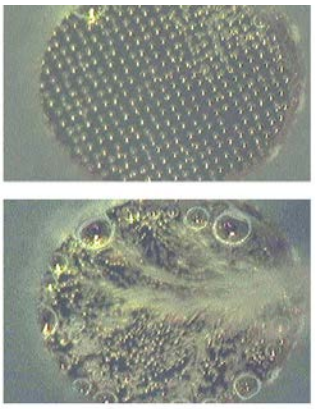

Fig. 4: Hydrogen evolution at the diamond-based electrolyzer with microdots at a bias of ΔV = -3.5 V. Top: Directly after bias switch-on; Bottom: Steady state.

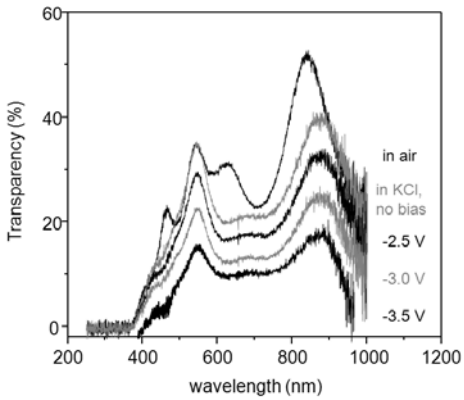

Fig. 5: Optical transparency of NCD electrolyzer in air and in 0.1 M KCl under different bias (hydrogen evolution) conditions. Peaks are due to thin film interferences. Cutoff at 400 nm is due to residual Si/SiC cluster after nucleation

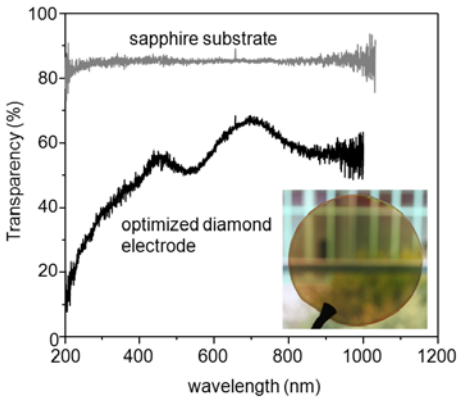

Fig. 6: Optical transparency of NCD electrode with optimized Si/SiC interlayer in air. The diamond adsorption edge is approx.. 225 nm.

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Conference at a Glance

Sunday, June 17, 2012

8:00 AM - 8:30 AM	**Short Course Check-In/Registration**	Conference Registration Desk
8:30 AM – 4:30 PM	**Short Course – Steep Slope Devices**	Room 107
3:00 PM – 6:00 PM	**Conference Check-In/Registration**	Conference Registration Desk
5:00 PM – 6:30 PM	**Opening Reception**	Senate Suites

Monday, June 18, 2012

7:30 AM – 8:20 AM	**Conference Check-In/Registration (continued)**	Conference Registration Desk
8:20 AM - 12:00 PM	**Introductions, Award Presentations, and Plenary Session**	Dean's Hall I & II
12:00 PM – 1:30 PM	**Buffet Lunch** (sponsored by Penn State Outreach)	President's Hall I & II
1:30 PM – 5:10 PM	**Session II.A** CMOS Plus: MEMs, Sensors and Harvestors **Session II.B.** Alternate Transistor Concept	Dean's Hall I Dean's Hall II
5:10 PM – 6:00 PM	**Poster Set-Up** (on display boards)	President's Hall I & II
6:00 PM – 8:30 PM	**Session III.** Poster Session and reception	President's Hall I & II
8:30 PM – 9:00 PM	**Poster Removal** (from display boards)	President's Hall I & II

Tuesday, June 19, 2012

8:20 AM – 12:00 PM	**Session IV.A.** Wide Bandgap/High-Speed Devices **Session IV.A.** 1/2-Dimensional FETs	Dean's Hall I Dean's Hall II
12:00 PM – 1:30 PM	**Buffet Lunch** (sponsored by Penn State Outreach)	President's Hall II
1:30 PM – 5:10 PM	**Session V.A** III-V MOSFETs/TFETs **Session V.B** Spin/Memory	Dean's Hall I Dean's Hall II
5:10 PM – 6:00 PM	**Tour of Millennium Science Building**	Buses – Outside of President's Hall IV
6:30 PM – 8:00 PM	**Conference Banquet**	President's Hall III & IV
8:00 AM – 10:30 PM	**Rump Sessions** **R-1:** Wells vs. Sheets vs. Tubes **R-2:** Compound semiconductors on Si: "A Happy Marriage" or "Keep Your Filthy Materials Out Of My Fab"?	 Senate Suites Senate Suites

Conference at a Glance

Wednesday, June 20, 2012

8:20 AM – 9:20 AM	**Joint DRC/EMC Plenary Session**	Dean's Hall I & II

DRC SESSIONS – Wednesday AM

10:00 AM – 12:00 PM	**Session VI.A** Transistor Modeling **Session VI.B** Thin-Film Devices	Dean's Hall I Dean's Hall II
12:00 PM – 1:30 PM	**Lunch** (on your own)	Restaurants – Ground Floor

EMC SESSIONS – Wednesday AM

Session A	Plenary - Nonpolar and Semipolar GaN Materials and Devices: The Journey so Far
Session B	Group III-Nitrides: Light Emitting Diodes (LEDs)
Session C	Nanowire Devices
Session D	Graphene for Device Applications
Session E	Metameterials and Materials for THz, Plasmonics and Polaritons
Session F	Narrow Bandgap Semiconductor Materials
Session G	Nanoscale Characterization of Electronic Materials

DRC SESSIONS – Wednesday PM

1:30 PM – 3:10 PM	**Session VII.A** Optoelectronic Devices **Session VII.B** Biological Devices	Dean's Hall I Dean's Hall II

EMC SESSIONS – Wednesday PM

Session H	Group III-Nitrides: Transistors
Session I	Compound Semiconductor Nanowires
Session J	Synthesis of Graphene and Carbon Nanotubes
Session K	Oxide Semiconductor Growth, Doping, and Defects
Session L	III-V Semiconductors: Epitaxial Materials and Devices
Session M	Next Generation Solar Cell Materials and Devices I