Engineering Faculty Document No. 4-03
March 13, 2007

TO: The Engineering Faculty
FROM: The Faculty of the School of Electrical and Computer Engineering
RE: New Graduate Level Course: ECE 683

The faculty of the School of Electrical and Computer Engineering has approved the following new course. This action is now submitted to the Engineering Faculty with a recommendation for approval.

ECE 683 Advanced VLSI Design
Sem: Spring. Class: 3; Credit: 3.
Prerequisite: ECE-456, or ECE-559, or consent of instructor.

This is an advanced VLSI course for graduate students. High performance and low-power design issues in modern and future processors will be discussed in detail. There will be a project associated with the course. It is a follow-up course for ECE 559.

Reason: This course is important for the VLSI area and questions for the Qualifying Exam (QE) are taken from this course. It has been offered at least three times in the past with adequate enrollment.

Course History: The course has been offered as the experimental course, 695K, in the fall semesters of 2005, 2003, and 2002 with enrollments of 11, 15, and 8 respectively.

Mark J. T. Smith
Professor and Head

Supporting Documentation

Required Text: None

Recommended References:

1. Low Power CMOS VLSI Circuit Design, Kaushik Roy and Sharat Prasad, Wiley-Interscience, ISBN No. 0-4-71-11488-X.
2. Synthesis and Optimization of Digital Circuits, G De Micheli, McGraw Hill, ISBN No. 0-07-016333-2.
3. Published papers from conferences and journals.

Course Outline:

Lectures	*Principal Topics*
6	**Logic Synthesis:** (1) Two-level (2) Multi-level (3) Timing and layout driven synthesis
12	**High-Performance Design:** (1) High performance logic families like Domino, Noise-tolerance Domino, EDCL, SSDL, DCSL, NORA, etc. (2) Clocking strategies (3) Asynchronous Designs (4) Interconnects
14	**Low-Power Design** (1) Power estimation (2) Ultra low voltage designs (3) Circuit/device/technology issues (4) High level and system level design considerations (5) Interconnects
9	**VLSI Signal Processing:** (1) Multipliers and adders (2) Scheduling and binding of datapaths (3) Low-power design (4) Reconfigurable DSP
3	**Process variation and variation tolerant design**