TO: The Faculty of the College of Engineering

FROM: Elmore Family School of Electrical and Computer Engineering

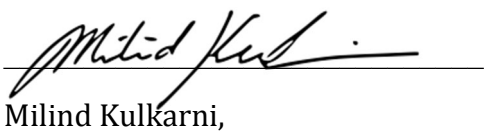
RE: New Graduate Course, ECE 51216 Digital Systems Design Automation

The faculty of the School of Electrical and Computer Engineering has approved the following new course. This action is now submitted to the Engineering Faculty with a recommendation for approval.

ECE 51216 Digital Systems Design Automation
Sem. 2, Lecture 3, Cr. 3.
Prerequisite by Topic: ECE 27000 and ECE 26400 and senior standing, or graduate standing

Description: This course will provide an introduction to the tools used to design and analyze circuits at the logic level of abstraction (where circuits are composed of gates and flip-flops). Most digital chips used in computing and electronic systems (including microprocessors, graphics processors, chips used in network routers, cell phones, digital audio/video appliances, automotive electronics) are entirely or largely designed using EDA tools. This course will focus on the foundations of logic-level EDA tools, including the design of exact and heuristic algorithms that form the basis for VLSI Computer-Aided Design. Topics covered include an overview of the IC design flow and levels of abstraction, synthesis of two-level (AND-OR / PLA) circuits, multi-level logic synthesis and technology mapping, sequential circuit synthesis, Logic-level verification using Boolean Satisfiability and BDDs, Timing Analysis, Power analysis and Reduction, and design techniques for emerging nanoscale technologies.

Reason: Digital integrated circuits used in electronic computing systems (including cell phones, personal computers, servers, wearable devices, network routers and automotive electronics) are entirely or largely designed using Electronic Design Automation (EDA) tools. EDA, which is also referred to as Computer Aided Design (CAD), has been a key enabler to the semiconductor, electronics and computing industries. An understanding of how EDA tools work is essential for IC designers (EDA tool users) who wish to get the most of the tools, as well as to developers of EDA tools. In addition, the algorithms and computational techniques used in EDA tools have found wide applicability in many other application domains.



Milind Kulkarni,
Associate Head for Teaching and Learning
Elmore Family School of Electrical and Computer Engineering

Purdue University
School of Electrical and Computer Engineering
ECE 595Z: Digital Systems Design Automation, Spring 2018
Course Syllabus

Instructor:
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URL: https://engineering.purdue.edu/ECE/People/ptProfile?resource_id=46143

Office Hours: T-Th 1:00PM – 2:00 PM in MSEE 348

Course Description

Digital integrated circuits used in electronic computing systems (including cell phones, personal computers, servers, wearable devices, network routers and automotive electronics) are entirely or largely designed using Electronic Design Automation (EDA) tools. EDA, which is also referred to as Computer Aided Design (CAD), has been a key enabler to the semiconductor, electronics and computing industries. An understanding of how EDA tools work is essential for IC designers (EDA tool users) who wish to get the most of the tools, as well as to developers of EDA tools. In addition, the algorithms and computational techniques used in EDA tools have found wide applicability in many other application domains.

This course provides an introduction to the tools used to design and analyze digital circuits at the logic level of abstraction (where circuits are composed of gates and flip-flops). The course explores EDA tools by abstracting the underlying computational problems and presenting exact and heuristic algorithms that are used to solve them. Topics covered include an overview of the integrated circuit design flow, advanced Boolean algebra, synthesis of two-level circuits, multi-level logic synthesis and technology mapping, sequential circuit synthesis, formal verification, timing analysis and optimization, power analysis and reduction, and design tools for emerging nanoscale technologies.

Text / Reading List

Primary Reading List

- Lecture notes provided as handouts in class or electronically through the course website

Secondary Reading List

- Synthesis and Optimization of Digital Circuits, G. De Micheli, Kluwer Academic Publishers, 2006, ISBN-13 No. 978-0070582781 .
- Logic Synthesis and Verification, G. D. Hachtel and F. Somenzi, Kluwer Academic Publishers, 2006, ISBN-13 No. 978-0387310046.

- Logic Synthesis, S. Devadas, A. Ghosh, K. Keutzer, McGraw-Hill Professional, ISBN-13 No. 978-0070165007, June 1994.

Prerequisites

- ECE 270 and ECE 264 and senior standing, or graduate standing
- Prerequisite by Topic: Digital Logic Design, C or C++ or Java programming, basic familiarity with data structures and algorithms

Grading

The grade will be based on a cumulative score comprised of the following components:

- Homeworks and hands-on assignments – 30%
- Mid-term and/or final exam – 20%
- Course project – 40%
- Participation – 10%

A late submission penalty will be applied to each homework, assignment, or project submission that is received after the specified deadline.

The mapping from cumulative score to the course grade is as follows:

- [90%-100%] – A
- [80% - 90%) – B
- [70% - 80%) – C
- [60% - 70%) – D
- [0% - 60%) – F

The above score ranges for each grade may be modified at the end of each semester based on the score distribution, or to include ranges

Class Schedule

Weeks	Principal Topics
1	Introduction to EDA, Overview of Integrated Circuit (IC) design flow and levels of abstraction in IC design, Quick tour through design automation at the logic level.
1	Advanced Boolean Algebra: Representations of Boolean functions, Operations on Boolean functions, Co-factors and their applications, Unate functions and unate-recursive paradigm
3	Two-level logic synthesis: Re-cap of K-maps and Quine McCluskey method, Covering as a core problem in EDA, Exact and heuristic covering algorithms, Efficient generation of prime implicants, Heuristic two-level synthesis.
3	Multi-level logic synthesis: Boolean networks, Transformations on Boolean networks, Factoring, Algebraic and Boolean division, Kernel-based factoring, Efficient factoring using 0-1 matrices, Satisfiability and

	Observability don't cares, Optimization using don't cares, Technology mapping, Multi-level synthesis in practice.
1	Sequential synthesis: Finite-State Machine Synthesis – State minization and Encoding, Structural sequential optimization with Retiming
1	Timing Analysis: Clocking models for sequential circuits, Delay models for gates, Topological timing analysis, Functional timing analysis and the false path problem.
1	Timing Optimization: Collapsing and Re-structuring, Delay optimizing circuit transforms, Eliminating false paths, Technology mapping for minimum delay.
2	Combinational and Sequential Verification: Equivalence checking and model checking, Binary Decision Diagrams, Efficient function manipulation and analysis using BDDs, Use of BDDs for verification, Boolean Satisfiability Algorithms and Applications to Verification.
2	Low power design - Power estimation, Technology mapping for low power, Clock gating, Power management at the logic level (operand isolation, guarded evaluation and pre-computation)
1	Current topics - Variation-aware design, Design for nanoscale technologies

Academic Dishonesty

Purdue prohibits "dishonesty in connection with any University activity. Cheating, plagiarism, or knowingly furnishing false information to the University are examples of dishonesty." [Part 5, Section III-B-2-a, Student Regulations] Furthermore, the University Senate has stipulated that "the commitment of acts of cheating, lying, and deceit in any of their diverse forms (such as the use of substitutes for taking examinations, the use of illegal cribs, plagiarism, and copying during examinations) is dishonest and must not be tolerated. Moreover, knowingly to aid and abet, directly or indirectly, other parties in committing dishonest acts is in itself dishonest." [University Senate Document 72-18, December 15, 1972].

A useful resource that provides further information is Purdue's student guide for academic integrity (https://www.purdue.edu/odos/academic-integrity/).

Academic dishonesty will result in a penalty that could range from a zero for the assignment or exam question to a failing grade for the course.

Disclaimer

This syllabus is subject to change for reasons that include work-related travel of the instructor and emergencies.

In the event of a major campus emergency, course requirements, deadlines and grading percentages are subject to changes that may be necessitated by a revised semester calendar or other circumstances beyond the instructor's control. Relevant changes to this course will be posted onto the course website or class mailing list.

You are expected to read your @purdue.edu email and view the course website regularly to receive these messages.

See the University's website for additional information: https://www.purdue.edu/ehps/emergency_preparedness/

Addendum: EFD 7-22

Previous offerings of EFD 7-22, Digital Sys Design Automation:

Spr. 20 (33), Spr. 19 (33), Spr. 18 (21), Spring 17 (21), Spr. 15 (28), Spr. 14 (32), Spr. 13 (11), Spr. 12 (18), Spr. 11 (11)