

PURDUE

UNIVERSITY

SCHOOL OF ELECTRICAL
AND COMPUTER ENGINEERING
UNDERGRADUATE ADVISING OFFICE

Engineering Faculty Document 52-20

February 27, 2020

Page 1 of 1

To: The Engineering Faculty
From: School of Electrical and Computer Engineering
Re: ECE 33700

The School of Electrical and Computer Engineering has approved the following changes to an existing course. This action is now submitted to the Engineering Faculty with a recommendation for fast-track approval.

ECE 33700 ASIC Design Laboratory
Semesters offered: Fall, Spring
Non-repeatable
Credit 2

Pre/Co-requisites:
ECE 27000 with a minimum grade of C

FROM:

Course Description

Introduction to standard cell design of VLSI digital circuits using VHDL hardware description language. Emphasis on how to write VHDL that will map readily to hardware. Laboratory experiments using commercial grade computer-aided design (CAD) tools for VHDL based design, schematic based logic entry, logic and VHDL simulation, automatic placement and routing, timing analysis and testing.

TO:

Course Description

Introduction to standard cell design of Application Specific Integrated Circuits (ASICs) using modern hardware description languages (HDLs). Emphasis on how to write HDL code that will map readily to hardware. Laboratory experiments using commercial grade computer-aided design (CAD) tools for HDL based design, logic simulation, automatic placement and routing, timing analysis and verification.

Reason

The course has evolved over the years but the description has never been updated. This will bring it in line with what is actually being taught in the course.

History of Previous Offering

This course has ran for over 15 years and the content has changed to better match technology and degree requirements.



Michael R. Melloch, Associate Department Head of ECE

ASIC Design Laboratory

Syllabus

Instructor: Mark Johnson (mcjohnso@purdue.edu, EE 248, 494-0636)

Spring 2020

1 Course Description and Goals

The primary objective of this course is to provide ASIC (Application Specific Integrated Circuit) design experience through the implementation of subsystems using a Hardware Description Language (HDL). This semester the HDL we will be using is called Verilog. CAD (Computer Aided Design) software will be used to synthesize (create) schematics from HDL code, simulate circuit behavior, automatically generate a physical layout, and verify circuit performance for each design project. A strong emphasis will be placed on how to write HDL code that will translate well into hardware. The course utilizes some of the most common and popular design software used in the ASIC industry. The QuestaSim[®] VHDL/Verilog simulator from Mentor Graphics will be used for HDL and schematic simulation. Synopsis Design Compiler[®] will be used to synthesize a schematic design from HDL code. Innovus from Cadence will be used to generate Integrated Circuit (IC) layouts and verify the timing performance of the IC layout. The first several weeks of the course will consist primarily of lab experiments intended to familiarize you with HDL coding, QuestaSim[®], and Synopsis Design Compiler[®]. Later in the semester you will have design assignments in which you will implement a variety of subsystem designs typical of what would be needed in a large scale "System on chip" (SoC). Near the end of the semester you will practice the use of Innovus to generate a CAD layout needed to fabricate an IC. In the last design assignment you will take a design all the way from logic design to physical layout.

The focus of the lectures will be on helping you understand the ASIC design process, the use of Verilog in designing a module for an ASIC, and many of the decisions and trade-offs you have to make when implementing an ASIC.

2 Course Administration Info

2.1 Lab Website

All course materials will be disseminated via the Blackboard Learn course site.

2.2 Teaching Assistants

- (Lead/Admin TA) Mingxuan He (he238@purdue.edu)
- Lab TAs:
 - Shaunak Oswal (oswals@purdue.edu)

2.3 Text(s) & Required Items

Required Text: Digital Integrated Circuit Design Using Verilog and SystemVerilog by Ronald Mehler © 2015 (electronic access through Purdue Libraries)

Required Item: iClicker student response unit (either iClicker or iClicker2 is acceptable)

Recommended Reference: Digital Design, any edition after the 2nd edition is sufficient, John Wakerly (you should already have from EE270)

2.4 Attendance Policy

Attendance is only strictly mandatory for events and activities necessary to pass the course such as exams and project presentations. However, there are numerous gradable events which take place in lab or lecture for which you will only earn credit if you are present. Those include: clicker participation in lecture, lecture quizzes, in class exercises, in-lab quizzes, and project team briefings with your TA. **Job interviews will not be accepted as a reason to reschedule or miss an exam. You need to keep exam times in mind when scheduling interviews. Extensions on deadlines will not be granted for job interviews.** However, makeups on in-class quizzes, in-class exercises, and clicker participation will be allowed if you notify the instructor in advance.

2.5 Registration Details

Instructor Office Hours: <https://engineering.purdue.edu/~mcjohnso/OfficeHours.pdf>

TA Office Hours: https://calendar.google.com/calendar/embed?src=ilnj2tdotugk6v8pbeq26pve140group.calendar.google.com&ctz=America%2FNew_York

Credit Hours: 2

Table 1: Course Sections

Section	Registrar Section #	Meeting Time
Lecture	015	T 09:30 am-10:20 am
Lab Section 1	002	T 2:30pm-5:20pm
Lab Section 2	004	W 2:30pm-5:20pm
Lab Section 3	008	T 2:30pm-5:20pm
Lab Section 4	009	F 2:30pm-5:20pm

3 Required Objectives (ABET)

In order to pass this course there are certain objectives you must satisfy. In order to be accredited, ECE is required to specify and enforce objectives which are reviewed periodically by accreditation organization known as **ABET**. To satisfy the course objectives you must demonstrate some minimum level of competence in selected areas of your coursework. The objectives are specified as follows:

3.1 ASIC Design Laboratory Course ABET Objectives

1. Design combinational and sequential logic in a variety of styles: schematic, structural, behavioral, and dataflow.
2. Demonstrate and awareness of timing and resource usage associated with each logic design approach.
3. Use, modify, and create scripts to control the logic synthesis process.
4. Create a test bench and use it to verify a design that incorporates multiple sequential blocks.
5. Place, route, and verify timing of an ASIC design.
6. Determine the RTL level architecture implied by HDL code of moderate complexity.
7. Explain the difference between various ASIC and digital system design approaches - standard cell, full custom, and programmable devices.

3.2 Exam based Objectives

Objectives 2, 6, and 7 will be demonstrated primarily by adequate performance on selected test questions during the mid-term exams (1st chance) and the final exam (2nd chance).

3.3 Lab based Objectives

Objectives 1, 3, 4, and 5 will be only be demonstrated through adequate completion of laboratory exercises.

3.3.1 Minimum Completion Requirements for Lab based Objectives

Objective 1 requires you to complete lab 2, by earning at least 70% of the possible points for this lab.

Objective 3 requires you to complete lab 3, by earning at least 70% of the possible points for this lab.

Objective 4 requires you to complete labs 6 and 7, and at least one of labs 8 or 9, by earning at least 50% of the possible points for automated design grading portion of the respective lab.

Objective 5 will be satisfied if you achieve a score of at least 70% on lab 11.

A course objective check-off sheet will be provided for your use in keeping track of meeting all course objectives.

3.3.2 Objectives Remediation

For lab based objectives, you have until two weeks from the original/non-extended lab exercise deadline to remediate the related outcome. These two week periods are inclusive of any holidays or university breaks, and thus the deadlines will not be adjusted or shifted in response to the occurrence of a holiday or university break.

If you are unable to demonstrate your design(s) passing the outcome within this time, you will fail the outcome.

For exam based objectives, you are guaranteed two opportunities to complete the objective. The first opportunity for each objective will be on either the first or second exam during the semester. The second opportunity will be on the final exam.

3.4 Warnings

1. Satisfying only these minimum objectives does not guarantee that you will pass, but **failure to achieve these objectives guarantees that you will fail.**

2. If you have any confusion or questions regarding the Objectives, please contact your professor or teaching assistant for further clarifications. Please make absolutely sure that you satisfy all the lab and lecture Objectives before the end of the semester.

4 Collaboration Rules

Under no circumstances is source code sharing allowed, except for when explicitly stated in coursework requirements/directions.

Unless explicitly stated in the directions/requirements for an assignment/exercise, all course work is to be done individually. When collaboration is explicitly allowed/required the following rules apply:

- You are strictly limited to current ASIC Design Lab students as collaborators.
- The only *code* you may share is non-synthesizable test bench code.
- You may discuss with each other how you coded parts of your design, but when writing you must not copy, refer to, or transcribe (such as having someone read or message to you) another person's code.
- You are encouraged to collaborate on debugging, but any corrections must be made by you.
- In order to gain points on a lab that allows collaboration you must submit a collaboration form, with the name of each person you collaborated with, with a general idea of the topic of collaboration. Also if you choose not to collaborate you must still submit a form stating no collaborators.
- Code that is similar to someone you did not list as a collaborator will be investigated by the course staff and may be considered a violation of academic honesty policy. Even between your collaborators, *copying code* will be a violation.

5 Lab Structure

5.1 Lab Schedule

The weekly lab sessions are organized week by week as given in Table 2. Topics in given can change, but very little change is expected.

Table 2: Lab Schedule

Week #	Week of	Lab #	Lab Foundational Topic(s)	Lab Mastery Topic(s)
1	1/13	1	Intro to Verilog, Design Flow, & 270 Refresher	
2	1/20	2	Extendable Logic Design	Exhaustive Testing
3	1/27	3	Non-Exhaustive Testing, Coverage Analysis, & Synthesis Tuning	Assertions, Debugging, & Test Vectors
4	2/3	4	Synchronous Logic Design and Testing & RTL Diagramming	Verification Tasks
5	2/10	5	Serial Communication Basics & FSM Design	Data-Streaming Tasks
6	2/17	6	Intro to Serial Communication Protocols (UART)	
7	2/24	7	Math Algorithms in HW (Convolution & FIR Filter)	
8	3/2	8	Multi-Cycle SoC Bus Protocols (APB-Accessible UART Receiver)	
9	3/9	9	Pipelined SoC Bus Protocols (AHB-Lite FIR Filter Accelerator)	
10	3/16		Spring Break	
11	3/23	10	IC Layout Tutorial	IC Layout Area Tuning
12	3/30	11	IC Layout Process Analysis, Cooperative Design Lab Design Planning	IC Critical Timing Tuning
13	4/6	12	Cooperative Design Lab Design Planning	Design Planning Demo Due in Lab
14	4/13	12	Cooperative Design Lab Implementation	
15	4/20	12	Cooperative Design Lab Verification	
16	4/27	12	Cooperative Design Lab Completion (Demos & Report)	

5.2 General Notes Regarding Lab Sessions

- All lab handouts will be available on the course website or distributed by your lab instructor.
- Collaboration (limited to the extent specified in Section 4) is only allowed for the Cooperative Design Lab. All other labs are *individual* work, and any collaboration during these labs is considered academic dishonesty.
- MG accounts used for the course are accessible by the course staff.

5.3 Lab Session Format

Most lab periods for the first twelve weeks will begin with a meeting in the conference room in the lab. That is when your TA will distribute materials, discuss class business, and explain lab requirements. The remaining time is designated for you to work on lab exercise and project work. *All labs are individual work unless specified otherwise.*

5.4 Lab Attendance

Prior to the Cooperative Design Lab, lab attendance is not graded, but do not expect leniency if you miss important information or a quiz at the beginning of lab. If you miss a lab session (except for a posted "open lab") for any reason, discuss this with your TA. When the Cooperative Design Lab is in progress, you will be expected to attend lab to meet with your team and to review progress on your project with the TA. Participation in progress briefings will factor into your project grade.

5.5 Lab Work

Lab exercises will be a mixture of CAE tool tutorials and design planning, implementation, and verification work. In some lab exercises, you will have to complete design planning work that will be used as the starting point for implementation during a subsequent lab exercise. For this reason (as well as for legibility and generally good design practice) all design planning work must be completed via digital means such as diagramming tools like Dia, Visio, Draw.IO and LibreDraw for all diagramming and schematic work and www.wavedrom.com for all timing waveform work. No hand-drawn/hand-written work will be accepted for grading for lab exercise and project related work. Furthermore, all lab exercise and project related work must be version controlled via at least a local Git repository in your course account (which will be setup during lab 1).

5.6 Lab Deadlines

All lab exercises are due as part of the pre-lab for the following lab session. If you need your pre-lab work to complete the next lab, you must make a copy for yourself before turning the original. The original will not be returned to you until it has been graded. Pre-lab and prior week's work must be handed at the beginning of lab during the opening discussion. Any items requiring demonstration to a TA or lab assistant must be signed off by that time.

There is an opportunity for partial late credit on all lab exercises except lab 12 (Cooperative Design Lab). **For labs 1 through 5, 10, and 11, you are allowed one 'late lab' where you may choose to take a 10% grading penalty on the entirety of that lab in exchange for a 1 week extension for that lab.** You must notify your lab TA in advance (before the regular deadline has passed) that you are wanting to use your 'late lab'. Once used for a lab, the 'late lab' option is irrevocable, and thus you cannot change your decision to use it for a different lab. **For labs 6-9, late credit is only available for electronic submission portions of the exercises. You will receive 75% of the points from the late electronic submission if done within one week of its regular deadline, and 50% if completed within the 2nd week.** No points will be given for remediated sign-offs.

Please be diligent in doing your work on time. If you have a serious problem that merits an extension, discuss this with Dr. Johnson as soon as possible. Any class-wide changes regarding deadlines will be announced by the course staff in the announcement section in Blackboard.

If you are experiencing flu symptoms, DO NOT come to class, lab, and DO NOT come to see your instructor in person. Instead, notify Dr. Johnson and your TA as soon as possible via email or telephone. We will work with you to determine a schedule for completion of your work. Unless extreme circumstances make this impossible, if you fail to notify us within seven calendar days of the deadline affected by your illness you will forfeit the right to the make up the missed work

Any extensions must be approved by one of the course instructor(s) or head TA. Furthermore, what is changed for one lab section will not carry over to the others unless you are specifically informed by the course staff.

5.7 Lab Submission

Electronic Submission

A substantial portion of your lab work will be submitted electronically and your designs will be tested automatically. Consequently, it is essential that you follow specifications for file names and input/output signal names. Failure to do this may cause a "correct" design to fail all tests and get a very poor grade. There will be no lab

regrading because of faulty file names and/or input/output signal names, unless told otherwise by course staff. Electronic submissions are due by the start of your next lab session, unless otherwise announced by the course staff.

Lab Evaluation Sheet

Lab evaluation forms for the week's lab must be signed off by a TA before the beginning of the your next designated lab session, unless otherwise announced by the course staff. Make sure that your TA records the score from your evaluation sheet in your presence before you leave. The TA will NOT keep your evaluation sheet. He or she will merely record the score and give the sheet back to you. It is your responsibility to keep your evaluation sheet until your score is posted on blackboard.

6 Lecture Structure

6.1 Lecture Format

The primary use of the lecture time will be for the explanation of concepts needed for your lab work. However, lecture times could also include unannounced quizzes, in-class design exercises, question/answer sessions, invited speakers, and exams. Lecture attendance is not mandatory, but absences could result in zeros on quizzes or in-class exercises that you miss. Student response units (i.e., clickers) will be used during most lectures. Part of your homework and quiz grade for the semester will include points for your participation using the clickers. Except when announced, your clicker responses will NOT be graded for correctness, just for participation.

6.2 Quizzes

Quizzes will be given during lecture or opening discussion in lab that cover the material presented during the lectures, included in a reading assignment, or practiced in lab. Quizzes will not always be announced.

6.3 Exams

In-class exams are one of the means that will be used to verify that you have met required course objectives. They will also serve to check your learning of topics not directly practiced in the lab. Finally, exams and quizzes will both help to differentiate between project partners who understand what they are doing and those who do not. A person who completes an assignment or project, but shortly after that knows very little about how it was done will be suspect. There will be two mid-terms and an optional final exam. If you are failing any exam objectives, this is your last guaranteed opportunity to satisfy these objectives. If you are doing poorly on midterm exams, this is also an opportunity to improve your exam average. You will have the choice of answering just the outcome questions (solely to pass the outcomes) or you can complete the entire make-up to replace your worst exam score of the semester. The percentage of the total grade given to exams has been deliberately kept low because the bulk of your work in this course will be on the lab work.

7 Course Grading

7.1 Grading Category Weights

Quizzes, Homework, Lecture Exercises, & Clicker Use:	5%
Exams (mid-terms):	30%
Lab Assignments (labs 1-5, 10, & 11):	15%
Design Assignments (labs 6-9):	25%
Cooperative Design Lab:	25%
– Technical Accomplishment:	15%
– Documentation:	5%
– Demonstration:	5%

A few things should be noted:

- Lab assignments account for 65% of your grade, so do not take them lightly.
- You are responsible for your choice of Cooperative Design Lab partners, so choose wisely.
- If it is clear that a partner has contributed little or nothing to a Cooperative Design Lab, they will be penalized. However, that does not absolve the rest of team of their responsibility completing the Cooperative Design Lab.

7.2 Overall Grading Scale

Following are the criteria for the assignment of letter grades:

A+:	96% and above	C+:	77-78.9%
A:	91-95.9%	C:	71-76.9%
A-:	89-90.9%	C-:	69-70.9%
B+:	87-88.9%	D+:	67-68.9%
B:	81-86.9%	D:	61-66.9%
B-:	79-80.9%	D-:	59-60.9%
		F:	Below 59% or failing an objective

7.3 Regrade Requests

Regrade requests must be made and submitted to your TA or instructor no later than one week after the assignment was handed back to you. No regrade request will be accepted after that.

8 Academic Honesty

Purdue's Academic Honesty Pledge:

As a Boilermaker pursuing academic excellence, I pledge to be honest and true in all that I do. Accountable together - we are Purdue. [<https://www.purdue.edu/provost/teachinglearning/honor-pledge.html>]

As with other courses here at Purdue, cheating is not tolerated. In this course any form of cheating will result in a zero for that assignment and may result in failure of the course. In severe cases, academic action will also be taken up with the ECE department. The act of cheating includes (but is not limited to) turning in another student's work as your own, allowing someone to turn in your work, falsifying any lab checkoff sheets. Discussing your designs with other students will not be considered cheating provided that what you submit is your own work.

Automated and manual checking of your design files will be used to identify cases of plagiarism. It will be considered plagiarism even if what you submit only contains fragments of another person's work or fragments of your own work show up in someone else's work. In addition, current student's work will be checked against designs from prior semesters. If part of your design is based on some publicly available example (such as from a textbook or the web), you are expected to include a comment giving credit to the source with enough information for your TA to look up the example. In fact, failure to give credit constitutes a misrepresentation of your work and would be considered plagiarism. The use of any source files from previous semesters will result in a zero.

Use of online repositories:

If you wish to make your work visible to potential employers, do it with a private repository. If other students find your work and use it as part of their own (even after you have finished this course), you will be implicated in an academic dishonesty incident. The incident report to the Office of the Dean of Students (ODOS) will identify the person providing the information as well as the person using the information. Even after you graduate, it is not in your interest for ODOS to have academic dishonesty incidents on file.

Intellectual property rights to course materials:

All learning materials provided for this class or notes derived from these materials are the intellectual property of your instructor and/or Purdue University. As such, they cannot be sold or bartered without the express written permission of your instructor nor can they be disseminated to anyone other than current students of the class. This includes posting to websites, databased, or inclusion in public repositories.

Student Reports of Academic Dishonesty:

Purdue University provides official channels for reports of student dishonesty. If you observe instances of academic dishonesty, you are encouraged to report the incident to the Office of the Dean of Students (purdue.edu/odos) either in person, by calling 765-494-8778, or by emailing integrity@purdue.edu

Self-reporting of Academic Dishonesty Encouraged:

If you commit an act of academic dishonesty, it is in your best interest to notify the course instructor within a timely fashion after the incident rather than be caught by course staff. Penalties are always at the discretion of the instructor, but the consequences are usually less severe for a student who self-reports than for a student whose action is discovered by course staff.

9 Rules for Students Retaking the Course

If a student has taken the course before (Withdraw/Fail/Incomplete) and wants to retake this course. The following are the policies:

- Only student's own individual work from prior semester can be reused and resubmitted.
- Cooperative Design Lab work from a prior semester may not be reused or resubmitted (unless all students from the same team in prior semester are retaking and form the team together again).

- When a student reuses their previous lab work they must improve their grade for the assignment in order to earn any credit for it, unless they previously had received at least 80% of the maximum grade for that work.

10 Laboratory Room Rules

Violators' names will be noted and reported to ECN. Repeat offenders may face restricted computer privileges and/or other disciplinary actions.

Food: Neither food nor drink are permitted near any of the computer equipment. There is one exception. Drink bottles which do not spill easily are permitted. I.e., if one can invert the bottle without liquid coming out, it qualifies.

Computer Hogs: Simultaneous use of more than one computer by the same person or locking the screen and leaving for more than 10 minutes is inconsiderate towards other users. Those who do this will have their running processes killed to free the machine for other users.

Lab Access Priorities: Class in session gets the first priority for access to workstation. TA on duty gets priority to use one workstation. In all other cases, access is first come first served.

Music and Other Noise: Be considerate to other people in the lab. Use headphones if you want to listen to music. Keep conversation down to a reasonable level.

Trash: Do not leave trash behind at your workstation, this includes scrap/scratch paper and other items you brought with you or used and no longer want.

10.1 Lab access outside of scheduled class times

EE 61 Unlimited access as long as the EE building is open (very nearly 24x7). When a class is in session, students in that class have priority for access to the workstations.

EE 132, EE 206, EE 207, EE 215 Unlimited access as long as the building is open (very nearly 24x7) and the room is not reserved for another course's lab or office hours session. In general, EE 132, EE 206, EE 207, and EE 215 are scheduled so as to keep at least one open for unscheduled use at most times.

Remote Access Compute servers that permit remote access to desktop sessions are available. Details for access will be provided via the course Blackboard site.

11 Emergency Procedures

In the event of a major campus emergency, course requirements, deadlines and grading percentages are subject to changes that may be necessitated by a revised semester calendar or other circumstances beyond the instructor's control. If a campus shutdown is announced by Purdue University officials, a course announcement will be posted in the Blackboard discussion groups and a Blackboard email message will be emailed to the entire class with instructions. You may also reach course staff at the phone numbers and email addresses listed at the top of this document.

In the event of an emergency while in class or lab, a copy of the following emergency instructions poster should be visible near the telephone. Please refer to it for instructions on how to proceed.

http://www.purdue.edu/epps/emergency_preparedness/flipchart/index.html

12 Other Student Resources

Commitment to Nondiscrimination Purdue University is committed to maintaining a community which recognizes and values the inherent worth and dignity of every person; fosters tolerance, sensitivity, understanding, and mutual respect among its members; and encourages each individual to strive to reach his or her own potential. In pursuit of its goal of academic excellence, the University seeks to develop and nurture diversity. The University believes that diversity among its many members strengthens the institution, stimulates creativity, promotes the exchange of ideas, and enriches campus life. Purdue's nondiscrimination policy can be found at http://www.purdue.edu/purdue/ea_eou_statement.html.

Mental Health Support: Purdue University is committed to advancing the mental health and well-being of its students. If you or someone you know is feeling overwhelmed, depressed, and/or in need of support, services are available. For help, such individuals should contact Counseling and Psychological Services (CAPS) at (765) 494-6995 and <http://www.purdue.edu/caps/> during and after hours, on weekends and holidays, or through its counselors physically located in the Purdue University Student Health Center (PUSH) during business hours.

Disability Accommodations: Purdue University strives to make learning experiences as accessible as possible. If you anticipate or experience physical or academic barriers based on disability, you are welcome to let me know so that we can discuss options. You are also encouraged to contact the Disability Resource Center at: drc@purdue.edu or by phone: 765-494-1247. Students may present a "Letter of Accommodation" to the instructor at any point in the semester, but a minimum of one week advance notice will be required to provide accommodations for any exam or other course activity.

