# PURDUE UNIVERSITY
REQUEST FOR ADDITION, EXPIRATION,
OR REVISION OF AN UNDERGRADUATE COURSE
(10000-40000 LEVEL)

**DEPARTMENT** School of Electrical and Computer Engineering (EFD 51-11)
**EFFECTIVE SESSION** Spring 2012

**INSTRUCTIONS:** Please check the items below which describe the purpose of this request.

- New course with supporting documents
- Add existing course offered at another campus
- Expiration of a course
- Change in course number
- Change in course title
- Change in course credit/type
- Change in course attributes (department head signature only)
- Change in instructional hours
- Change in course description
- Change in course requisites
- Change in semesters offered (department head signature only)
- Transfer from one department to another

**PROPOSED:**

- **Subject Abbreviation:** ECE
- **Course Number:** 41438
- **Long Title:** ASIC Fab and Test II
- **Short Title:** ASIC Fab and Test II

**EXISTING:**

- Subject Abbreviation
- Course Number
- Long Title
- Short Title

**Abbreviated title will be entered by the Office of the Registrar if omitted. (30 CHARACTERS ONLY)**

**CREDIT TYPE**

<table>
<thead>
<tr>
<th>Credit Type</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed Credit: Cr. Hrs.</td>
<td>2</td>
</tr>
<tr>
<td>Variable Credit Range: Minimum Cr. Hrs.</td>
<td>(Check One)</td>
</tr>
<tr>
<td>Variable Credit Range: Maximum Cr. Hrs.</td>
<td></td>
</tr>
<tr>
<td>Equivalent Credit: Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

**COURSE TYPE**

- Pass/Not Pass Only
- Satisfactory/Unsatisfactory Only
- Repeatable
- Maximum Repeatable Credit:
- Credit by Examination
- Special Fees
- Instructor
- Full Time Privilege
- Off Campus Experience

**Course Attributes**

**TERM OFFERED**

- Summer
- Fail
- Spring

**CAMPUS(ES) INVOLVED**

- Calumet
- N. Central
- Cont Ed
- Tech Statewide
- Ft. Wayne
- Indianapolis
- W. Lafayette

**Credit Type**

- Lecture
- Recitation
- Presentation
- Laboratory
- Lab Prep
- Studio
- Distance
- Clinic
- Experiential
- Research
- Ind. Study
- Pract/Observe

**COURSE DESCRIPTION (INCLUDE REQUISITES/RESTRICTIONS):**

See attached.

**COURSE LEARNING OUTCOMES:**

See attached.

**Signature**

Office of the Registrar

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**Calumet Department Head**
Date: 8/25/11

**Calumet School Dean**
Date:

**Fort Wayne Department Head**
Date:

**Fort Wayne School Dean**
Date:

**Indianapolis Department Head**
Date:

**Indianapolis School Dean**
Date:

**North Central Department Head**
Date:

**North Central Chancellor**
Date:

**West Lafayette Department Head**
Date:

**West Lafayette College/School Dean**
Date:

**West Lafayette Registrar**
Date:

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**OFFICE OF THE REGISTRAR**
School of Electrical and Computer Engineering (EFD 51-11)

Description:
The second semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC, having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL, Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

Prerequisite: ECE 41437 and Departmental Approval

Restrictions: Must be enrolled in the School of Electrical and Computer Engineering

Course Learning Outcomes:

A student who successfully fulfills the course requirements will have demonstrated:

i. Create testbenches and verify the functionality of the design in source code after logic synthesis and after layout. [4; e,k]

ii. Create an ASIC layout that is verified and ready for fabrication. [3; c,k]

iii. Design, implement, and use a hardware testbed for verification of functionality and performance of the chip after fabrication. Use a reconfigurable logic prototype for early testing and in lieu of a fabricated custom IC if necessary. [4; c,e,k]

iv. Communicate effectively by means of an oral presentation of the project either to students in another course or at a technical conference. [6; g]

v. Communicate effectively in writing by means of a collective technical report on the project and individual reports on how each outcome was satisfied. [6; g]
TO: The Faculty of the College of Engineering
FROM: The Faculty of the School of Electrical and Computer Engineering
RE: New Undergraduate Courses: ECE 41437 ASIC Fabrication and Test I and ECE 41438 ASIC Fabrication and Test II

The faculty of the School of Electrical and Computer Engineering has approved the following new courses. This action is now submitted to the Engineering Faculty with a recommendation for approval.

**ECE 41437 ASIC Fabrication and Test I**
Sem. Fall, Cr. 2, Lecture 1, Lab 1
**Prerequisites:** ECE 33700 and Departmental Approval
**Restrictions:** Must be enrolled in the School of Electrical and Computer Engineering
**Description:** The first semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

**ECE 41438 ASIC Fabrication and Test II**
Sem. Spring, Cr. 2, Lecture 1, Lab 1
**Prerequisites:** ECE 41437 and Departmental Approval
**Restrictions:** Must be enrolled in the School of Electrical and Computer Engineering
**Description:** The second semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

**Reason:** This course allows students to gain practical experience with the design and testing of an ASIC (Application Specific Integrated Circuit) using industry standard tools. In addition, formalizing the course with a permanent number is needed to sustain industrial support for the course. The courses have previously been offered experimentally as ECE 49500 in Fall 2006, Spring 2007, Fall 2007, Spring 2008, Fall 2008, Spring 2009, Fall 2009, Spring 2010, and Fall 2010, Spring 2011 with an average enrollment of 3 for each course.

On behalf of V. Balakrishnan, Head

APPROVED FOR THE FACULTY OF THE SCHOOLS OF ENGINEERING BY THE ENGINEERING CURRICULUM COMMITTEE

ECC Minutes 5
Date 10/17/11
Chairman ECC R. Cipra
ECE 41438 - ASIC Fabrication and Test II

Lecture Hours: 1.0 Lab Hours: 1.0 Credits: 2.0

Requisites:
ECE 41437 and Departmental Approval.

Catalog Description:
The second semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results. In the event that chip fabrication is unavailable, a reconfigurable logic based prototype may be tested instead. The instructor will meet weekly with each design team to monitor progress, explain new concepts, and guide the team in satisfying all course outcomes.

Supplemental Information:
In the event that chip fabrication is unavailable, a reconfigurable logic based prototype may be tested instead. The instructor will meet weekly with each design team to monitor progress, explain new concepts, and guide the team in satisfying all course outcomes.

Required Text(s): None.

Recommended Text(s):


Course Outcomes:

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ECE 41438 ASIC Fabrication and Test II
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Restrictions: Must be enrolled in the School of Electrical and Computer Engineering
Description: The second semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL (VHSIC (very high speed integrated circuit) Hardware Description Language), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

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on behalf of M. Balakrishnan, Head
Supporting Documentation EFD 51-11

Assessment Method for Course Outcomes: Any completed outcomes (1-7) will be assessed through evaluation of each students outcome completion report (described in outcome 8), corroborated by instructor observation during the semester, and by an end of semester interview. Outcome 8 will be assessed grading of the collective technical report and the individual outcome completion report.

Lab Outline:

<table>
<thead>
<tr>
<th>Lab</th>
<th>Activity</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Verify functionality and manufacturability of the layout (if not completed in semester 1)</td>
</tr>
<tr>
<td>2</td>
<td>Submit design for Fabrication (if fabrication is possible)</td>
</tr>
<tr>
<td>3-12</td>
<td>Design and implement a hardware testbed</td>
</tr>
<tr>
<td>5-14</td>
<td>Test functionality and performance of ASIC and/or reconfigurable logic implementation</td>
</tr>
<tr>
<td>13-15</td>
<td>Prepare a testing report to be submitted to the organization that provided funds or wafer space for fabrication of the design (if fabrication is possible)</td>
</tr>
<tr>
<td>4-12</td>
<td>Prepare a paper and/or poster for submission to selected engineering education conference. If conference presentation isn't possible, give presentation to another ECE course.</td>
</tr>
<tr>
<td>13-15</td>
<td>Final Report</td>
</tr>
</tbody>
</table>

Final Exam Week. End of semester interview.

Engineering Design Content:

Analysis
Construction
Testing
Evaluation

Engineering Design Consideration(s):

Manufacturability
School of Electrical and Computer Engineering (EFD 51-11)

Description:

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Course Learning Outcomes:

A student who successfully fulfills the course requirements will have demonstrated:

i. Explain critical steps in the preparation of an ASIC design for fabrication and the tools required to perform these steps: functional verification, logic synthesis, physical layout, physical verification, and timing verification. (ALL individually). [3; k]

ii. an ability to use advanced ASIC design software for at least 2 of the following: functional verification, logic synthesis, physical layout, physical verification, and timing verification. Create or use scripts to automate repetitive aspects of the process. [3; k]

iii. an ability to define functional and physical requirements for an ASIC design of the team's choosing. [4; c,e]

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v. an ability to estimate speed, throughput, and expected circuit area to ensure that constraints are satisfied.. [4; c]

vi. an ability to create testbenches and verify the functionality of the design in source code, and after logic synthesis.. [4; e,k]

vii. an ability to communicate effectively in writing by means of a collective technical report on the project and individual reports on how each outcome was satisfied.. [6; g]
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Prerequisite: ECE 41437 and Departmental Approval

Restrictions: Must be enrolled in the School of Electrical and Computer Engineering

Course Learning Outcomes:

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**REQUEST FOR ADDITION, EXPIRATION, OR REVISION OF AN UNDERGRADUATE COURSE**

### DEPARTMENT
School of Electrical and Computer Engineering (EFD 51-11)

### EFFECTIVE SESSION
Fall 2011

### INSTRUCTIONS:
Please check the items below which describe the purpose of this request.

1. [ ] New course with supporting documents  
2. [ ] Add existing course offered at another campus  
3. [ ] Expulsion of a course  
4. [ ] Change in course number  
5. [ ] Change in course title  
6. [ ] Change in course credit/type  
7. [ ] Change in course attributes (department head signature only)  
8. [ ] Change in Instructional hours  
9. [ ] Change in course description  
10. [ ] Change in course prerequisites  
11. [ ] Change in semesters offered (department head signature only)  
12. [ ] Transfer from one department to another

### PROPOSED:

<table>
<thead>
<tr>
<th>Subject Abbreviation</th>
<th>ECE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Course Number</td>
<td>41437</td>
</tr>
<tr>
<td>Long Title</td>
<td>ASIC Fab and Test I</td>
</tr>
<tr>
<td>Short Title</td>
<td>ASIC Fab and Test I</td>
</tr>
</tbody>
</table>

**Abbreviated title will be entered by the Office of the Registrar if omitted. (max characters only)**

### CREDIT TYPE

<table>
<thead>
<tr>
<th>Type</th>
<th>Fixed Credit</th>
<th>Cr. Hrs.</th>
<th>Variable Credit Range</th>
<th>Minimum Cr. Hrs.</th>
<th>(Check One)</th>
<th>Or</th>
<th>Maximum Cr. Hrs.</th>
<th>Yes</th>
<th>No</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.</td>
<td></td>
<td></td>
<td>Equivalent Credit:</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### CREDIT HOURS

<table>
<thead>
<tr>
<th>Type</th>
<th>Minutes</th>
<th>Meetings</th>
<th>Per 5-Mtg</th>
<th>Per Week</th>
<th>Weeks Offered</th>
<th>% of Credit Allocated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lecture</td>
<td>50</td>
<td>1</td>
<td></td>
<td></td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>Recitation</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Presentation</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Laboratory</td>
<td>100</td>
<td>2</td>
<td></td>
<td></td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>Lab Prep</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Studio</td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>Distance</td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Clinic</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Experiential</td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>Research</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ind. Study</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Prac/Observ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### COURSE ATTRIBUTES:

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Check All That Apply</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### COURSE DESCRIPTION (INCLUDE REQUISITES/RESTRICTIONS):

See attached.

### COURSE LEARNING OUTCOMES:

See attached.

### TERMS OFFERED

- [ ] Summer  
- [X] Fall  
- [ ] Spring

### CAMPUS(ES) INVOLVED

- [ ] Calumet  
- [ ] Cont Ed  
- [ ] Ft. Wayne  
- [ ] Indianapolis  
- [X] W. Lafayette

### Cross-Listed Courses

**RECEIVED BY THE REGISTRAR OCT 26 AM 9:45**
TO: The Faculty of the College of Engineering

FROM: The Faculty of the School of Electrical and Computer Engineering

RE: New Undergraduate Courses: ECE 41437 ASIC Fabrication and Test I and ECE 41438 ASIC Fabrication and Test II

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Sem. Fall, Cr. 2, Lecture 1, Lab 1
Prerequisites: ECE 33700 and Departmental Approval
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ECE 41438 ASIC Fabrication and Test II
Sem. Spring, Cr. 2, Lecture 1, Lab 1
Prerequisites: ECE 41437 and Departmental Approval
Restrictions: Must be enrolled in the School of Electrical and Computer Engineering
Description: The second semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC very high speed integrated circuit) Hardware Description Language), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

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[Signature]

on behalf of V. Balakrishnan, Head

APPROVED FOR THE FACULTY OF THE SCHOOLS OF ENGINEERING BY THE ENGINEERING CURRICULUM COMMITTEE

ECC Minutes #5
Date 10/17/11
Chairman ECC R. Cipra
ECE 41437 - ASIC Fabrication and Test I

Lecture Hours: 1.0 Lab Hours: 1.0 Credits: 2.0

Requisites:
ECE 337

Catalog Description:
The first semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

Supplementary Information:
In the event that chip fabrication is unavailable, a reconfigurable logic based prototype may be tested instead. The instructor will meet weekly with each design team to monitor progress, explain new concepts, and guide the team in satisfying all course outcomes.

Required Text(s): None.

Recommended Text(s):


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Assessment Method for Course Outcomes: Any completed outcomes (1-7) will be assessed through evaluation of each student's outcome completion report (described in outcome 8), corroborated by instructor observation during the semester, and by an end of semester interview. Outcome 8 will be assessed grading of the collective technical report and the individual outcome completion report.

Lab Outline:

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<thead>
<tr>
<th>Lab</th>
<th>Activity</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-2</td>
<td>Define Design Requirements and Constraints</td>
</tr>
<tr>
<td>3-6</td>
<td>Define Chip Architecture</td>
</tr>
<tr>
<td>5-10</td>
<td>Prepare design using a hardware description language</td>
</tr>
<tr>
<td>8-12</td>
<td>Synthesize design to gate level representation</td>
</tr>
<tr>
<td>6-12</td>
<td>Prepare Simulation Test Benches</td>
</tr>
<tr>
<td>8-14</td>
<td>Verify functionality of source code and gate level design</td>
</tr>
<tr>
<td>12-14</td>
<td>Prepare ASIC Layout. Might not complete until second semester.</td>
</tr>
<tr>
<td>13-14</td>
<td>Verify functionality and manufacturability of the layout. Might not complete until second semester.</td>
</tr>
<tr>
<td>15</td>
<td>Submit design for Fabrication (if fabrication is available). Might not complete until second semester.</td>
</tr>
</tbody>
</table>

Engineering Design Content:

Establishment of Objectives and Criteria
Synthesis
Analysis
Construction
Testing
Evaluation

Engineering Design Consideration(s):

Manufacturability
ECE 41438 - ASIC Fabrication and Test II

Lecture Hours: 1.0 Lab Hours: 1.0 Credits: 2.0

Requisites:
ECE 41437 and Departmental Approval.

Catalog Description:
The second semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results. In the event that chip fabrication is unavailable, a reconfigurable logic based prototype may be tested instead. The instructor will meet weekly with each design team to monitor progress, explain new concepts, and guide the team in satisfying all course outcomes.

Supplemental Information:
In the event that chip fabrication is unavailable, a reconfigurable logic based prototype may be tested instead. The instructor will meet weekly with each design team to monitor progress, explain new concepts, and guide the team in satisfying all course outcomes.

Required Text(s): None.

Recommended Text(s):


Course Outcomes:

A student who successfully fulfills the course requirements will have demonstrated:

i. Create testbenches and verify the functionality of the design in source code after logic synthesis and after layout. [4; e,k]

ii. Create an ASIC layout that is verified and ready for fabrication. [3; c,k]

iii. Design, implement, and use a hardware testbed for verification of functionality and performance of the chip after fabrication. Use a reconfigurable logic prototype for early testing and in lieu of a fabricated custom IC if necessary. [4; c,e,k]

iv. Communicate effectively by means of an oral presentation of the project either to students in another course or at a technical conference. [6; g]

v. Communicate effectively in writing by means of a collective technical report on the project and individual reports on how each outcome was satisfied. [6; g]
**Assessment Method for Course Outcomes:** Any completed outcomes (1-7) will be assessed through evaluation of each students outcome completion report (described in outcome 8), corroborated by instructor observation during the semester, and by an end of semester interview. Outcome 8 will be assessed grading of the collective technical report and the individual outcome completion report.

**Lab Outline:**

<table>
<thead>
<tr>
<th>Lab</th>
<th>Activity</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NOTE: Exact schedule is determined based on status of project at the end of the prior semester. It also depends on the schedule of the fabrication vendor. Week 1 will prepare complete ASIC layout (if not completed in semester 1)</td>
</tr>
<tr>
<td>1</td>
<td>Verify functionality and manufacturability of the layout (if not completed in semester 1)</td>
</tr>
<tr>
<td>2</td>
<td>Submit design for Fabrication (if fabrication is possible)</td>
</tr>
<tr>
<td>3-12</td>
<td>Design and implement a hardware testbed</td>
</tr>
<tr>
<td>5-14</td>
<td>Test functionality and performance of ASIC and/or reconfigurable logic implementation</td>
</tr>
<tr>
<td>13-15</td>
<td>Prepare a testing report to be submitted to the organization that provided funds or wafer space for fabrication of the design (if fabrication is possible)</td>
</tr>
<tr>
<td>4-12</td>
<td>Prepare a paper and/or poster for submission to selected engineering education conference. If conference presentation isn't possible, give presentation to another ECE course.</td>
</tr>
<tr>
<td>13-15</td>
<td>Final Report</td>
</tr>
<tr>
<td></td>
<td>Final Exam Week. End of semester interview.</td>
</tr>
</tbody>
</table>

**Engineering Design Content:**

Analysis  
Construction  
Testing  
Evaluation

**Engineering Design Consideration(s):**

Manufacturability
School of Electrical and Computer Engineering (EFD 51-11)

Description:

The first semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL (VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

Prerequisite: ECE 33700 and Departmental Approval

Restrictions: Must be enrolled in the School of Electrical and Computer Engineering

Course Learning Outcomes:

A student who successfully fulfills the course requirements will have demonstrated:

i. Explain critical steps in the preparation of an ASIC design for fabrication and the tools required to perform these steps: functional verification, logic synthesis, physical layout, physical verification, and timing verification. (ALL individually). [3; k]

ii. an ability to use advanced ASIC design software for at least 2 of the following: functional verification, logic synthesis, physical layout, physical verification, and timing verification. Create or use scripts to automate repetetive aspects of the process. [3; k]

iii. an ability to define functional and physical requirements for an ASIC design of the team's choosing. [4; c,e]

iv. an ability to define a circuit architecture that can be expected meet functional requirements subject to performance and area constraints. [4; c,e]

v. an ability to estimate speed, throughput, and expected circuit area to ensure that constraints are satisfied. [4; c]

vi. an ability to create testbenches and verify the functionality of the design in source code, and after logic synthesis. [4; e,k]

vii. an ability to communicate effectively in writing by means of a collective technical report on the project and individual reports on how each outcome was satisfied. [6; g]
School of Electrical and Computer Engineering (EFD 51-11)

Description:
The second semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

Prerequisite: ECE 41437 and Departmental Approval

Restrictions: Must be enrolled in the School of Electrical and Computer Engineering

Course Learning Outcomes:

A student who successfully fulfills the course requirements will have demonstrated:

i. Create testbenches and verify the functionality of the design in source code after logic synthesis and after layout. [4; e,k]

ii. Create an ASIC layout that is verified and ready for fabrication. [3; c,k]

iii. Design, implement, and use a hardware testbed for verification of functionality and performance of the chip after fabrication. Use a reconfigurable logic prototype for early testing and in lieu of a fabricated custom IC if necessary. [4; c,e,k]

iv. Communicate effectively by means of an oral presentation of the project either to students in another course or at a technical conference. [6; g]

v. Communicate effectively in writing by means of a collective technical report on the project and individual reports on how each outcome was satisfied. [6; g]
**REQUEST FOR ADDITION, EXPIRATION, OR REVISION OF AN UNDERGRADUATE COURSE**

**DEPARTMENT:** School of Electrical and Computer Engineering (EFD 51-11)

**EFFECTIVE SESSION:** Spring 2012

**INSTRUCTIONS:** Please check the items below which describe the purpose of this request.

- [X] New course with supporting documents
- [ ] Add existing course offered at another campus
- [ ] Expiration of a course
- [ ] Change in course number
- [ ] Change in course title
- [ ] Change in course credit/type
- [ ] Change in course attributes (department head signature only)
- [ ] Change in instructional hours
- [ ] Change in course description
- [ ] Change in course prerequisites
- [ ] Change in semesters offered (department head signature only)
- [ ] Transfer from one department to another

**PROPOSED:**

<table>
<thead>
<tr>
<th>Subject Abbreviation</th>
<th>Course Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECE</td>
<td>41438</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Long Title</th>
<th>ASIC Fab and Test II</th>
</tr>
</thead>
</table>

**EXISTING:**

<table>
<thead>
<tr>
<th>Subject Abbreviation</th>
<th>Course Number</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Short Title</th>
<th>ASIC Fab and Test II</th>
</tr>
</thead>
</table>

**TERMS OFFERED:**

<table>
<thead>
<tr>
<th>Check All That Apply</th>
<th>Summer</th>
<th>Fall</th>
<th>Spring</th>
</tr>
</thead>
</table>

**CAMPUS(ES) INVOLVED:**

- Calumet
- Cont Ed
- Pt. Wayne
- Indianapolis
- W. Lafayette

**CREDIT TYPE:**

1. Fixed Credit: Cr. Hrs.
2. Variable Credit Range:
   - Minimum Cr. Hrs.
   - Maximum Cr. Hrs.

**Equivalency Credit:**

- Yes
- No

**COURSE Attributes:**

1. Pass/Not Pass Only
2. Satisfactory/Unsatisfactory Only
3. Repeatable
4. Credit by Examination
5. Special Fees
6. Registration Approval Type
   - Department
   - Instructor
7. Variable Title
8. Honors
9. Full Time Privilege
10. Off-Campus Experience

**COURSE DESCRIPTION (INCLUDE REQUISITES/RESTRICTIONS):**

See attached.

**COURSE LEARNING OUTCOMES:**

See attached.

**Cross-Listed Courses:**

- [ ]
- [ ]
- [ ]

**Calumet Department Head**

**Calumet School Dean**

**Fort Wayne Department Head**

**Fort Wayne School Dean**

**Indianapolis Department Head**

**Indianapolis School Dean**

**North Central Department Head**

**North Central Chancellor**

**West Lafayette Department Head**

**West Lafayette College/School Dean**

**West Lafayette Registrar**

**OFFICE OF THE REGISTRAR**
Form 40 attachment

School of Electrical and Computer Engineering (EFD 51-11 )

Description:
The second semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC, having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL, Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

Prerequisite: ECE 41437 and Departmental Approval

Restrictions: Must be enrolled in the School of Electrical and Computer Engineering

Course Learning Outcomes:

A student who successfully fulfills the course requirements will have demonstrated:

i. Create testbenches and verify the functionality of the design in source code after logic synthesis and after layout. [4; e,k]

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