Office of the Registrar
FORM 40 REV. 11/09

PURDUE UNIVERSITY
REQUEST FOR ADDITION, EXPIRATION,
OR REVISION OF AN UNDERGRADUATE COURSE
(10000-40000 LEVEL)

Print Form

EFD 51-11

DEPARTMENT School of Electrical and Computer Engineering (EFD 51-11) EFFECTIVE SESSION Spring 2012

INSTRUCTIONS: Please check the items below which describe the purpose of this request.

- [X] 1. New course with supporting documents
- [ ] 2. Add existing course offered at another campus
- [ ] 3. Expiration of a course
- [ ] 4. Change in course number
- [ ] 5. Change in course title
- [ ] 6. Change in course credit/type
- [ ] 7. Change in course attributes (department head signature only)
- [ ] 8. Change in instructional hours
- [ ] 9. Change in course description
- [ ] 10. Change in course requisites
- [ ] 11. Change in semesters offered (department head signature only)
- [ ] 12. Transfer from one department to another

PROPOSED:		EXISTING:	
Subject Abbreviation	ECE	Subject Abbreviation	
Course Number	41438	Course Number	
Long Title	ASIC Fab and Test II		
Short Title	ASIC Fab and Test II		

Abbreviated title will be entered by the Office of the Registrar if omitted. (30 CHARACTERS ONLY)

TERMS OFFERED
Check All That Apply:
[ ] Summer [ ] Fall [X] Spring

CAMPUS(ES) INVOLVED
[ ] Calumet [ ] N. Central
[ ] Cont Ed [ ] Tech Statewide
[ ] Ft. Wayne [X] W. Lafayette
[ ] Indianapolis

CREDIT TYPE
1. Fixed Credit: Cr. Hrs. 2
2. Variable Credit Range: Minimum Cr. Hrs
(Check One) To [ ] Or [ ]
Maximum Cr. Hrs.
3. Equivalent Credit: Yes [ ] No [ ]

COURSE ATTRIBUTES: Check All That Apply
1. Pass/Not Pass Only [ ]
2. Satisfactory/Unsatisfactory Only [ ]
3. Repeatable [ ]
Maximum Repeatable Credit: [ ]
4. Credit by Examination [ ]
5. Special Fees [ ]
6. Registration Approval Type
Department [X] Instructor [ ]
7. Variable Title [ ]
8. Honors [ ]
9. Full Time Privilege [ ]
10. Off Campus Experience [ ]

ScheduleType	Minutes Per Mtg	Meetings Per Week	Weeks Offered	% of Credit Allocated
Lecture	50	1	16	
Recitation				
Presentation				
Laboratory	100	2	16	
Lab Prep				
Studio				
Distance				
Clinic				
Experiential				
Research				
Ind. Study				
Pract/Observ				

Cross-Listed Courses

RECEIVED
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OFFICE OF THE REGISTRAR

COURSE DESCRIPTION (INCLUDE REQUISITES/RESTRICTIONS):
See attached.

*COURSE LEARNING OUTCOMES:
See attached.

	Date		Date
Calumet Department Head		Calumet School Dean	
Fort Wayne Department Head		Fort Wayne School Dean	
Indianapolis Department Head		Indianapolis School Dean	
North Central Department Head		North Central Chancellor	
West Lafayette Department Head	8/25/11	West Lafayette College/School Dean	11/16/2011
		West Lafayette Registrar	11/23/11

OFFICE OF THE REGISTRAR

11/21/11

Form 40 attachment

School of Electrical and Computer Engineering (EFD 51-11)

Description:

The second semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC, having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL, Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

Prerequisite: ECE 41437 and Departmental Approval

Restrictions: Must be enrolled in the School of Electrical and Computer Engineering

Course Learning Outcomes:

A student who successfully fulfills the course requirements will have demonstrated:

i. Create testbenches and verify the functionality of the design in source code after logic synthesis and after layout. [4; e,k]
ii. Create an ASIC layout that is verified and ready for fabrication.. [3; c,k]
iii. Design, implement, and use a hardware testbed for verification of functionality and performance of the chip after fabrication. Use a reconfigurable logic prototype for early testing and in lieu of a fabricated custom IC if necessary.. [4; c,e,k]
iv. Communicate effectively by means of an oral presentation of the project either to students in another course or at a technical conference.. [6; g]
v. Communicate effectively in writing by means of a collective technical report on the project and individual reports on how each outcome was satisfied.. [6; g]

ECE 41438

TO: The Faculty of the College of Engineering

FROM: The Faculty of the School of Electrical and Computer Engineering

RE: New Undergraduate Courses: ECE 41437 ASIC Fabrication and Test I and ECE 41438 ASIC Fabrication and Test II

The faculty of the School of Electrical and Computer Engineering has approved the following new courses. This action is now submitted to the Engineering Faculty with a recommendation for approval.

ECE 41437 **ASIC Fabrication and Test I**
Sem. Fall, Cr. 2, Lecture 1, Lab 1
Prerequisites: ECE 33700 and Departmental Approval
Restrictions: Must be enrolled in the School of Electrical and Computer Engineering
Description: The first semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

ECE 41438 **ASIC Fabrication and Test II**
Sem. Spring, Cr. 2, Lecture 1, Lab 1
Prerequisites: ECE 41437 and Departmental Approval
Restrictions: Must be enrolled in the School of Electrical and Computer Engineering
Description: The second semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

Reason: This course allows students to gain practical experience with the design and testing of an ASIC (Application Specific Integrated Circuit) using industry standard tools. In addition, formalizing the course with a permanent number is needed to sustain industrial support for the course. The courses have previously been offered experimentally as ECE 49500 in Fall 2006, Spring 2007, Fall 2007, Spring 2008, Fall 2008, Spring 2009, Fall 2009, Spring 2010, and Fall 2010, Spring 2011 with an average enrollment of 3 for each course.

Jeffrey L. Gray
on behalf of V. Balakrishnan, Head

APPROVED FOR THE FACULTY
OF THE SCHOOLS OF ENGINEERING
BY THE ENGINEERING
CURRICULUM COMMITTEE

ECC Minutes #5

Date 10/17/11

Chairman ECC R. Cipra

ECE 41438

Supporting Documentation EFD 51-11

ECE 41438 - ASIC Fabrication and Test II

Lecture Hours: 1.0 Lab Hours: 1.0 Credits: 2.0

Requisites:
ECE 41437 and Departmental Approval.

Catalog Description:
The second semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results. In the event that chip fabrication is unavailable, a reconfigurable logic based prototype may be tested instead. The instructor will meet weekly with each design team to monitor progress, explain new concepts, and guide the team in satisfying all course outcomes.

Supplemental Information:
In the event that chip fabrication is unavailable, a reconfigurable logic based prototype may be tested instead. The instructor will meet weekly with each design team to monitor progress, explain new concepts, and guide the team in satisfying all course outcomes.

Required Text(s): None.

Recommended Text(s):

1. *VHDL for Logic Synthesis*, 2nd Edition, Andrew Rushton, John Wiley & Sons, 1998, ISBN No. 047198325x.

Course Outcomes:

A student who successfully fulfills the course requirements will have demonstrated:

i. Create testbenches and verify the functionality of the design in source code after logic synthesis and after layout. [4; e,k]
ii. Create an ASIC layout that is verified and ready for fabrication.. [3; c,k]
iii. Design, implement, and use a hardware testbed for verification of functionality and performance of the chip after fabrication. Use a reconfigurable logic prototype for early testing and in lieu of a fabricated custom IC if necessary.. [4; c,e,k]
iv. Communicate effectively by means of an oral presentation of the project either to students in another course or at a technical conference.. [6; g]
v. Communicate effectively in writing by means of a collective technical report on the project and individual reports on how each outcome was satisfied.. [6; g]

ECE 41438

TO: The Faculty of the College of Engineering

FROM: The Faculty of the School of Electrical and Computer Engineering

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ECE 41438 **ASIC Fabrication and Test II**
Sem. Spring, Cr. 2, Lecture 1, Lab 1
Prerequisites: ECE 41437 and Departmental Approval
Restrictions: Must be enrolled in the School of Electrical and Computer Engineering
Description: The second semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

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J. Z. Gray
on behalf of V. Balakrishnan, Head

APPROVED FOR THE FACULTY
OF THE SCHOOLS OF ENGINEERING
BY THE ENGINEERING
CURRICULUM COMMITTEE

ECC Minutes #5

Date 10/17/11

Chairman ECC R. Cipra

Assessment Method for Course Outcomes: Any completed outcomes (1-7) will be assessed through evaluation of each students outcome completion report (described in outcome 8), corroborated by instructor observation during the semester, and by an end of semester interview. Outcome 8 will be assessed grading of the collective technical report and the individual outcome completion report.

Lab Outline:

Lab	Activity
	NOTE: Exact schedule is determined based on status of project at the end of the prior semester. It also depends on the schedule of the fabrication vendor. Week 1 will prepare complete ASIC layout (if not completed in semester1)
1	Verify functionality and manufacturability of the layout (if not completed in semester 1)
2	Submit design for Fabrication (if fabrication is possible)
3-12	Design and implement a hardware testbed
5-14	Test functionality and performance of ASIC and/or reconfigurable logic implementation
13-15	Prepare a testing report to be submitted to the organization that provided funds or wafer space for fabrication of the design (if fabrication is possible)
4-12	Prepare a paper and/or poster for submission to selected engineering education conference. If conference presentation isn't possible, give presentation to another ECE course.
13-15	Final Report
	Final Exam Week. End of semester interview.

Engineering Design Content:

Analysis
Construction
Testing
Evaluation

Engineering Design Consideration(s):

Manufacturability

ECE 41438

Form 40 attachment

School of Electrical and Computer Engineering (EFD 51-11)

Description:

The first semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

Prerequisite: ECE 33700 and Departmental Approval

Restrictions: Must be enrolled in the School of Electrical and Computer Engineering

Course Learning Outcomes:

A student who successfully fulfills the course requirements will have demonstrated:

i. Explain critical steps in the preparation of an ASIC design for fabrication and the tools required to perform these steps: functional verification, logic synthesis, physical layout, physical verification, and timing verification. (ALL individually). [3; k]
ii. an ability to use advanced ASIC design software for at least 2 of the following: functional verification, logic synthesis, physical layout, physical verification, and timing verification. Create or use scripts to automate repetetive aspects of the process. [3; k]
iii. an ability to define functional and physical requirements for an ASIC design of the team's choosing. [4; c,e]
iv. an ability to define a circuit architecture that can be expected meet functional requirements subject to performance and area constraints. [4; c,e]
v. an ability to estimate speed, throughput, and expected circuit area to ensure that constraints are satisfied.. [4; c]
vi. an ability to create testbenches and verify the functionality of the design in source code, and after logic synthesis.. [4; e,k]
vii. an ability to communicate effectively in writing by means of a collective technical report on the project and individual reports on how each outcome was satisfied.. [6; g]

ECE 41438

Form 40 attachment

School of Electrical and Computer Engineering (EFD 51-11)

Description:

The second semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

Prerequisite: ECE 41437 and Departmental Approval

Restrictions: Must be enrolled in the School of Electrical and Computer Engineering

Course Learning Outcomes:

A student who successfully fulfills the course requirements will have demonstrated:

i. Create testbenches and verify the functionality of the design in source code after logic synthesis and after layout. [4; e,k]
ii. Create an ASIC layout that is verified and ready for fabrication.. [3; c,k]
iii. Design, implement, and use a hardware testbed for verification of functionality and performance of the chip after fabrication. Use a reconfigurable logic prototype for early testing and in lieu of a fabricated custom IC if necessary.. [4; c,e,k]
iv. Communicate effectively by means of an oral presentation of the project either to students in another course or at a technical conference.. [6; g]
v. Communicate effectively in writing by means of a collective technical report on the project and individual reports on how each outcome was satisfied.. [6; g]

Office of the Registrar
FORM 40 REV. 11/09

PURDUE UNIVERSITY
REQUEST FOR ADDITION, EXPIRATION,
OR REVISION OF AN UNDERGRADUATE COURSE
(10000-40000 LEVEL)

Print Form

EFD 51-11

DEPARTMENT School of Electrical and Computer Engineering (EFD 51-11) EFFECTIVE SESSION ~~Fall 2011~~ (20120)

INSTRUCTIONS: Please check the items below which describe the purpose of this request.

- [X] 1. New course with supporting documents
- [ ] 2. Add existing course offered at another campus
- [ ] 3. Expiration of a course
- [ ] 4. Change in course number
- [ ] 5. Change in course title
- [ ] 6. Change in course credit/type
- [ ] 7. Change in course attributes (department head signature only)
- [ ] 8. Change in instructional hours
- [ ] 9. Change in course description
- [ ] 10. Change in course requisites
- [ ] 11. Change in semesters offered (department head signature only)
- [ ] 12. Transfer from one department to another

PROPOSED:		EXISTING:	
Subject Abbreviation	ECE	Subject Abbreviation	
Course Number	41437	Course Number	
Long Title	ASIC Fab and Test I		
Short Title	ASIC Fab and Test I		

Abbreviated title will be entered by the Office of the Registrar if omitted. (30 CHARACTERS ONLY)

TERMS OFFERED
Check All That Apply:
[ ] Summer [X] Fall [ ] Spring

CAMPUS(ES) INVOLVED
[ ] Calumet [ ] N. Central
[ ] Cont Ed [ ] Tech Statewide
[ ] Ft. Wayne [X] W. Lafayette
[ ] Indianapolis

CREDIT TYPE
1. Fixed Credit: Cr. Hrs. 2
2. Variable Credit Range: Minimum Cr. Hrs ____ (Check One) To [ ] Or [ ]
Maximum Cr. Hrs. ____
3. Equivalent Credit: Yes [ ] No [ ]

COURSE ATTRIBUTES: Check All That Apply
1. Pass/Not Pass Only [ ]
2. Satisfactory/Unsatisfactory Only [ ]
3. Repeatable [ ]
Maximum Repeatable Credit: [ ]
4. Credit by Examination [ ]
5. Special Fees [ ]
6. Registration Approval Type: Department [X] Instructor [ ]
7. Variable Title [ ]
8. Honors [ ]
9. Full Time Privilege [ ]
10. Off Campus Experience [ ]

ScheduleType	Minutes Per Mtg	Meetings Per Week	Weeks Offered	% of Credit Allocated
Lecture	50	1	16	
Recitation				
Presentation				
Laboratory	100	2	16	
Lab Prep				
Studio				
Distance				
Clinic				
Experiential				
Research				
Ind. Study				
Pract/Observ				

Cross-Listed Courses

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EFD 51-11

COURSE DESCRIPTION (INCLUDE REQUISITES/RESTRICTIONS):
See attached.

*COURSE LEARNING OUTCOMES:
See attached.

Calumet Department Head	Date	Calumet School Dean	Date
Fort Wayne Department Head	Date	Fort Wayne School Dean	Date
Indianapolis Department Head	Date	Indianapolis School Dean	Date
North Central Department Head	Date	North Central Chancellor	Date
West Lafayette Department Head	8/5/11 Date	West Lafayette College/School Dean	10/24/11 Date
		West Lafayette Registrar	Sandra Schaffer 10/30/11 Date

OFFICE OF THE REGISTRAR

10/28/11

ECE 41437

~~Engineering Faculty~~ No. 51-11
February 14, 2011

TO: The Faculty of the College of Engineering

FROM: The Faculty of the School of Electrical and Computer Engineering

RE: New Undergraduate Courses: ECE 41437 ASIC Fabrication and Test I and ECE 41438 ASIC Fabrication and Test II

The faculty of the School of Electrical and Computer Engineering has approved the following new courses. This action is now submitted to the Engineering Faculty with a recommendation for approval.

ECE 41437 **ASIC Fabrication and Test I**
Sem. Fall, Cr. 2, Lecture 1, Lab 1
Prerequisites: ECE 33700 and Departmental Approval
Restrictions: Must be enrolled in the School of Electrical and Computer Engineering
Description: The first semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

ECE 41438 **ASIC Fabrication and Test II**
Sem. Spring, Cr. 2, Lecture 1, Lab 1
Prerequisites: ECE 41437 and Departmental Approval
Restrictions: Must be enrolled in the School of Electrical and Computer Engineering
Description: The second semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

Reason: This course allows students to gain practical experience with the design and testing of an ASIC (Application Specific Integrated Circuit) using industry standard tools. In addition, formalizing the course with a permanent number is needed to sustain industrial support for the course. The courses have previously been offered experimentally as ECE 49500 in Fall 2006, Spring 2007, Fall 2007, Spring 2008, Fall 2008, Spring 2009, Fall 2009, Spring 2010, and Fall 2010, Spring 2011 with an average enrollment of 3 for each course.

on behalf of V. Balakrishnan, Head

APPROVED FOR THE FACULTY
OF THE SCHOOLS OF ENGINEERING
BY THE ENGINEERING
CURRICULUM COMMITTEE

ECC Minutes #5

Date 10/17/11

Chairman ECC R. Cipra

ECE 41437

ECE 41437 - ASIC Fabrication and Test I

Lecture Hours: 1.0 Lab Hours: 1.0 Credits: 2.0

Requisites:
ECE 337

Catalog Description:
The first semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

Supplementary Information:
In the event that chip fabrication is unavailable, a reconfigurable logic based prototype may be tested instead. The instructor will meet weekly with each design team to monitor progress, explain new concepts, and guide the team in satisfying all course outcomes.

Required Text(s): None.

Recommended Text(s):

1. *Digital Integrated Circuits*, 2nd Edition, Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, Prentice -Hall, 2003, ISBN No. 0130909963.
2. *VHDL for Logic Synthesis*, 2nd Edition, Andrew Rushton, John Wiley & Sons, 1998, ISBN No. 047198325x.

Course Outcomes:

A student who successfully fulfills the course requirements will have demonstrated:

i. Explain critical steps in the preparation of an ASIC design for fabrication and the tools required to perform these steps: functional verification, logic synthesis, physical layout, physical verification, and timing verification. (ALL individually). [3; k]
ii. an ability to use advanced ASIC design software for at least 2 of the following: functional verification, logic synthesis, physical layout, physical verification, and timing verification. Create or use scripts to automate repetetive aspects of the process. [3; k]
iii. an ability to define functional and physical requirements for an ASIC design of the team's choosing. [4; c,e]
iv. an ability to define a circuit architecture that can be expected meet functional requirements subject to performance and area constraints. [4; c,e]
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vi. an ability to create testbenches and verify the functionality of the design in source code, and after logic synthesis.. [4; e,k]

vii. an ability to communicate effectively in writing by means of a collective technical report on the project and individual reports on how each outcome was satisfied.. [6; g]

Assessment Method for Course Outcomes: Any completed outcomes (1-7) will be assessed through evaluation of each students outcome completion report (described in outcome 8), corroborated by instructor observation during the semester, and by an end of semester interview. Outcome 8 will be assessed grading of the collective technical report and the individual outcome completion report.

Lab Outline:

Lab	Activity
1-2	Define Design Requirements and Constraints
3-6	Define Chip Architecture
5-10	Prepare design using a hardware description language
8-12	Synthesize design to gate level representation
6-12	Prepare Simulation Test Benches
8-14	Verify functionality of source code and gate level design
12-14	Prepare ASIC Layout. Might not complete until second semester.
13-14	Verify functionality and manufacturability of the layout. Might not complete until second semester.
15	Submit design for Fabrication (if fabrication is available). Might not complete until second semester.

Engineering Design Content:

Establishment of Objectives and Criteria
Synthesis
Analysis
Construction
Testing
Evaluation

Engineering Design Consideration(s):

Manufacturability

ECE 41437

Supporting Documentation EPD 51-11

ECE 41438 - ASIC Fabrication and Test II

Lecture Hours: 1.0 Lab Hours: 1.0 Credits: 2.0

Requisites:
ECE 41437 and Departmental Approval.

Catalog Description:
The second semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results. In the event that chip fabrication is unavailable, a reconfigurable logic based prototype may be tested instead. The instructor will meet weekly with each design team to monitor progress, explain new concepts, and guide the team in satisfying all course outcomes.

Supplemental Information:
In the event that chip fabrication is unavailable, a reconfigurable logic based prototype may be tested instead. The instructor will meet weekly with each design team to monitor progress, explain new concepts, and guide the team in satisfying all course outcomes.

Required Text(s): None.

Recommended Text(s):

1. *VHDL for Logic Synthesis*, 2nd Edition, Andrew Rushton, John Wiley & Sons, 1998, ISBN No. 047198325x.

Course Outcomes:

A student who successfully fulfills the course requirements will have demonstrated:

i. Create testbenches and verify the functionality of the design in source code after logic synthesis and after layout. [4; e,k]
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iii. Design, implement, and use a hardware testbed for verification of functionality and performance of the chip after fabrication. Use a reconfigurable logic prototype for early testing and in lieu of a fabricated custom IC if necessary.. [4; c,e,k]
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Lab Outline:

Lab	Activity
	NOTE: Exact schedule is determined based on status of project at the end of the prior semester. It also depends on the schedule of the fabrication vendor. Week 1 will prepare complete ASIC layout (if not completed in semester1)
1	Verify functionality and manufacturability of the layout (if not completed in semester 1)
2	Submit design for Fabrication (if fabrication is possible)
3-12	Design and implement a hardware testbed
5-14	Test functionality and performance of ASIC and/or reconfigurable logic implementation
13-15	Prepare a testing report to be submitted to the organization that provided funds or wafer space for fabrication of the design (if fabrication is possible)
4-12	Prepare a paper and/or poster for submission to selected engineering education conference. If conference presentation isn't possible, give presentation to another ECE course.
13-15	Final Report
	Final Exam Week. End of semester interview.

Engineering Design Content:

Analysis
Construction
Testing
Evaluation

Engineering Design Consideration(s):

Manufacturability

ECE 41437

~~Form 40 attachment~~

School of Electrical and Computer Engineering (EFD 51-11)

Description:

The first semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

Prerequisite: ECE 33700 and Departmental Approval

Restrictions: Must be enrolled in the School of Electrical and Computer Engineering

Course Learning Outcomes:

A student who successfully fulfills the course requirements will have demonstrated:

i. Explain critical steps in the preparation of an ASIC design for fabrication and the tools required to perform these steps: functional verification, logic synthesis, physical layout, physical verification, and timing verification. (ALL individually). [3; k]
ii. an ability to use advanced ASIC design software for at least 2 of the following: functional verification, logic synthesis, physical layout, physical verification, and timing verification. Create or use scripts to automate repetetive aspects of the process. [3; k]
iii. an ability to define functional and physical requirements for an ASIC design of the team's choosing. [4; c,e]
iv. an ability to define a circuit architecture that can be expected meet functional requirements subject to performance and area constraints. [4; c,e]
v. an ability to estimate speed, throughput, and expected circuit area to ensure that constraints are satisfied.. [4; c]
vi. an ability to create testbenches and verify the functionality of the design in source code, and after logic synthesis.. [4; e,k]
vii. an ability to communicate effectively in writing by means of a collective technical report on the project and individual reports on how each outcome was satisfied.. [6; g]

ECE 41437

School of Electrical and Computer Engineering (EFD 51-11)

Description:

The second semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC (Application Specific Integrated Circuit), having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL ((VHSIC (very high speed integrated circuit) Hardware Description Language)), Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

Prerequisite: ECE 41437 and Departmental Approval

Restrictions: Must be enrolled in the School of Electrical and Computer Engineering

Course Learning Outcomes:

A student who successfully fulfills the course requirements will have demonstrated:

i. Create testbenches and verify the functionality of the design in source code after logic synthesis and after layout. [4; e,k]
ii. Create an ASIC layout that is verified and ready for fabrication.. [3; c,k]
iii. Design, implement, and use a hardware testbed for verification of functionality and performance of the chip after fabrication. Use a reconfigurable logic prototype for early testing and in lieu of a fabricated custom IC if necessary.. [4; c,e,k]
iv. Communicate effectively by means of an oral presentation of the project either to students in another course or at a technical conference.. [6; g]
v. Communicate effectively in writing by means of a collective technical report on the project and individual reports on how each outcome was satisfied.. [6; g]

Office of the Registrar
FORM 40 REV. 11/09

PURDUE UNIVERSITY
REQUEST FOR ADDITION, EXPIRATION,
OR REVISION OF AN UNDERGRADUATE COURSE
(10000-40000 LEVEL)

Print Form

EFD 51-11

DEPARTMENT School of Electrical and Computer Engineering (EFD 51-11) EFFECTIVE SESSION Spring 2012

INSTRUCTIONS: Please check the items below which describe the purpose of this request.

- [X] 1. New course with supporting documents
- [ ] 2. Add existing course offered at another campus
- [ ] 3. Expiration of a course
- [ ] 4. Change in course number
- [ ] 5. Change in course title
- [ ] 6. Change in course credit/type
- [ ] 7. Change in course attributes (department head signature only)
- [ ] 8. Change in instructional hours
- [ ] 9. Change in course description
- [ ] 10. Change in course requisites
- [ ] 11. Change in semesters offered (department head signature only)
- [ ] 12. Transfer from one department to another

PROPOSED:	EXISTING:
Subject Abbreviation ECE	Subject Abbreviation
Course Number 41438	Course Number
Long Title ASIC Fab and Test II	
Short Title ASIC Fab and Test II	

Abbreviated title will be entered by the Office of the Registrar if omitted. (30 CHARACTERS ONLY)

TERMS OFFERED
Check All That Apply:
[ ] Summer [ ] Fall [X] Spring

CAMPUS(ES) INVOLVED
[ ] Calumet [ ] N. Central
[ ] Cont Ed [ ] Tech Statewide
[ ] Ft. Wayne [X] W. Lafayette
[ ] Indianapolis

CREDIT TYPE
1. Fixed Credit: Cr. Hrs. 2
2. Variable Credit Range: Minimum Cr. Hrs
(Check One) To [ ] Or [ ]
Maximum Cr. Hrs.
3. Equivalent Credit: Yes [ ] No [ ]

COURSE ATTRIBUTES: Check All That Apply
1. Pass/Not Pass Only [ ]
2. Satisfactory/Unsatisfactory Only [ ]
3. Repeatable [ ]
Maximum Repeatable Credit: [ ]
4. Credit by Examination [ ]
5. Special Fees [ ]
6. Registration Approval Type
Department [X] Instructor [ ]
7. Variable Title [ ]
8. Honors [ ]
9. Full Time Privilege [ ]
10. Off Campus Experience [ ]

ScheduleType	Minutes Per Mtg	Meetings Per Week	Weeks Offered	% of Credit Allocated
Lecture	50	1	16	
Recitation				
Presentation				
Laboratory	100	2	16	
Lab Prep				
Studio				
Distance				
Clinic				
Experiential				
Research				
Ind. Study				
Pract/Observ				

Cross-Listed Courses

COURSE DESCRIPTION (INCLUDE REQUISITES/RESTRICTIONS):
See attached.

*COURSE LEARNING OUTCOMES:
See attached.

Calumet Department Head	Date	Calumet School Dean	Date
Fort Wayne Department Head	Date	Fort Wayne School Dean	Date
Indianapolis Department Head	Date	Indianapolis School Dean	Date
North Central Department Head	Date	North Central Chancellor	Date
West Lafayette Department Head	8/25/11 Date	West Lafayette College/School Dean	11/16/2011 Date
		West Lafayette Registrar	Date

OFFICE OF THE REGISTRAR

File

Form 40 attachment

School of Electrical and Computer Engineering (EFD 51-11)

Description:

The second semester of a two-semester sequence to give teams of 3 to 6 students the experience of designing an ASIC, having the chip fabricated, and testing it. The team of students will develop requirements for a design, prepare the design using VHDL, Verilog, or schematic entry tools, create and use test benches to functionally verify the design, use automated tools to prepare a circuit layout, verify the final layout, submit the layout for fabrication, prepare a physical test bed, test or demonstrate the chip, and document all aspects of the design and test results.

Prerequisite: ECE 41437 and Departmental Approval

Restrictions: Must be enrolled in the School of Electrical and Computer Engineering

Course Learning Outcomes:

A student who successfully fulfills the course requirements will have demonstrated:

i. Create testbenches and verify the functionality of the design in source code after logic synthesis and after layout. [4; e,k]
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