PURDUE UNIVERSITY
REQUEST FOR ADDITION, EXPIRATION,
OR REVISION OF AN UNDERGRADUATE COURSE
(10000-40000 LEVEL)

DEPARTMENT School of Electrical and Computer Engineering (EFD 32-10) EFFECTIVE SESSION Fall 2010

INSTRUCTIONS: Please check the items below which describe the purpose of this request.

- New course with supporting documents
- Add existing course offered at another campus
- Expiration of a course
- Change in course number
- Change in course title
- Change in course credit/type
- Change in course attributes (department head signature only)
- Change in instructional hours
- Change in course description
- Change in course requisites
- Change in semesters offered (department head signature only)
- Transfer from one department to another

PROPOSED:
Subject Abbreviation
Course Number
Long Title ASIC Design Laboratory
Short Title ASIC Design Laboratory

EXISTING:
Subject Abbreviation ECE
Course Number 33700

TERMS OFFERED
Check All That Apply:
- Summer
- Fall
- Spring

CAMPUS(ES) INVOLVED
- Calumet
- Cont Ed
- Ft. Wayne
- Indianapolis
- N. Central
- Tech Statewide
- W. Lafayette

Abbreviated title will be entered by the Office of the Registrar if omitted. (30 CHARACTER ONLY)

CREDIT TYPE
1. Fixed Credit: Cr. Hrs.
2. Variable Credit Range: Minimum Cr. Hrs. To Maximum Cr. Hrs.
3. Equivalent Credit: Yes

Schedule Type
Lecture
Instruction
Recitation
Seminar
Laboratory
Lab Prep
Studio
Distance
Clinic
Experiential
Research
Ind. Study
Prac/Observe

Minutes Per Mtg
Meetings Per Week
Weekly Offered
% of Credit Allocated

COURSE ATTRIBUTES: Check All That Apply
1. Pass/Not Pass Only
2. Satisfactory/Unsatisfactory Only
3. Repeatability
4. Credit by Examination
5. Special Fees
6. Registration Approval Type Department
7. Variable Title
8. Honors
9. Full Time Privilege
10. Off Campus Experience

Cross-Listed Courses

COURSE DESCRIPTION (INCLUDE REQUISITES/RESTRICTIONS):
Prerequisites: ECE 27000 Minimum Grade of C

*COURSE LEARNING OUTCOMES:
See attachment.

Calumet Department Head Date
Calumet School Dean Date

Fort Wayne Department Head Date
Fort Wayne School Dean Date

Indianapolis Department Head Date
Indianapolis School Dean Date

West Lafayette Department Head Date
West Lafayette College/School Dean Date
West Lafayette Registrar Date

OFFICE OF THE REGISTRAR

Signature
Date

Office of the Registrar
FORM 40 REV. 11/09
PURDUE UNIVERSITY
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PROPOSED:

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<tr>
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</thead>
<tbody>
<tr>
<td>ASIC Design Laboratory</td>
<td>ECE</td>
<td>33700</td>
<td>33700</td>
</tr>
</tbody>
</table>

Long Title: ASIC Design Laboratory
Short Title: ASIC Design Laboratory

Abbreviated title will be entered by the Office of the Registrar if omitted. (30 CHARACTERS ONLY)

TERMS OFFERED

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CAMPUS(ES) INVOLVED

- Calumet
- Cont Ed
- Ft. Wayne
- Tech Statewide
- Indianapolis
- N. Central
- W. Lafayette

CREDIT TYPE

<table>
<thead>
<tr>
<th>1. Fixed Credit: Cr. Hrs.</th>
<th>2. Variable Credit Range: Minimum Cr. Hrs (Check One)</th>
<th>3. Equivalent Credit: Yes</th>
<th>No</th>
</tr>
</thead>
</table>

COURSE ATTRIBUTES: Check All That Apply

|-----------------------|------------------------------------|--------------|------------------------|

<table>
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<tr>
<th>5. Special Fees</th>
<th>6. Registration Approval Type</th>
<th>7. Variable Title</th>
<th>8. Honors</th>
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|------------------------|---------------------------|

Schedule Type

- Lecture
- Recitation
- Laboratory
- Corporation
- Lab Prep
- Studio
- Distance
- Clinic
- Experiential
- Research
- Ind. Study
- Pract/Observer

% of Credit

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<th>Minutes Per Mtg</th>
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</thead>
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COURSE DESCRIPTION (INCLUDE REQUISITES/RESTRICTIONS):

Prerequisites: ECE 27000 Minimum Grade of C

*COURSE LEARNING OUTCOMES:

See attachment.

Calumet Department Head Date

Calumet School Dean Date

Fort Wayne Department Head Date

Fort Wayne School Dean Date

Indianapolis Department Head Date

Indianapolis School Dean Date

North Central Department Head Date

North Central Chancellor Date

West Lafayette Department Head Date

West Lafayette School Dean Date

West Lafayette Registrar Date

OFFICE OF THE REGISTRAR
TO: The Faculty of the College of Engineering  
FROM: The Faculty of the School of Electrical and Computer Engineering  
RE: Change to Existing Undergraduate Course: ECE 33700, ASIC Design Laboratory, change in requisites.

The faculty of the School of Electrical and Computer Engineering has approved the following changes to an existing course. This action is now submitted to the Engineering Faculty with a recommendation for approval.

From: ECE 33700 ASIC Design Laboratory  
Sem. Fall, Spring; Cr. 2; Lecture 2.  
Prerequisites: ECE 27000  
Restrictions: Must be enrolled in one of the following: School of Electrical & Computer Engineering  
Description: Introduction to standard cell design of VLSI (Very Large Scale Integration) digital circuits using the VHDL hardware description language (Very High Speed Integrated Circuits Hardware Description Language). Emphasis on how to write VHDL that will map readily to hardware. Laboratory experiments using commercial grade computer-aided design (CAD) tools for VHDL based design, schematic based logic entry, logic and VHDL simulation, automatic placement and routing, timing analysis, and testing.

To: ECE 33700 ASIC Design Laboratory  
Sem. Fall, Spring; Cr. 2; Lecture 2.  
Prerequisites: ECE 27000 Minimum Grade of C  
Restrictions: Must be enrolled in: School of Electrical & Computer Engineering  
Description: Introduction to standard cell design of VLSI (Very Large Scale Integration) digital circuits using the VHDL hardware description language (Very High Speed Integrated Circuits Hardware Description Language). Emphasis on how to write VHDL that will map readily to hardware. Laboratory experiments using commercial grade computer-aided design (CAD) tools for VHDL based design, schematic based logic entry, logic and VHDL simulation, automatic placement and routing, timing analysis, and testing.

Approved for the Faculty of the Schools of Engineering by the Engineering Curriculum Committee  
ECC Minutes 4424  
Date 4/20/10  
Chairman ECC R. Cipra
Reason: This course is part of the Core Curriculum for the BSCmpE degree. Subsets of Core Curriculum courses serve as prerequisites for most upper division ECE electives. In addition, a degree requirement for all ECE students is to achieve a GPA in all major-area (ECE) courses of at least a 2.0. Therefore, in order to ensure that ECE students are as well prepared as possible for upper division ECE courses, as well as to facilitate their achievement of the minimum major-area GPA of 2.0, a minimum grade requirement in the key ECE prerequisite course is being proposed.

[Signature]

on behalf of Y. Balakrishnan, Interim Head
School of Electrical and Computer Engineering
Course Learning Outcomes:

i. understand and use major syntactic elements of VHDL - entities, architectures, processes, functions, common concurrent statements, and common sequential statements.

ii. design combinational logic in a variety of styles including: schematic, structural VHDL, and behavioral VHDL, as well as demonstrate an awareness of timing and resource usage associated with each approach.

iii. design common sequential functions: flip-flops, registers, latches, and state-machines.

iv. create a VHDL test bench and use it to test/verify a sequential VHDL design of moderate complexity.

v. place, route, and verify timing of a standard cell design.

vi. draw, given commented VHDL code of moderate complexity, a corresponding RTL level block diagram.

vii. use, modify, and create scripts to control the synthesis process.

viii. use different design styles, constraints, and optimization options to achieve required synthesis results.

ix. explain the difference between various ASIC design approaches - standard cell, full custom, and programmable devices.

x. prepare functional and interface requirements for a sequential design project of the student's choosing.

xi. create the hierarchical decomposition of a sequential design.

xii. gain experience in the oral presentation of their work to others.

xiii. work in a team and negotiate the division of labor.

xiv. gain familiarity with the use and purpose of design reviews.

xv. prepare final design documentation sufficient for another engineer to use, test, or enhance the design.