Office of the Registrar FORM 40 REV. 11/09

PURDUE UNIVERSITY REQUEST FOR ADDITION, EXPIRATION, OR REVISION OF AN UNDERGRADUATE COURSE (10000-40000 LEVEL)

Print Form

EFD 32-10

PARTMENT School of Electrical and Computer Engineering (EFD 32-10) EFFECTIVE SESSION Fall 2010					
INSTRUCTIONS: Please check the items below which describe the purpose of this request.					
INSTRUCTIONS: Please check the items below 1. New course with supporting docu 2. Add existing course offered at an 3. Expiration of a course 4. Change in course number 5. Change in course title 6. Change in course credit/type PROPOSED: Subject Abbreviation Course Number Long Title ASIC Design Laboratory Short Title ASIC Design Laboratory	ments 7.	Change in instruction Change in course de Change in course re Change in semester	escription equisites rs offered (department head signature only) lepartment to another TERMS OFFERED Check All That Apply: Summer Fall Spring CAMPUS(ES) INVOLVED Calumet N. Central Tech Statewide Ft. Wayne W. Lafayette		
Abbreviated title will be entered	by the Office of the Registrar if omitted. (30 CHAR	ACTERS ONLY)	Indianapolis 77		
CREDIT TYPE 1.Fixed Credit: Cr. Hrs. 2.Variable Credit Range: Minimum Cr. Hrs (Check One) To Or Maximum Cr. Hrs. 3.Equivalent Credit: Yes No ScheduleType Minutes Per Mtg Lecture Citation Sentation Laboratory Lab Prep Studio Distance Clinic Experiential Research Ind. Study Pract/Observ COURSE DESCRIPTION (INCLUDE REQUISITE: Prerequisites: ECE 27000 Minimum Grade of C	1. Pass/Not Pass Only 2. Satisfactory/Unsatisfactory Only 3. Repeatable Maximum Repeatable Credit: 4. Credit by Examination 5. Special Fees Weeks Offered Allocated	Depa 7. Variable Title 8. Honors 9. Full Time P	on Approval Type rtment Instructor		
*COURSE LEARNING OUTCOMES: See attachment.					
Calumet Department Head Date	Calumet School Dean	Date			
Fort Wayne Department Head Date	Fort Wayne School Dean	Date			
Indianapolis Deparlment Head Date	Indianapolis School Dean	Date	0.4		
rth Central Department Head Date 3/3/1/0 West Latavette Department Head Date	North Central Chancellor West Lafayette College/School Dean	Date S/24/2010 Date West I	Date Registrar		

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Office of the Registrar FORM 40 REV. 11/09

PURDUE UNIVERSITY

REQUEST FOR ADDITION, EXPIRATION, OR REVISION OF AN UNDERGRADUATE COURSE (10000-40000 LEVEL)

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Date

West Lafayette Registrar

EFD 32-10 DEPARTMENT School of Electrical and Computer Engineering (EFD 32-10) **EFFECTIVE SESSION Fall 2010** INSTRUCTIONS: Please check the items below which describe the purpose of this request. New course with supporting documents 7. Change in course attributes (department head signature only) 2. Add existing course offered at another campus 8. Change in instructional hours 3. Expiration of a course 9. Change in course description Change in course number 10. Change in course requisites Change in course title Change in semesters offered (department head signature only) Change in course credit/type 12. Transfer from one department to another PROPOSED: **EXISTING: TERMS OFFERED** Check All That Apply: **Subject Abbreviation** Subject Abbreviation ECE Summer Fall Spring Course Number Course Number 33700 CAMPUS(ES) INVOLVED Calumet Long Title ASIC Design Laboratory N. Central Cont Ed Tech Statewide Ft. Wayne Short Title ASIC Design Laboratory W. Lafayette Indianapolis Abbreviated title will be entered by the Office of the Registrar if omitted. (30 CHARACTERS ONLY) COURSE ATTRIBUTES: Check All That Apply 1.Fixed Credit: Cr. Hrs. 1. Pass/Not Pass Only 6. Registration Approval Type 2. Variable Credit Range: Instructor 2. Satisfactory/Unsatisfactory Only Department Minimum Cr. Hrs 3. Repeatable (Check One) Оr 7. Variable Title Maximum Repeatable Credit: Maximum Cr. Hrs. 8. Honors 4. Credit by Examination 9. Full Time Privilege 3.Equivalent Credit: Yes No 5. Special Fees 10. Off Campus Experience ScheduleType Minutes Meetings Per % of Credit Weeks Week Cross-Listed Courses Per Mtg Allocated Offered Lecture Recitation esentation poratory Lab Prep Studio Distance Clinic Experiential Research Ind. Study Pract/Observ COURSE DESCRIPTION (INCLUDE REQUISITES/RESTRICTIONS): Prerequisites: ECE 27000 Minimum Grade of C *COURSE LEARNING OUTCOMES: See attachment. Calumet Department Head Calumet School Dean Date Date Fort Wayne Department Head Date Fort Wayne School Dean Date Date Indianapolis School Dean Indianapolis Department Head Date North Central Department Head Date North Central Chancellor Date

West Lafayette College/School Dean

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		Name of the State

TO:

The Faculty of the College of Engineering

FROM:

The Faculty of the School of Electrical and Computer Engineering

RE:

Change to Existing Undergraduate Course: ECE 33700, ASIC Design Laboratory,

change in requisites.

The faculty of the School of Electrical and Computer Engineering has approved the following changes to an existing course. This action is now submitted to the Engineering Faculty with a recommendation for approval.

From:

ECE 33700 ASIC Design Laboratory

Sem. Fall, Spring; Cr. 2; Lecture 2.

Prerequisites: ECE 27000

Restrictions: Must be enrolled in one of the following: School of Electrical &

Computer Engineering

Description: Introduction to standard cell design of VLSI (Very Large Scale Integration) digital circuits using the VHDL hardware description language (Very High Speed Integrated Circuits Hardware Description Language). Emphasis on how to write VHDL that will map readily to hardware. Laboratory experiments using commercial grade computer-aided design (CAD) tools for VHDL based design, schematic based logic entry, logic and VHDL simulation, automatic placement and

routing, timing analysis, and testing.

To:

ECE 33700 ASIC Design Laboratory

Sem. Fall, Spring; Cr. 2; Lecture 2.

Prerequisites: ECE 27000 Minimum Grade of C

Restrictions: Must be enrolled in: School of Electrical & Computer Engineering Description: Introduction to standard cell design of VLSI (Very Large Scale Integration) digital circuits using the VHDL hardware description language (Very High Speed Integrated Circuits Hardware Description Language). Emphasis on how to write VHDL that will map readily to hardware. Laboratory experiments using commercial grade computer-aided design (CAD) tools for VHDL based design, schematic based logic entry, logic and VHDL simulation, automatic placement and

routing, timing analysis, and testing.

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Date 4/20/10
Chairman ECC R. Cipsa

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Reason:

This course is part of the Core Curriculum for the BSCmpE degree. Subsets of Core Curriculum courses serve as prerequisites for most upper division ECE electives. In addition, a degree requirement for all ECE students is to achieve a GPA in all majorarea (ECE) courses of at least a 2.0. Therefore, in order to ensure that ECE students are as well prepared as possible for upper division ECE courses, as well as to facilitate their achievement of the minimum major-area GPA of 2.0, a minimum grade requirement in the key ECE prerequisite course is being proposed.

on behalf of V. Balakrishnan, Viterim Head School of Electrical and Computer Engineering

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School of Electrical and Computer Engineering (EFD 32-10)

Course Learning Outcomes:

- understand and use major syntactic elements of VDHL entities, architectures, processes, functions, common concurrent statements, and common sequential statements.
- ii. design combinational logic in a variety of styles including: schematic, structural VHDL, and behavioral VHDL, as well as demonstrate an awareness of timing and resource usage associated with each approach.
- iii. design common sequential functions: flip-flops, registers, latches, and state-machines..
- iv. create a VDHL test bench and use it to test/verify a sequential VHDL design of moderate complexity.
- v. place, route, and verify timing of a standard cell design.
- vi. draw, given commented VHDL code of moderate complexity, a corresponding RTL level block diagram.
- vii. use, modify, and create scripts to control the synthesis process.
- viii. use different design styles, constraints, and optimization options to achieve required synthesis results.
- ix. explain the difference between various ASIC design approaches standard cell, full custom, and programmable devices.
- x. prepare functional and interface requirements for a sequential design project of the student's choosing.
- xi. create the hierarchical decomposition of a sequential design.
- xii. gain experience in the oral presentation of their work to others.
- xiii. work in a tema and negotiate the division of labor.
- xiv. gain familiarity with the use and purpose of design reviews.
- xv. prepare final design documentation sufficient for another engineer to use, test, or enhance the design.

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