

TO: The Faculty of the College of Engineering

FROM: School of Electrical and Computer Engineering of the College of Engineering

RE: New Graduate Course, ECE 51214 CMOS Analog IC Design

The faculty of the School of Electrical and Computer Engineering has approved the following new course. This action is now submitted to the Engineering Faculty with a recommendation for approval.

ECE 51214 CMOS Analog IC Design

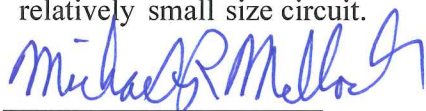
Sem. 1, Lecture 3, Cr. 3.

Prerequisite: ECE 255 or equivalent courses or consent of instructor

Prerequisite by Topic: General knowledge of terminology and concepts from undergraduate courses in circuit design and microelectronics; familiarity with SPICE

Description: The course covers general topics in CMOS analog IC design; biasing, noise, single stage amplifiers, differential amplifiers, OP-Amp, OTA, frequency domain analysis, and active filters. While the focus of the course is on CMOS IC design, design in bipolar and Bi CMOS technologies are introduced as well. A design project is a key component of the course. The students conduct group or individual design projects. Process Design *Kit* and EDA tools are provided for the design projects.

Reason: Since this course covers broad topics in CMOS IC design, it is appropriate for entry level graduate students or advanced undergraduates who have general knowledge of terminology and concepts from undergraduate courses in circuit design and microelectronics. Two undergraduate students had enrolled during the first offer, and both got B. About 5 undergraduate students had enrolled during the second offer, but all of them dropped in the first two weeks. The main complaint from the undergraduate students was design project load. There were complaints about the size of the design project from a few grad students, too. The layout and post-layout simulation parts will be removed from the design project to reduce the course load to a reasonable level, and to encourage motivated undergraduate students to enroll this course. The layout and post-layout simulation will be covered as a homework using relatively small size circuit.



Michael R. Melloch, Associate Head
School of Electrical and Computer Engineering

PURDUE UNIVERSITY
REQUEST FOR ADDITION, EXPIRATION,
OR REVISION OF A GRADUATE COURSE
(50000-60000 LEVEL)

DEPARTMENT Electrical and Computer Engineering EFFECTIVE SESSION Spring 2018

INSTRUCTIONS: Please check the items below which describe the purpose of this request.

- | | |
|--|--|
| <input checked="" type="checkbox"/> 1. New course with supporting documents (complete proposal form) | <input type="checkbox"/> 7. Change in course attributes |
| <input type="checkbox"/> 2. Add existing course offered at another campus | <input type="checkbox"/> 8. Change in instructional hours |
| <input type="checkbox"/> 3. Expiration of a course | <input type="checkbox"/> 9. Change in course description |
| <input type="checkbox"/> 4. Change in course number | <input type="checkbox"/> 10. Change in course requisites |
| <input type="checkbox"/> 5. Change in course title | <input type="checkbox"/> 11. Change in semesters offered |
| <input type="checkbox"/> 6. Change in course credit/type | <input type="checkbox"/> 12. Transfer from one department to another |

PROPOSED: Subject Abbreviation <u>ECE</u> Course Number <u>51214</u> Long Title <u>CMOS Analog IC Design</u> Short Title <u>CMOS Analog IC Design</u> <small>Abbreviated title will be entered by the Office of the Registrar if omitted. (30 CHARACTERS ONLY)</small>		EXISTING: Subject Abbreviation _____ Course Number _____		TERMS OFFERED Check All That Apply: <input checked="" type="checkbox"/> Fall <input type="checkbox"/> Spring <input type="checkbox"/> Summer
CAMPUS(ES) INVOLVED <input type="checkbox"/> Calumet <input type="checkbox"/> N. Central <input type="checkbox"/> Cont Ed <input type="checkbox"/> Tech Statewide <input type="checkbox"/> Ft. Wayne <input checked="" type="checkbox"/> W. Lafayette <input type="checkbox"/> Indianapolis				

CREDIT TYPE 1. Fixed Credit: Cr. Hrs. <u>3</u> 2. Variable Credit Range: Minimum Cr. Hrs _____ (Check One) To <input type="checkbox"/> Or <input type="checkbox"/> Maximum Cr. Hrs _____ 3. Equivalent Credit: Yes <input type="checkbox"/> No <input checked="" type="checkbox"/> 4. Thesis Credit: Yes <input type="checkbox"/> No <input checked="" type="checkbox"/>	COURSE ATTRIBUTES: Check All That Apply 1. Pass/Not Pass Only <input type="checkbox"/> 2. Satisfactory/Unsatisfactory Only <input type="checkbox"/> 3. Repeatable <input type="checkbox"/> Maximum Repeatable Credit: <input type="checkbox"/> 4. Credit by Examination <input type="checkbox"/> 5. Fees <input type="checkbox"/> Coop <input type="checkbox"/> Lab <input type="checkbox"/> Rate Request <input type="checkbox"/> Include comment to explain fee _____	6. Registration Approval Type Department <input type="checkbox"/> Instructor <input type="checkbox"/> 7. Variable Title <input type="checkbox"/> 8. Honors <input type="checkbox"/> 9. Full Time Privilege <input type="checkbox"/> 10. Off Campus Experience <input type="checkbox"/>
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Schedule Type	Minutes Per Mtg	Meetings Per Week	Weeks Offered	% of Credit Allocated	Cross-Listed Courses
Lecture	50	3	16	100	
Recitation					
Presentation					
Laboratory					
Lab Prep					
Studio					
Distance					
Clinic					
Experiential					
Research					
Ind. Study					
Pract/Observ					

COURSE DESCRIPTION (INCLUDE REQUISITES/RESTRICTIONS):
 The course covers general topics in CMOS analog IC design; biasing, noise, single stage amplifiers, differential amplifiers, OP-Amp, OTA, frequency domain analysis, and active filter. While the focus of the course is on CMOS IC design, design in bipolar and BiCMOS technologies are introduced as well. A design project is a key component of the course. The students conduct group or individual design project. Process

***COURSE LEARNING OUTCOMES:**
 Attached

Calumet Department Head	Date	Calumet School Dean	Date	Calumet Director of Graduate Studies	Date
Fort Wayne Department Head	Date	Fort Wayne School Dean	Date	Fort Wayne Director of Graduate Studies	Date
Indianapolis Department Head	Date	Indianapolis School Dean	Date	IUPUI Associate Dean for Graduate Education	Date
North Central Department Head	Date	North Central School Dean	Date	North Central Director of Graduate Studies	Date
<i>M.R. Melhorn</i>	<i>10/17/17</i>	West Lafayette College/School Dean	Date	Date Approved by Graduate Council	Date
Graduate Area Committee Convener	Date	Graduate Dean	Date	Graduate Council Secretary	Date
				West Lafayette Registrar	Date

Outcomes: ECE 51214 CMOS Analog IC Design

ECE Graduate Learning Outcomes:

- a. Knowledge and Scholarship (thesis/non-thesis)
 - b. Communication (thesis/non-thesis)
 - c. Critical Thinking (thesis/non-thesis)
 - d. Ethical and Responsible Research (thesis) or Professional and Ethical Responsibility (non-thesis)
- List Learning Objectives for this course and map each Learning Objective to one or more of the ECE Graduate Learning Outcomes (a-d, listed above):
 - Learn a basic knowledge of bias circuits [a,c]
 - Learn a basic knowledge of noise analysis [a,c]
 - Learn a basic knowledge of single stage amplifiers and their applications [a,c,d]
 - Learn a basic knowledge of differential Op-amp, OTA, and practical design skills [a,b,c,d]
 - Learn a basic knowledge of feedback circuits [a,c,d]
 - Learn a basic knowledge of active filters, practical design skills and applications [a,b,c,d]

**Supporting Document to the Form 40G
for a New Graduate Course**

To: Purdue University Graduate Council

From: Faculty Member: Byunghoo Jung

Department: Electrical and Computer Engineering

Campus: West Lafayette

Date:

Subject: Proposal for New Graduate Course

Contact for information if questions arise: Name: Matt Golden
Phone: 494-3374
Email: goldenm@purdue.edu
Address: EE Building, Room 135

Course Subject Abbreviation and Number: ECE 51214

Course Title: CMOS Analog IC Design

Course Description:

The course covers general topics in CMOS analog IC design; biasing, noise, single stage amplifiers, differential amplifiers, OP-Amp, OTA, frequency domain analysis, and active filter. While the focus of the course is on CMOS IC design, design in bipolar and BiCMOS technologies are introduced as well. A design project is a key component of the course. The students conduct group or individual design project. Process Design *Kit* and EDA tools are provided for the design project.

Semesters Offered:

For the benefit of graduate student plan of study development, how frequently will this prototype be offered? Which semesters?
Each Fall

A. Justification for the Course:

Provide a complete and detailed explanation of the need for the course (e. g., in

the preparation of students, in providing new knowledge/training in one or more topics, in meeting degree requirements, etc.), how the course contributes to existing majors and/or concentrations, and how the course relates to other graduate courses offered by the department, other departments, or interdisciplinary programs.

Justify the level of the proposed graduate course (500- or 600-level) including statements on, but not limited to: (1) the target audience, including the anticipated number of undergraduate and graduate students who will enroll in the course; and (2) the rigor of the course.

Since this course covers broad topics in CMOS IC design, it is appropriate for entry level graduate students or advanced undergraduates who have general knowledge of terminology and concepts from undergraduate courses in circuit design and microelectronics. Two undergraduate students had enrolled during the first offer, and both got B. About 5 undergraduate students had enrolled during the second offer, but all of them dropped in the first two weeks. The main complaint from the undergraduate students was design project load. There were complaints about the size of the design project from a few grad students, too. The layout and post-layout simulation parts will be removed from the design project to reduce the course load to a reasonable level, and to encourage motivated undergraduate students to enroll this course. The layout and post-layout simulation will be covered as a homework using relatively small size circuit.

Use the following criteria:

Graduate Council policy requires that courses at the 50000 level in the Purdue system should be taught at the graduate level and meet four criteria: a) the use of primary literature in conjunction with advanced secondary sources (i.e., advanced textbooks); b) assessments that demonstrate synthesis of concepts and ideas by students; c) demonstrations that topics are current, and; d) components that emphasize research approaches/methods or discovery efforts in the course content area (reading the research, critiquing articles, proposing research, performing research). Such courses should be taught so that undergraduate students are expected to rise to the level of graduate work and be assessed in the same manner as the graduate students.

- Anticipated enrollment
 - Undergraduate 2-5
 - Graduate 20-25

B. Learning Outcomes and Method of Evaluation or Assessment:

ECE Graduate Learning Outcomes:

- a. Knowledge and Scholarship (thesis/non-thesis)
 - b. Communication (thesis/non-thesis)
 - c. Critical Thinking (thesis/non-thesis)
 - d. Ethical and Responsible Research (thesis) or Professional and Ethical Responsibility (non-thesis)
- List Learning Objectives for this course and map each Learning Objective to one or more of the ECE Graduate Learning Outcomes (a-d, listed above):
 - Learn a basic knowledge of bias circuits [a,c]
 - Learn a basic knowledge of noise analysis [a,c]
 - Learn a basic knowledge of single stage amplifiers and their applications [a,c,d]
 - Learn a basic knowledge of differential Op-amp, OTA, and practical design skills [a,b,c,d]
 - Learn a basic knowledge of feedback circuits [a,c,d]
 - Learn a basic knowledge of active filters, practical design skills and applications [a,b,c,d]

- Methods of Instruction

- Lecture

- Will/can this course be offered via Distance Learning?

- No

- Grading Criteria

Grading criteria (select from checklist); include a statement describing the criteria that will be used to assess students and how the final grade will be determined. Add and delete rows as needed.

- exams and/or quizzes
- papers and/or projects

- ▶ Describe the criteria that will be used to assess students and how the final grade will be determined:

The course will be graded primarily on a combination of examinations and course projects. A smaller part of the grade will be based on homework, quiz, and class participation. The examination component will include two mid-term exams. The course project component will include interim and final design reports.

C. Prerequisite(s):

List prerequisites and/or experiences/background required. If no prerequisites are indicated, provide an explanation for their absence. Add bullets as needed.

- ECE 255 or equivalent courses or consent of instructor

Prerequisite by Topic: General knowledge of terminology and concepts from undergraduate courses in circuit design and microelectronics; familiarity with SPICE

D. Course Instructor(s):

Provide the name, rank, and department/program affiliation of the instructor(s). Is the instructor currently a member of the Graduate Faculty? (If the answer is no, indicate when it is expected that a request will be submitted.) Add rows as needed.

Name	Rank	Dept.	Graduate Faculty or expected date
Byunghoo Jung	Associate Professor	ECEN	Yes

E. Course Outline:

Provide an outline of topics to be covered and indicate the relative amount of time or emphasis devoted to each topic. If laboratory or field experiences are used to supplement a lecture course, explain the value of the experience(s) to enhance the quality of the course and student learning. For special topics courses, include a sample outline of a course that would be offered under the proposed course. **(This information must be listed and may be copied from syllabus).**

Lectures	Principal Topics
1	CMOS device physics review
3	Spice models and layout
2	Current biasing
2	Voltage reference
5	Noise analysis
7	Single stage amplifiers
6	OTA and Opamp design
4	Gain boosting and bandwidth extension

- 4 Feedback
- 4 Stability and compensation
- 1 Integrated active filter design
- 3 Switched capacitor filter design

F. Reading List (including course text):

A primary reading list or bibliography should be limited to material the students will be required to read in order to successfully complete the course. It should not be a compilation of general reference material.

A secondary reading list or bibliography should include material students may use as background information.

- Primary Reading List
 - Design of Analog CMOS Integrated Circuits by Behzad Razavi (McGraw-Hill) (ISBN 0-07-238032-2)
- Secondary Reading List
 - CMOS Analog Circuit Design by Phillip E. Allen (Oxford) (ISBN 0-19-511644-5)
 - Analog Integrated Circuit Design by David Johns and Ken Martin (Wiley) (ISBN 0-471-14448-7)
 - CMOS Circuit Design, Layout, and Simulation (Wiley) (ISBN 978-0-470-22941-5)

G. Library Resources

Describe any library resources that are currently available or the resources needed to support this proposed course.

H. Course Syllabus

(While not a necessary component of this supporting document, an example of a course syllabus is available, for information, by clicking on the link below, which goes to the *Graduate School's Policies and Procedures Manual for Administering Graduate Student Program*.

See Appendix K.

[http://www.purdue.edu/gradschool/faculty/documents/Graduate School Policies and Procedures Manual.pdf](http://www.purdue.edu/gradschool/faculty/documents/Graduate_School_Policies_and_Procedures_Manual.pdf)

ECE595 CMOS Analog IC Design (3Cr), Fall 2017

Class Schedule: MWF 3:30AM ~ 4:20PM, EE 222

Important Announcement Regarding Campus Emergency:

In the event of a major campus emergency, course requirements, deadlines and grading percentages are subject to changes that may be necessitated by a revised semester calendar or other circumstances. In such an event, information will be provided through Blackboard Learn.

Prerequisite:

- ✓ ECE 255 Introduction to Electronic Analysis and Design or Equivalent

Requisites by Topic: General knowledge of terminology and concepts from undergraduate courses in circuit design and microelectronics; familiarity with SPICE

Instructor: Byunghoo Jung (494-2866, jungb@pru.edu)

Office hours: MWF 1:30AM-2:30PM or by appointment (Room WANG 2053)

Class Website: Blackboard Learn

Required Text: Design of Analog CMOS Integrated Circuits by Behzad Razavi (MaGraw-Hill)

Recommended Text(s):

1. *Analog Integrated Circuit Design*, David Johns and Ken Martin, Wiley, ISBN No. 0471144487.
2. *CMOS Analog Circuit Design*, Phillip E. Allen, Oxford, ISBN No. 0195116445.
3. *CMOS Circuit Design, Layout, and Simulation*, Wiley, ISBN No. 9780470229415.

Course Description: The course covers general topics in CMOS analog IC design; biasing, noise, single stage amplifiers, differential amplifiers, OP-Amp, OTA, frequency domain analysis, and active filter. While the focus of the course is on CMOS IC design, design in bipolar and BiCMOS technologies are introduced as well. A design project is a key component of the course. The students conduct group or individual design project. Process Design Kit and EDA tools are provided for the design project.

Course Objectives:

A student who successfully fulfills the course requirements will have demonstrated:

- i. a basic knowledge of bias circuits [a,c]
- ii. a basic knowledge of noise analysis [a,c]
- iii. an understanding of single stage amplifiers and their applications [a,c,d]
- iv. an understanding of differential Op-amp ,OTA, and practical design skills. [a,b,c,d]

ECE595 CMOS Analog IC Design (3Cr), Fall 2017

- v. an understanding of feedback circuits [a,c,d]
- vi. an understanding of basic active filters, practical design skills and applications [a,b,c,d]

Assessment Method for Learning Objectives: 2 midterm exams and design projects: i. The first midterm exam covers bias circuit design, noise analysis, and single stage amplifiers ii. The second midterm exam covers differential Opamp, OTA, frequency domain analysis, and active filter design iii. The students are asked to demonstrate their project design (schematic level) at the end of the semester

Exam and Design Project Schedule

- ✓ **Project Proposal Due:** submit to the instructor through email by 6:00PM on Sept. 15 (Fri)
- ✓ **First Exam:** Oct. 18 (Wed) In-class exam, close book/notebook, single-side Letter size paper with equations
- ✓ **Interim Project Report Due:** submit to the instructor by 6:00PM on Nov. 01 (Wed)
- ✓ **Second Exam:** Nov. 20 (Mon) In class exam, open book, open notebook
- ✓ **Final Project Report Due:** submit to the instructor by 6:00PM on Dec. 11 (Mon)
- ✓ **Submit homework and project reports to Instructor:** E-mail submission is recommended. **PDF (or MS-Word) format only!**

Grading Policy

- ✓ Absolute and relative scale:
 - When the average is lower than 65/100: 25% A, 40%B, 25% C, 10% D/F
 - When the average is over 65/100: 35% A, 40% B, 20% C, 5% D/F
 - When the average is over 75/100: 40% A, 50% B, 10% C
- ✓ 2 mid-terms each accounting for 25% of the grade ($25\% \cdot 2 = 50\%$)
- ✓ Design Project accounts for 40% of the grade
- ✓ Homework assignments account for 10%
- ✓ Late projects or assignments will **NOT** be accepted
 - You may request extension for homework assignment or make-up exam for documented emergencies (e.g. hospitalization, death of family member, etc.) It has to be requested BEFORE its due date except campus emergency.
- ✓ Any form of cheating will be reported to the Dean of students AND result in a failing grade
- ✓ Must fulfill ABET requirements to get a passing grade

CAD LAB

- ✓ VLSI CAD Lab located in MSEE189 and 360 Potter Engineering Center
- ✓ Linux/SUN workstations running Cadence and HSpice
- ✓ Courtesy key for after-hour access can be obtained from front desk in Potter Engineering Library

Collaboration and Academic Honesty Policy

ECE595 CMOS Analog IC Design (3Cr), Fall 2017

Limited collaboration among students on the design project and homework problems is encouraged. Such collaboration may include verbal discussion of problems, and the use of scratch paper or writing boards to discuss concepts and approaches to solving specific problems. It is also OK for students to verbally compare the final answers obtained for a given problem as a method of checking their work. However, if you collaborate with others, please list the names of all those with whom you collaborated at the top of each solution set you hand in.

The following academic honesty rules should be considered in force at all times:

- ✓ Never show any draft of a homework solution to another student in the class until after the homework due date and after that person has handed in his/her own solution set.
- ✓ Never look at any draft of another person's homework solution until after the homework due date and after you have handed in your solution set.
- ✓ Never use another person's simulation files or supply your simulation files to another person for design project.

If any of the above academic honesty rules are violated by any student in the course, the student will receive a failing grade for the course and the incident will be reported to the Dean of the Student for further administrative action.

Lecture Outline:

Lectures	Principal Topics
1	CMOS device physic review
3	Spice models and layout
2	Current biasing
2	Voltage reference
5	Noise analysis
7	Single stage amplifiers
6	OTA and Op-amp design
4	Gain boosting and bandwidth extension
4	Feedback
4	Stability and compensation
1	Integrated active filter design
3	Switched capacitor filter design