Office of the Registrar
FORM 40 REV. 7/05

PURDUE UNIVERSITY

REQUEST FOR ADDITION, EXPIRATION, OR REVISION OF A COURSE

Print Form

2-05

DEPARTMENT The School of Electrical and Computer Engineering EFFECTIVE SESSION Fall 2006

INSTRUCTIONS: Please check the items below which describe the purpose of this request.

- [X] 1. New course with supporting documents
- [ ] 2. Add existing course
- [ ] 3. Expiration of a course
- [ ] 4. Change in course number
- [ ] 5. Change in course title
- [ ] 6. Change in course credit/type
- [ ] 7. Change in course attributes
- [ ] 8. Change in instructional hours
- [ ] 9. Change in course description
- [ ] 10. Change in course requisites
- [ ] 11. Change in semesters offered
- [ ] 12. Transfer from one department to another

PROPOSED:		EXISTING:	
Subject Abbreviation	ECE	Subject Abbreviation	
Course Number	337	Course Number	
Long Title	ASIC Design Laboratory		
Short Title	ASIC Des Lab ASIC Design Lab		

Abbreviated title will be entered by the Office of the Registrar if omitted. (22 CHARACTERS ONLY)

TERMS OFFERED Check All That Apply: Summer [ ] Spring [X] Fall [X]

CAMPUS(ES) INVOLVED

- Calumet [ ]
- Indianapolis [ ]
- W.Lafayette [X]
- Tech Statewide [ ]
- Ft. Wayne [ ]
- N. Central [ ]
- Cont Ed [ ]

CREDIT TYPE

1. Fixed Credit: Cr. Hrs. 2
2. Variable Credit Range: Minimum Cr. Hrs ____ (Check One) To [ ] Or [ ] Maximum Cr. Hrs ____
3. Equivalent Credit: Yes [ ] No [ ]
4. Thesis Credit: Yes [ ] No [ ]

COURSE ATTRIBUTES: Check all That Apply

1. Pass/Not Pass Only [ ]
2. Satisfactory/Unsatisfactory Only [ ]
3. Repeatable [X] NO
   Maximum repeatable credit: ____
4. Credit by Examination [ ]
5. Designator Required [ ]
6. Special Fees [ ]

7. Registration Approval Type: Department [X] Instructor [ ]
8. Variable Title [ ]
9. Remedial [ ]
10. Honors [ ]
11. Full Time Privilege [ ]
12. Off Campus Experience [ ]

Instructional Type	Minutes Per Mtg	Meetings Per Week	Weeks Offered	% of Credit Allocated	Delivery Method (Asyn. Or Syn)	Delivery Medium(Audio,Internet, Live,Text-Based, Video)
Lecture	50	1	16	50		
Recitation						
Presentation						
Laboratory	150	1	16	50		
Lab Prep						
Studio						
Distance						
Clinic						
Experiential						
Research						
Ind. Study						
Pract/Observ						

Cross-Listed Courses

COURSE DESCRIPTION (INCLUDE REQUISITES): P: ECE 264, ECE 270

Introduction to standard cell design of VLSI (Very Large Scale Integration) digital circuits using the VHDL hardware description language (Very High Speed Integrated Circuits Hardware Description Language). Emphasis on how to write VHDL that will map readily to hardware. Laboratory experiments using commercial grade computer-aided design (CAD) tools for VHDL based design, schematic based logic entry, logic and VHDL simulation, automatic placement and routing, timing analysis, and testing.

Calumet Undergrad Curriculum Committee	Date	Calumet Department Head	Date	Calumet School Dean	Date
Fort Wayne Department Head	Date	Fort Wayne School Dean	Date	Fort Wayne Chancellor	Date
Indianapolis Department Head	Date	Indianapolis School Dean	Date	Undergrad Curriculum Committee	Date 2/7/06
North Central Department Head	Date 2/2/06	North Central Chancellor	Date 2/3/06	Date Approved by Graduate Council	
West Lafayette Department Head	Date	West Lafayette College/School Dean	Date	Graduate Council Secretary	Date
Graduate Council Area Committee Chair	Date	Graduate Dean	Date	West Lafayette Registrar	Date 2/17/06

OFFICE OF THE REGISTRAR

TO: The Faculty of the College of Engineering

FROM: The Faculty of the School of Electrical and Computer Engineering

RE: New Undergraduate-Level Course

The faculty of the School of Electrical and Computer Engineering has approved the following new course. This action is now submitted to the Engineering Faculty with a recommendation for approval.

ECE 337 ASIC Design Laboratory
Class 1, Lab 3, Credit 2
Prerequisites: ECE 264 and ECE 270

Course Description: Introduction to standard cell design of VLSI (Very Large Scale Integration) digital circuits using the VHDL hardware description language (Very High Speed Integrated Circuits Hardware Description Language). Emphasis on how to write VHDL that will map readily to hardware. Laboratory experiments using commercial grade computer-aided design (CAD) tools for VHDL based design, schematic based logic entry, logic and VHDL simulation, automatic placement and routing, timing analysis, and testing.

Reason: This is a required course for the Computer Engineering degree, and it will continue to be offered for the foreseeable future.

Course History: This course was offered as an experimental course as ECE 495D in the Spring 2002, Fall 2002, Spring 2003, Fall 2003, Spring 2004, and Fall 2005 semesters with enrollments of 79, 50, 99, 57, 85, and 32 students respectively.

Mark J.T. Smith

Professor and Head

APPROVED BY THE FACULTY OF THE
B
CFR Minutes 1014
Date 12-9-05
Chairman CFR Robert E Montgomery

Supporting Documentation:

Required Text(s):

1. *VHDL for Logic Synthesis*, 2nd Edition, Andrew Rushton, John Wiley & Sons, Inc., 1998, ISBN No. 0-471-98325-X.

Recommended Reference(s):

1. *Digital Design Principles and Practices*, 4th Edition, John F. Wakerly, Prentice Hall, 2006, ISBN No. 0-13-186389-4.

Course Outcomes:

A student who successfully fulfills the course requirements will have demonstrated an ability to:

i. understand and use major syntactic elements of VDHL - entities, architectures, processes, functions, common concurrent statements, and common sequential statements.
ii. design combinational logic in a variety of styles including: schematic, structural VHDL, and behavioral VHDL, as well as demonstrate an awareness of timing and resource usage associated with each approach.
iii. design common sequential functions: flip-flops, registers, latches, and state-machines.
iv. create a VDHL test bench and use it to test/verify a sequential VHDL design of moderate complexity.
v. place, route, and verify timing of a standard cell design.
vi. draw, given commented VHDL code of moderate complexity, a corresponding RTL (Register Transfer Level) block diagram.
vii. use, modify, and create scripts to control the synthesis process.
viii. use different design styles, constraints, and optimization options to achieve required synthesis results.
ix. explain the difference between various ASIC (Application Specific Integrated Circuit) design approaches - standard cell, full custom, and programmable devices.
x. prepare functional and interface requirements for blocks within a sequential system design.
xi. create the hierarchical decomposition of a sequential design.

xii. work in a team and negotiate the division of labor.
xiii. gain familiarity with the use and purpose of design reviews.
xiv. document the final architecture, design statistics (area, timing), and test results.

Assessment Method for Course Outcomes:

Satisfaction of outcomes i-v, vii, and viii is demonstrated through completion of lab exercises during weeks 7 through 9. Outcomes vi and ix are assessed on written tests. Outcomes x through xiv are satisfied through completion of a final design project.

Engineering Design Content:

Establishment of objectives and criteria: For the final project, students are given a general system specification for which students must define an architecture and specification for individual functional units within the architecture.

Synthesis: Given functional and interface requirements, students use VHDL code to implement a circuit design to satisfy those requirements. Early in the semester, students are provided with detailed specifications for individual blocks. For the final project, students have to conceive of their design RTL (Register Transfer Level) block diagram, and implement and implement each of those blocks.

Analysis: Given a design in either RTL or gate level form, students are required to identify timing delay paths, and prepare timing and area budgets based on their analyses of the design. Results are compared to automated reports which can be extracted from their designs.

Testing and Evaluation: Students practice the development and use of automated or semi-automated test benches for thorough verification of logic designs. These test benches can be applied at each stage of the design process. Note: in industrial practice, ASIC designs are verified extensively by means of simulation and design rule checks because an ASIC fabrication run is extremely expensive and time consuming.

Engineering Design Considerations:

Economic: final projects are required to target either area or timing optimization, both of which have economic implications. Area strongly influences manufacturing cost and

design yield. Timing strongly influences marketability of many products. Students are also expected to be able to identify and explain implementation alternatives (ASIC, FPGA [Field-Programmable Gate Array], gate array, etc.) appropriate for a particular set of design objectives.

Manufacturability: Design techniques and automated processes practiced in this course are similar to those used in industry to ensure manufacturability.

Lab Outline:

Week(s)	Topic(s)
1	Lecture: VHDL intro; Design software introduction
2-4	VHDL techniques for synthesis of combinational logic, sequential logic, and test bench design; Debugging tips and techniques
5-8	System level design techniques; RTL Design approach; Use of multiple state machines; Design of simple controllers; VHDL techniques to facilitate design re-use; System level design exercises - first a simple controller such as a traffic-light controller, then a more advanced system such as an I2C bus interface or UART. Mid-term exam. Present specifications for final project
9-10	Design budgeting (area and time) techniques; Students submit architecture description for final project
11-12	Review of CMOS logic; Introduction to digital CMOS IC layout; Design review in lab.
13-15	Current issues in ASIC design; Timing verification; Mid-term exam. Final project reports and demonstrations in lab.