Engineering Faculty Document No. 18-18 September 28, 2017 Page 1 of 1

TO: The Faculty of the College of Engineering

FROM: School of Electrical and Computer Engineering of the College of Engineering

RE: New Graduate Course, ECE 60645 High-speed Semiconductor Devices

The faculty of the School of Electrical and Computer Engineering has approved the following new course. This action is now submitted to the Engineering Faculty with a recommendation for approval.

ECE 60645 High-speed Semiconductor Devices

Sem. 2, Lecture 3, Cr. 3.

Prerequisite: ECE 60600 or taking ECE 60600 at the same time

Prerequisite by Topic: ECE 25500 and ECE 30500 level of semiconductor physics and devices

Description: As semiconductor device geometry miniaturizes, the device becomes faster and some devices move into the quantum-effect region. These high-speed devices are the key components for future electronic systems in communications, computers, control, and consumer applications. This course covers the physics and operational principles of these devices to meet the needs of microelectronics in the 21th century. This course emphasizes the integration of the state-of-the-art technologies such as high-k dielectrics, SiGe, SiC and GaN devices. This course is intended for graduate students in science and engineering who are either i) interested in pursuing research in semiconductor materials, structures or devices, or ii) seeking the broad device background on the state-of-the-art technologies for a future R&D career in the microelectronic industry.

Reason: This is the course above ECE 60600 and is used for graduate students to broad their knowledge on modern semiconductor devices. We expect the students having the knowledge on fundamentals of semiconductor materials and the basic concepts of field-effect transistors and bipolar junction transistors.

.

Michael R. Melloch, Associate Head School of Electrical and Computer Engineering

Office of the Desisters
Office of the Registrar
FORM 400 PEVA 440
FORM 40G REV. 4/13

PURDUE UNIVERSITY REQUEST FOR ADDITION, EXPIRATION, OR REVISION OF A GRADUATE COURSE (50000-60000 LEVEL)

DEPARTMENT	nputer Engineeri	ng EFF	ECTIVE SESSION	Spring	2017		
INSTRUCTIONS: Please check the items			uest.	- CETTIN			
	and the second sec	its (complete proposal		7	7. Change in course	attributes	
2. Add existing cours					3. Change in instruct		
3. Expiration of a cou		i oumpuo). Change in course		
4. Change in course				_	0. Change in course		
					 Change in course Change in semest 		
5. Change in course							
6. Change in course	credit/type			L 1.	2. I ransfer from one	department to another	
PROPOSED:	EX	STING:			TEF	RMS OFFERED	
Subject Abbreviation ECE		bject Abbreviation			Che	eck All That Apply:	
	**				Fall	Spring Summer	
	60645 c	una Number			Name and Address of the Address of t	JS(ES) INVOLVED	
Course Number	00045	ourse Number	2 ¹				
					Calumet	N. Central	
Long Title LHigh-speed Semicor	nductor Devices				Cont Ed	Tech Statewide	
Ulinh an and Comission	Luste Davias				Ft. Wayne	V. Lafayette	
Short Title High-speed Semicond		amilled (20 CUADACTERS ON	11.20		Indianapolis		
Abbreviated title will be entered by t	the Office of the Registrar I	omitted. (30 CHARACTERS ON	ily)	1			1
CREDIT TYPE			COURSE ATT	RIBUTES:	Check All That Apply		1
1. Fixed Credit: Cr. Hrs.	1 Pass	Not Pass Only			Approval Type		
2. Variable Credit Range:		actory/Unsatisfactory Only	H	-		structor	
-							
Minimum Cr. Hrs	3. Repe			Variable Tit	le		
(Check One) To Or		aximum Repeatable Credit:		Honors		H	
Maximum Cr. Hrs		by Examination	9.	Full Time P	rivilege		
3. Equivalent Credit: Yes 🗌 No 🗹	(3) 21 SP28743	Coop Lab R	ate Request 10.	Off Campus	s Experience		
4. Thesis Credit: Yes 🗌 No 🗸	Include	comment to explain fee					
Schedule Type Minutes M	leetings Per Wee	s % of Credit				and the state of the	1
Per Mtg	Week Offer	ed Allocated			Г	Cross-Listed Courses	1
Lecture 3	50	16 100			÷		
Recitation							
Presentation					-		4
Laboratory							
Studio							
Distance					i i i i i i i i i i i i i i i i i i i		1
Clinic							
Experiential							
Research		· · · · · · · · · · · · · · · · · · ·					
Ind. Study							
					L		1
COURSE DESCRIPTION (INCLUDE REQUISIT							
As semiconductor device geometry miniaturizes systems in communications, computers, control							
century. This course emphasizes the integration							
engineering who are either i) interested in pursu	uing research in semico	ductor materials, structures	or devices, or ii) seekin	g the broad o	levice background on the s	tate-of-the-art technologies for a futur	re
*COURSE LEARNING OUTCOMES:							
attached							
ы							
Calumet Department Head	Date Calume	School Dean	Date	C	alumet Director of Graduate	e Studies	Date
		Octored D.				unte Otudine	Dete
Fort Wayne Department Head	Date Fort Wa	yne School Dean	Date	Fo	ort Wayne Director of Grad	uate Studies	Date
A							
Indianapolis Department Head	Date Indiana	oolis School Dean	Date		IPUI Associate Dean for Gr	aduate Education	Date
naanapois bepartment neat		Salo Concor Dearn	Dale	iu			Date
North Central Department Head	Date North C	entral School Dean	Date	N	orth Central Director of Gra	duate Studies	Date
111							
Ma O MA MI	1 1-						
MAKING KALA 11	15/17						
West Lafayette Department Head	Date West	fayette College/School Dear	n Date			Council	Date
West Lalayette Department Head		ayoue conege/ouriou Deal	, Dale	D	ate Approved by Graduate	Council	Date
Graduate Area Committee Convener	Date Gradua	e Dean	Date	G	raduate Council Secretary		Date
				14	/est Lafayette Registrar		Date
1					,		
		OFFICE CT	THE REGISTRA				

Course Description—ECE 60645

As semiconductor device geometry miniaturizes, the device becomes faster and some devices move into the quantum-effect region. These high-speed devices are the key components for future electronic systems in communications, computers, control, and consumer applications. This course covers the physics and operational principles of these devices to meet the needs of microelectronics in the 21th century. This course emphasizes the integration of the state-of-the-art technologies such as high-k dielectrics, SiGe, SiC and GaN devices. This course is intended for graduate students in science and engineering who are either i) interested in pursuing research in semiconductor materials, structures or devices, or ii) seeking the broad device background on the state-of-the-art technologies for a future R&D career in the microelectronic industry.

Learning Outcomes—ECE 60645

- a. Knowledge and Scholarship: This course is intended for graduate students in MN and related areas who are either i) interested in pursuing research in semiconductor materials, structures or devices, or ii) seeking the broad device background on the-state-of-the-art technologies for a future R&D career in the microelectronic industry. The students are required to understand the III-V compound semiconductor epitaxy technologies, dielectric technologies, III-V HEMTs and HBTs in depth about fabrication, process and device physics, scaled CMOS devices and also microwave, photonic and power devices. We have mid-term and final exams to test these basic concepts. We also have regular homework assignments.
- b. Communication: We have the discussion to do research and presentation to strengthen the students' communication skill and critical thinking. For example, we research on f_T and fmax high-speed matrix on GaAs HEMTs, InP HEMTs, GaN HEMTs, graphene FETs and MoS₂ FETs.
- c. Critical Thinking: The students are required to search and study the state-of-the-art device work published at IEDM, VLSI, EDL or IEEE TED. They choose some interesting topics and organize the materials into a 15-20 minutes presentation. They will discuss the pros and cons of the new technologies compared to the existing technologies. In this way, their critical thinking skill is enhanced.
- d. Ethical and Responsible Research or Professional and Ethical Responsibility: The discussion sessions are independent topics which assesses the professional and ethical responsibility. The presentation is similar to the formal conference presentation. I ask the students have to cite other people's work professionally. They can learn the professional and ethical responsibility during this training.

Supporting Document to the Form 40G for a New Graduate Course

To: Purdue University Graduate Council

From: Faculty Member: Peide Ye

Department: Electrical and Computer Engineering

Campus: West Lafayette

Date:

Subject: Proposal for New Graduate Course

Contact for information	Name:	Matt Golden
if questions arise:	Phone:	494-3374
	Email:	goldenm@purdue.edu
	Address:	EE Building, Room 135

Course Subject Abbreviation and Number: ECE 60645

Course Title: High-speed Semiconductor Devices

Course Description:

As semiconductor device geometry miniaturizes, the device becomes faster and some devices move into the quantum-effect region. These high-speed devices are the key components for future electronic systems in communications, computers, control, and consumer applications. This course covers the physics and operational principles of these devices to meet the needs of microelectronics in the 21th century. This course emphasizes the integration of the state-of-the-art technologies such as high-k dielectrics, SiGe, SiC and GaN devices. This course is intended for graduate students in science and engineering who are either i) interested in pursuing research in semiconductor materials, structures or devices, or ii) seeking the broad device background on the state-of-the-art technologies for a future R&D career in the microelectronic industry.

Semesters Offered:

For the benefit of graduate student plan of study development, how frequently will this prototype be offered? Which semesters? Spring Semester Odd Years

A. Justification for the Course:

Provide a complete and detailed explanation of the need for the course (e. g., in the preparation of students, in providing new knowledge/training in one or more topics, in meeting degree requirements, etc.), how the course contributes to existing majors and/or concentrations, and how the course relates to other graduate courses offered by the department, other departments, or interdisciplinary programs.

Justify the level of the proposed graduate course (500- or 600-level) including statements on, but not limited to: (1) the target audience, including the anticipated number of undergraduate and graduate students who will enroll in the course; and (2) the rigor of the course.

• This is the course above ECE 606 and is used for graduate students to broad their knowledge on modern semiconductor devices. We expect the students having the knowledge on fundamentals of semiconductor materials and the basic concepts of field-effect transistors and bipolar junction transistors.

Use the following criteria:

Graduate Council policy requires that courses at the 50000 level in the Purdue system should be taught at the graduate level and meet four criteria: a) the use of primary literature in conjunction with advanced secondary sources (i.e., advanced textbooks); b) assessments that demonstrate synthesis of concepts and ideas by students; c) demonstrations that topics are current, and; d) components that emphasize research approaches/methods or discovery efforts in the course content area (reading the research, critiquing articles, proposing research, performing research). Such courses should be taught so that undergraduate students are expected to rise to the level of graduate work and be assessed in the same manner as the graduate students.

- Anticipated enrollment
 - o Undergraduate
 - Graduate 15 (More students want to be registered in spring semester 2017)

B. Learning Outcomes and Method of Evaluation or Assessment:

0

ECE Graduate Learning Outcomes:

a. Knowledge and Scholarship: This course is intended for graduate students in MN and related areas who are either i) interested in pursuing research in

semiconductor materials, structures or devices, or ii) seeking the broad device background on the-state-of-the-art technologies for a future R&D career in the microelectronic industry. The students are required to understand the III-V compound semiconductor epitaxy technologies, dielectric technologies, III-V HEMTs and HBTs in depth about fabrication, process and device physics, scaled CMOS devices and also microwave, photonic and power devices. We have mid-term and final exams to test these basic concepts. We also have regular homework assignments.

- b. Communication: We have the discussion to do research and presentation to strengthen the students' communication skill and critical thinking. For example, we research on f_T and fmax high-speed matrix on GaAs HEMTs, InP HEMTs, GaN HEMTs, graphene FETs and MoS₂ FETs.
- c. Critical Thinking: The students are required to search and study the state-ofthe-art device work published at IEDM, VLSI, EDL or IEEE TED. They choose some interesting topics and organize the materials into a 15-20 minutes presentation. They will discuss the pros and cons of the new technologies compared to the existing technologies. In this way, their critical thinking skill is enhanced.
- d. Ethical and Responsible Research or Professional and Ethical Responsibility: The discussion sessions are independent topics which assesses the professional and ethical responsibility. The presentation is similar to the formal conference presentation. I ask the students have to cite other people's work professionally. They can learn the professional and ethical responsibility during this training.
- Methods of Instruction
 - o Lecture
- Will/can this course be offered via Distance Learning?

No plan at this moment

• Grading Criteria

Grading criteria (select from checklist); include a statement describing the criteria that will be used to assess students and how the final grade will be determined. Add and delete rows as needed.

- 2 exams including mid-term and final one.
- Discussion session with the presentations by the students after doing research on active research topics
- Homework weekly

- We don't have resource to do lab exercises at cleanroom at Birck. However, we will have a cleanroom tour and introduce the equipment functions and operations to the students
- Attendance/participation is strongly required and checked.
- Mid-term exam 40%, Final Exam 40%, Presentation/Research 10%, Homework 10%

C. Prerequisite(s):

List prerequisites and/or experiences/background required. If no prerequisites are indicated, provide an explanation for their absence. Add bullets as needed.

- ECE 606 or taking ECE 606 at the same time
- Prerequisite by Topic: ECE 255 and ECE 305 level of semiconductor physics and devices

D. Course Instructor(s):

Provide the name, rank, and department/program affiliation of the instructor(s). Is the instructor currently a member of the Graduate Faculty? (If the answer is no, indicate when it is expected that a request will be submitted.) Add rows as needed.

Name	Rank	Dept.	Graduate Faculty or expected date
Peide Ye	Professor	ECEN	Yes

E. Course Outline:

Provide an outline of topics to be covered and indicate the relative amount of time or emphasis devoted to each topic. If laboratory of field experiences are used to supplement a lecture course, explain the value of the experience(s) to enhance the quality of the course and student learning. For special topics courses, include a sample outline of a course that would be offered under the proposed course. (This information must be listed and may be copied from syllabus).

Weeks	Principal Topics
1	Overview of Modern Semiconductor Devices
	Semiconductor Epitaxial Growth (MBE and MOCVD)

1	Chemical Vapor Deposition (CVD)
	Atomic Layer Deposition (ALD); High-k dielectrics for ultimate CMOS
1	Homogeneous Field-Effect Transistors (III-V MESFET)
	Homogeneous Field-Effect Transistors (III-V MESFET and JFET)
1	Heterostructure Field-Effect Transistors (III-V HFET)
	Heterostructure Field-Effect Transistors (III-V HEMT)
1	Discussion on III-V MOSFET Research
	Discussion on GaN HEMT Research
1	Bipolar Transistor Operation, Silon Bipolar Transistor
1	Heterojunction Bipolar Transistor (III-V HBT) Scaled MOSFETs, CMOS/Bi CMOS
	Strain-Si and SiGe based MOSFETs
1	Discussion on Ge MOSFET Research
	Discussion on CNTFET Research
1	Power MOSFET, Si LDMOSFET
1	SiC Power Devices, GaN Power Devices
1	Quantum-Effect Devices (Resonant-Tunneling Diodes and RTBTs) Hot-Electron Devices
1	Discussion on Single-Dlectron-Transistors (SET) and Quantum
	Dots Research
1	Active Micowave Devices
1	Discussion on THz transistor Research (i.e. UIUC work) High-Speed Photonic Devices (LED, Pin Photodetector, Avalanche
	Photodetector)
1	High-Speed Photonic Devices (Laser)
	Discussion on VCSEL Research
1	Review

F. Reading List (including course text):

A primary reading list or bibliography should be limited to material the students will be required to read in order to successfully complete the course. It should not be a compilation of general reference material.

A secondary reading list or bibliography should include material students may use as background information.

Primary Reading List

o Class Notes

Secondary Reading List

S.M.Sze,"High-speed Semiconductor Devices"

G. Library Resources

Describe any library resources that are currently available or the resources needed to support this proposed course.

• The course text book will be on reserve at the library. All additional assigned readings will be made available to the students electronically through Blackboard or other means.

H. Course Syllabus

(While not a necessary component of this supporting document, an example of a course syllabus is available, for information, by clicking on the link below, which goes to the *Graduate School's Policies and Procedures Manual for Administering Graduate Student Program.* See Appendix K.

http://www.purdue.edu/gradschool/faculty/documents/Graduate School Policies a nd Procedures Manual.pdf

ECE 695V High-Speed Semiconductor Devices—Spring 2019 Schedule Time: Tuesday and Thursday 9:00-10:20 am Credit:3 Location:EE226

Data	Topics
1/8 T	Overview of Modern Semiconductor Devices
1/10 Th	Semiconductor Epitaxial Growth (MBE and MOCVD)
1/15 T	Chemical Vapor Deposition (CVD)
1/17 Th	Atomic Layer Deposition (ALD); High-k dielectrics for ultimate CMOS
1/22 T	Homogeneous Field-Effect Transistors (III-V MESFET)
1/24 Th	Homogeneous Field-Effect Transistors (III-V MESFET and JFET)
1/29 T	Heterostructure Field-Effect Transistors (III-V HFET)
1/31 Th	Heterostructure Field-Effect Transistors (III-V HEMT)
2/5 T	Discussion on III-V MOSFET Research
2/7 Th	Discussion on GaN HEMT Research
2/12 T	Bipolar Transistor Operation, Silon Bipolar Transistor
2/14 Th	Heterojunction Bipolar Transistor (III-V HBT)
2/19 T	Scaled MOSFETs, CMOS/Bi CMOS
2/21 Th	Strain-Si and SiGe based MOSFETs

2/26 T	Discussion on Ge MOSFET Research
2/28 Th	Discussion on CNTFET Research
3/5 T	Power MOSFET
3/7 Th	Si LDMOSFET
3/12 T	SiC Power Devices
3/14 Th	GaN Power Devices
3/19 T	Quantum-Effect Devices (Resonant-Tunneling Diodes and RTBTs)
3/21 Th	Hot-Electron Devices
3/26 T	Discussion on Single-Electron-Transistors (SET) and Quantum Dots Research
3/28 Th	Active Micowave Devices
4/2 T	Discussion on THz transistor Research (i.e. UIUC work)
4/4 Th	High-Speed Photonic Devices (LED, Pin Photodetector, Avalanche Photodetector)
4/9 T	High-Speed Photonic Devices (Laser)
4/11 Th	Discussion on VCSEL Research
4/16 T	RF Measurements
4/18 Th	State-of-the-Art CMOS (FinFETs and GAAFETs)
4/23 T	2D Materials and Devices
4/25 Th	Review Session
4/30 T	Final Exam

Course Outcomes:

- 1. Produce homework and presentations at the course that use appropriate formats, knowledge of electronic materials and devices, and documentation styles while controlling the right technical terms, writing skill including grammar and spelling.
- 2. Demonstrate an understanding of technical contents of the course and writing reports as a process that includes multiple drafts, collaboration, feedback, and reflection.
- 3. Examine critically, summarize, apply, analyze, and synthesize information as the basis for developing original ideas and claims.
- 4. Demonstrate proficiency in identifying, reading, evaluating, analyzing, and using reliable sources of technical contents of this course.

Grading:

We make the assignment weightings and mappings from scores to letter grades as following. We assign 40% weight on mid-term exam, 40% weight on final exam and 20% for homework, lecture attendance and discussion session presentation. The letter grade A refers to 90/100 or above; the letter grade B refers to 80/100 or above but less than 90/100; the letter grade C refers to 70/100 or above but less than 80/100; the letter grade D refers to 60/100 or above but less than 70/100; the letter grade F (fail) refers to less than 60/100. Any academic dishonest behavior will lead to the letter grade F.

Offering History: Spring 2021 – 10, Spring 2019 - 8