Engineering Faculty Document No. 15-07
May 16, 2007

TO: The Faculty of the College of Engineering
FROM: The Faculty of the School of Electrical and Computer Engineering
RE: ECE 68800 Changes in Terms Offered, Requisites, and Description

The faculty of the School of Electrical and Computer Engineering has approved the following changes in ECE 68800. This action is now submitted to the Engineering Faculty with a recommendation for approval.

From: **ECE 688 VLSI Testing And Verification**
Sem. 1 and 2. Class 3, cr. 3. Offered every third semester.
Prerequisite: ECE 559. Authorized equivalent courses or consent of instructor may be used in satisfying course pre- and co-requisites.

Description:
Discusses different aspects of VLSI testing and formal verification of designs. Design and manufacturing defect models are introduced along with test generation and fault simulation algorithms targeting the different fault models. Both combinational and sequential logic testing are covered, and different synthesis for testability schemes such as BIST (Built-In-Self-Test), scan path design, etc., are introduced. Other new and emerging test and verification techniques also are discussed.

To: **ECE 68800 VLSI Testing And Verification**
Sem. 2. Class 3, cr. 3
Prerequisite: ECE 27000 and ECE 55900

Description:
This course discusses different aspects of VLSI testing and formal verification of designs. Design and manufacturing defect models are introduced along with test generation and fault simulation algorithms targeting the different fault models. Both combinational and sequential logic testing are covered, and different synthesis for testability schemes such as BIST (Built-In-Self-Test), scan path design, etc. are introduced. Other new and emerging test and verification techniques are also discussed.

Reason: The course description and requisites have been changed to reflect the updated content of the course. The terms offered has been changed to reflect the actual offering schedule. Will be offered in odd numbered years.

M. J. T. Smith, Head
School of Electrical and Computer Engineering

ECE 688 VLSI Testing and Verification

Lecture Hours: 3. Credits: 3.

Normally Offered: Spring - odd years

Prerequisites: ECE 270 and ECE 559, or consent of instructor

Catalog Description: This course discusses different aspects of VLSI testing and formal verification of designs. Design and manufacturing defect models are introduced along with test generation and fault simulation algorithms targeting the different fault models. Both combinational and sequential logic testing are covered, and different synthesis for testability schemes such as BIST (Built-In-Self-Test), scan path design, etc. are introduced. Other new and emerging test and verification techniques are also discussed.

Required Text(s): None.

Lecture Outline:

Lectures	*Principal Topics*
2	Design Flow of VLSI Systems: (1) Design and manufacturing defect models (2) Simulation based design verification
3	Fault Simulation: (1) Parallel; (2) Deductive; (3) Concurrent.
2	Functional Testing Methodologies: (1) Exhaustive testing; (2) Pseudo-exhaustive testing.
12	Structure Based Testing: (1) Fault model based testing: (A) Stuck-at faults; (B) Bridging faults; (C) Stuck-open faults; (D) Delay faults (2) Fault Grading (3) Automatic Test Pattern Generation Algorithms: (A) D-Algorithms; (B) PODEM; (C) FAN, etc.
2	Sequential Machine Testing: (1) Machine identification experiments (2) Modified PODEM and D-algorithms
6	Quiescent Current Testability Methods; deep submicron challenges
8	Design for Testability Methods: (1) Testable combinational/sequential circuits (2) Scan path design (3) Partial scan (4) Built-in Self Test (BIST) (5) Data compaction techniques
6	Introduction to Formal Design Verification
3	On-Line Testing Methods: (1) Self-checking circuits (2) Error detecting/correcting codes