

**TO:** The Engineering Faculty  
**FROM:** The Faculty of the Elmore Family School of Electrical and Computer Engineering  
**RE:** New undergraduate course – ECE 40655

The Faculty of the Elmore Family School of Electrical and Computer Engineering has approved the following new undergraduate course. This action is now submitted to the Engineering Faculty with a recommendation for approval.

FROM (IF ALREADY OFFERED WITH TEMPORARY NUMBER):

Not from a temporary number but so many changes to ECE 45600 that we are creating a new course at the request of the Office of the Registrar

TO:

ECE 40655 Digital Integrated Circuit Analysis and Design

3 total credits; 3 credit lecture

As applied to digital integrated circuits, the MDs transistor is studied in depth-from its fabrication to its electrical characteristics. Combinational, sequential, and dynamic logic circuits are considered. While the focus of the course is on CMOS technology, bipolar, nMOS, and BiCMOS circuits are introduced as well. SPICE is used as both an analysis and design tool. Semiconductor memory circuits are also discussed.

Requisites: ECE 20002 and ECE 30500 [May be taken concurrently]

Learning Outcomes:

1. demonstrate a basic knowledge of CMOS IC processing and layout.]
2. demonstrate an understanding of CMOS inverter operation, both static and dynamic.
3. demonstrate an understanding of CMOS combinational logic circuit design and analysis.
4. demonstrate an understanding of basic CMOS arithmetic circuits.
5. demonstrate an understanding of CMOS digital array design.
6. demonstrate an understanding of basic CMOS sequential logic analysis.
7. demonstrate an understanding of memory technologies and designs.
8. demonstrate an ability to design, and analyze and simulate a CMOS digital circuit.

RATIONALE:

This course ran as ECE 45600 but has evolved over time and it is time to update it in the catalog, including removing material on bipolar transistors and circuit implementations using it to more relevant up-to-date material including signal circuits, CMOS Comparators, data converters, hold circuits and switched-capacitor circuits.

A handwritten signature in black ink on a light gray background. The signature reads "T.S. Mithuna" followed by a long, horizontal flourish.

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Mithuna Thottethodi

Associate Head of Teaching and Learning

Professor of the Elmore Family School of Electrical and Computer Engineering

Link to Curriculog entry: <https://purdue.curriculog.com/proposal:32657/form>

## ECE40655 Syllabus, Spring 2024

- Course:** ECE 40655 Digital Integrated Circuit Analysis and Design
- Instructor:** Prof. Saeed Mohammadi  
Office: Birck 2264, email: [saeedm@purdue.edu](mailto:saeedm@purdue.edu), Tel: 494-3557,  
Professor's office hours: to be determined via zoom
- CAD TA** Dali Lai, email: [lai127@purdue.edu](mailto:lai127@purdue.edu), Office hours: to be determined
- Textbook:** Digital Integrated Circuits, A design Perspective, 2<sup>nd</sup> edition, J.M. Rabaey, A. Chandrakasan, B. Nikolic, Prentice Hall
- + Instructor's notes available on Brightspace
- Schedule:** Tuesdays/Thursdays 12:00 – 1:15pm, Brown EE 222
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|------------|--|
| Week 1-2:  | Chapters 1, 2 (Review of technology and devices) |
| Week 3:    | Chapter 3 (Interconnect)                         |
| Week 4-5:  | Chapter 4 (Inverter)                             |
| Week 6-7:  | Chapter 5 (Combinational logic)                  |
| Week 8:    | Review, Midterm 1                                |
| Week 9-10: | Chapter 6 (Sequential Logic)                     |
| Week 11:   | Chapter 7 (Designing Arithmetic Building Blocks) |
| Week 12:   | Chapter 8 (Digital Circuit Implementation)       |
| Week 13:   | Chapter 9 (Interconnect – again!)                |
| Week 14:   | Chapter 10 (Memory and Array Structures)         |
| Week 15:   | Review, Midterm 2                                |
| Week 16:   | Project Presentations                            |
- Attendance Policy:** All students are required to upload a photo of themselves to their Brightspace page (Do it asap). While attendance in the class and on-line lectures is not mandatory, data from previous years shows that students who attended the lectures receive better grades. Do not come to lectures if you are sick. Missing an exam would require a letter from PUSH.
- Academic Integrity:** Academic integrity is one of the highest values that Purdue University holds. Individuals are encouraged to alert university officials to potential breaches of this value by either emailing [integrity@purdue.edu](mailto:integrity@purdue.edu) or by calling 765-494-8778. While information may be submitted anonymously, the more information is submitted the greater the opportunity for the university to investigate the concern. More details are available on our course Brightspace under University Policies and Statements.
- Learning Outcome:**  
*A student who successfully fulfills the course requirements will have demonstrated:*

1. a basic knowledge of CMOS IC processing and layout.]
2. an understanding of CMOS inverter operation, both static and dynamic.
3. an understanding of CMOS combinational logic circuit design and analysis.
4. an understanding of basic CMOS arithmetic circuits.
5. an understanding of CMOS digital array design.
6. an understanding of basic CMOS sequential logic analysis.
7. an understanding of memory technologies and designs.
8. an ability to design, and analyze and simulate a CMOS digital circuit.

Simulation: Cadence Spectre RF. Cadence 45nm PDK (45nm CMOS technology) is used for this course. Note that we reserve the right to check your class account at any time during the semester.

Grading: Homework (8 assignments) 20%  
 Your assignments include analysis, design, and simulations of digital circuits. We will not only pay attention to your results but most importantly to the approach in solving problems. In this course, academic honesty is of outmost importance. You are welcome to discuss how to solve a certain problem with your classmates. Do not copy HW problems from your classmate. Do not provide your HW to a classmate.

Exams (2 midterms) 40%  
 Midterm exams focus on your ability to analyze digital circuits. Examples of previous midterms will be provided for your convenience.

Projects x 2 40%  
 A major part of the course is your individual projects. The topics will be provided to you. You are responsible for doing research and literature search, design, optimization and simulation of the circuits. You will be asked to provide a report for each project and do a professional presentation for project 2. Note that we reserve the right to check your class account at any time during the semester.

- No make-up exam for midterms 1 and 2 will be scheduled. There will be no final exam.
- An A-4 sheet of formula is allowed for midterms.
- To pass the course, you must have passing grades from theoretical (exams) and simulation (projects) parts. Possible grades in this course are A+ (>96%), A (>92%), A- (>88%), B (>80%), C (>70%), D (>60%) and F (<60%).
- The final date to withdraw from a course with a W for Spring 2024 is Friday, April 22<sup>nd</sup>.

In the event of a major campus emergency, course requirements, deadlines, and grading percentages are subject to changes that may be necessitated by a revised semester calendar or other circumstances.

Here are ways to get information about changes in this course:

[saeedm@purdue.edu](mailto:saeedm@purdue.edu)

<https://purdue.brightspace.com/d21/home/599863>

email [saeedm@purdue.edu](mailto:saeedm@purdue.edu) or check Brightspace website

*Mental Health/Wellness Policy:*

If you find yourself beginning to feel some stress, anxiety and/or feeling slightly overwhelmed, try [WellTrack](#). Sign in and find information and tools at your fingertips, available to you at any time.

If you need support and information about options and resources, please contact or see the [Office of the Dean of Students](#). Call 765-494-1747. Hours of operation are M-F, 8 a.m.- 5 p.m.

If you find yourself struggling to find a healthy balance between academics, social life, stress, etc., sign up for free one-on-one virtual or in-person sessions with a [Purdue Wellness Coach at RecWell](#). Student coaches can help you navigate through barriers and challenges toward your goals throughout the semester. Sign up is free and can be done on BoilerConnect.

If you're struggling and need mental health services: Purdue University is committed to advancing the mental health and well-being of its students. If you or someone you know is feeling overwhelmed, depressed, and/or in need of mental health support, services are available. For help, such individuals should contact [Counseling and Psychological Services \(CAPS\)](#) at 765-494-6995 during and after hours, on weekends and holidays, or by going to the CAPS office on the second floor of the Purdue University Student Health Center (PUSH) during business hours.

