Office of the Registrar FORM 40G REV. 9/06

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PURDUE UNIVERSITY

REQUEST FOR ADDITION, EXPIRATION, OR REVISION OF A GRADUATE COURSE (500-600 LEVEL) Print Form

12-01

PEPARTMENT ECE EFFECTIVE SESSION Fall 2008 9

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INSTRUCTIONS: Please check the items below	which describe the purpose of this reque	st.	
New course with supporting doc	nange in course attributes		
			nange in instructional hours
3. Expiration of a course	•		nange in course description
4. Change in course number		L	nange in course requisites
5. Change in course title			nange in semesters offered No change
6. Change in course credit/type			ansfer from one department to another
PROPOSED:	EVICTIMO:		
FRUPUSED.	EXISTING:		TERMS OFFERED Check All That Apply:
Subject Abbreviation	Subject Abbreviation ECE		Summer X Fall Spring
Course Number	Course Number 670		CAMPUS(ES) INVOLVED
	SPECIAL SECURITY OF SECURITY O		Calumet N. Central
Long Title Modeling and Optimization of High	n-Performance interconnects		Cont Ed Tech Statewide
Short Title			Ft. Wayne
Abbreviated title will be entered	d by the Office of the Registrar if omitted.	22 CHARACTERS ONLY)	Indianapolis
CREDIT TYPE		DURSE ATTRIBUTES: Chec	ok All That Annly
1.Fixed Credit: Cr. Hrs.	1. Pass/Not Pass Only		ck All That Apply tration Approval Type
2.Variable Credit Range:	Satisfactory/Unsatisfactory Only		epartment Instructor
Minimum Cr. Hrs	3. Repeatable	8. Variab	and the second s
(Check One) To Or	Maximum Repeatable Credit:	9. Remed	
Maximum Cr. Hrs. 3.Equivalent Credit: Yes No	Credit by Examination Designator Required	10. Honor	s me Privilege
4.Thesis Credit: Yes No	Designator Required Special Fees		me Privilege Impus Experience
Instructional Type Minutes Meetings Pe	r Weeks % of Credit Delivery N	Method Delivery Mediun	n (Audio, Internet,
Per Mtg Week Lecture	Offered Allocated (Asyn. O	Syn.) Live, Text-E	Based, Video) Cross-Listed Courses
Recitation			
resentation	NAME OF TAXABLE PARTY O		
Laboratory			
Lab Prep Studio			
Distance	Postantian postantian processing		
Clinic			
Experiential			-
Research			
Ind. Study			
Pract/Observ	C).		
COURSE DESCRIPTION (INCLUDE REQUISITE	S).		
Sem. 1 of even years.			
Prerequisite: ECE-559 (or equivalent), or consen	t of instructor		
Calumet Department Head Date	Calumet School Dean	Date Cal	lumet Undergrad Curriculum Committee Date
Fort Wayne Department Head Date	Fort Wayne School Dean		rt Wayna Chancellor
Fort Wayne Department Head Date	r ort wayne ochool beari	Date Fo	rt Wayne Chancellor 12/03/08
Indianapolis Department Head Date	Indianapolis School Dean	Doto Tin	idergrad Curriculum Committee
Date		Date On	Date
North Cenifal Department Head / Date	North Central Chancellor	· Date / Da	te Approved by Graduate Council/ / /
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West Lafayette Department Head Date	West Lafayette College/School Dean	Date Gr	aduate Council Secretary Date
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Graduate Area Committee Convener Date	Graduate Dean	/Date We	est Lafayette Registrar Quate
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OFFICE OF THE REGISTRAR

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PURDUE UNIVERSITY

REQUEST FOR ADDITION, EXPIRATION, OR REVISION OF A GRADUATE COURSE (500-600 LEVEL)



Print Form

EFD 12-07

DEPARTMENT ECE

EFFECTIVE SESSION Fall 2008

INSTRUCTIONS: Please check the items below	which describe the purpose of this request.		
1. New course with supporting doc 2. Add existing course offered at at 3. Expiration of a course 4. Change in course number 5. Change in course title 6. Change in course credit/type	uments (complete proposal form) nother campus	8. CC 9. CC X 11. CC	hange in course attributes hange in instructional hours hange in course description hange in course requisites hange in semesters offered ransfer from one department to another
PROPOSED:	EXISTING:		TERMS OFFERED
			Check All That Apply:
Subject Abbreviation Course Number	Subject Abbreviation ECE Course Number 670		Summer X Fall Spring CAMPUS(ES) INVOLVED
Long Title Modeling and Optimization of High	n-Performance Interconnects		Calumet N. Central Cont Ed Tech Statewide
Short Title			Ft. Wayne XW. Lafayette
Abbreviated title will be entered	by the Office of the Registrar if omitted. (22 CHAR	ACTERS ONLY)	
1.Fixed Credit: Cr. Hrs. 2.Variable Credit Range: Minimum Cr. Hrs (Check One) To Or Maximum Cr. Hrs. 3.Equivalent Credit: Yes No A.Thesis Credit: Yes No To The Meetings Per Mtg Week 4.Thesis Credit: Yes Minutes Meetings Per Mtg Week Lecture	1. Pass/Not Pass Only 2. Satisfactory/Unsatisfactory Only 3. Repeatable Maximum Repeatable Credit: 4. Credit by Examination 5. Designator Required 6. Special Fees r Weeks % of Credit Delivery Method (Asyn. Or Syn.)	8. Variab 9. Remer 10. Honor 11. Full Ti 12. Off Ca Delivery Mediur	tration Approval Type epartment Instructor Instructor le Title
Calumet Department Head Date	Calumet School Dean	Date Cal	umet Undergrad Curriculum Committee Date
Fort Wayne Department Head Date	Fort Wayne School Dean	Date For	1 Wayne Chancellor 12/03/08
Indianapolis Department Head Date	Indianapolis School Dean	Date Uni	dergrad Cyfriculum Committee Date
North Central Department Head, Date Mulling 11/13/03	North Central Chancellor	Date Date	te Approved by Graduate Council
West Lafayette Department Head Date	West Lafayette College/School Dean	Date Gra	aduate Council Secretary Date
luate Area Committee Convener Date	Graduate Dean	Date We	st Lafayette Registrar Date

TQ:

The Faculty of the College of Engineering

FROM:

The Faculty of the School of Electrical and Computer Engineering

RE:

ECE 670 Changes in Terms Offered, Prerequisite and Content

The faculty of the School of Electrical and Computer Engineering has approved the following changes in ECE 670. This action is now submitted to the Engineering Faculty with a recommendation for approval.

From:

ECE 670 – Modeling and Optimization Of High-Performance Interconnects

Sem. 1. Class 3, cr. 3.

Prerequisite <u>ECE 559</u>, <u>608</u>. Authorized equivalent courses or consent of instructor may be used in satisfying course pre- and co-requisites.

RLC extraction of VLSI interconnects. Modeling of interconnects as RLC trees or networks. Elmore delay model. Reduced-order modeling: moment matching, Pade approximation, and Krylov-subspace methods. Device modeling with consideration of resistive shielding in the interconnection load. Delay calculation with consideration of devices and interconnects. Repeater insertion and planning at floor planning. Timing-driven placement: zero-slack algorithm for delay budgeting, net-based placement, and path-based placement. High-performance clock synthesis: zero-skew routing, bounded-skew routing and useful-skew routing. Term projects investigating interconnect-related issues are assigned.

To:

ECE 670 - Modeling and Optimization of High-Performance Interconnects

Sem. 1 of even years. Class 3, cr. 3

Prerequisite: ECE 559 (or equivalent), or consent of instructor

RLC extraction of VLSI interconnects. Modeling of interconnects as RLC trees or networks. Elmore delay model. Reduced-order modeling: moment matching, Padé approximation, and Krylov-subspace methods. Device modeling with consideration of resistive shielding in the interconnection load. Delay calculation with consideration of devices and interconnects. Repeater insertion and planning at floorplanning. Timing-driven placement: zero-slack algorithm for delay budgeting, net-based placement, and path-based placement. High-performance clock synthesis: zero-skew routing, bounded-skew routing, and useful-skew routing. Term projects investigating interconnect-related issues are assigned.

Reason:

The course prerequisite, text and content have been changed to reflect the updated

content of the course.

Mark J. T. Smith Head, Electrical and Computer Engineering APPROVED FOR THE FACULTY
OF THE SCHOOLS OF ENGINEERING
BY THE ENGINEERING
CURRICULUM COMMITTEE

ECC Minutes _____

Chairman ECC

Supporting Documentation

ECE 670 - Modeling and Optimization Of High-Performance Interconnects

Required Text: None.

Recommended References:

- 1. Interconnect Analysis and synthesis, C. K. Cheng, J. Lillis, S. Lin & N. Chang, John-Wiley, 2000, ISBN No. 0-471-29366-0.
- 2. Circuits, Interconnections, and Packaging for VLSI, H. B. Bakoglu, Addison-Wesley, 1990, ISBN No. 0-201-06008-6.
- 3. Performance Optimization of VLSI Interconnect Layout, J. Cong, L. He, C.K. Koh, &
- P. H. Madden, Integration, the VLSI Journal, 21, 1996.

Lectures	Principal Topics
2	Introduction: Trends of VLSI Interconnects, Challenges of Interconnect Design
6	Extraction of RLC Parasitics
3	RLC Simulation
2	Elmore Delay Model
7	Reduced Order Modeling
2	Driver Modeling and Delay Calculation
6	Repeater Insertion and Planning
6	Timing-Driven Placement
6	High-Performance Routing
1	Mid-term Exam
3	Term Project Presentation

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