School of Electrical and Computer Engineering
Purdue University
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Education:

PhD	Oct. 2012	Purdue University
MSECE	Aug. 2008	Purdue University
B. Tech.	May 2006	IIT Delhi

Professional and Honorary Society Memberships:

Institute of Electrical and Electronics Engineering (IEEE)
(Electron Device Society)
Senior Member: 2021 - Present
Member: 2012-2021
Student Member: 2005-2012

Honors and Awards:

[1] Seed for Success – Excellence in Research Acorn Award, Purdue University, 2018, 2020.

[2] DARPA Young Faculty Award, 2016.

[3] Monkowski Career Development Professorship in EE, Penn State University, 2014-2017.

[4] TSMC Outstanding Student Research Bronze Award, 2012.

[5] Intel Ph.D. Fellowship, 2009-2010.

[6] Certificate of Recognition for outstanding job during Summer Internship, Intel Labs, 2010.

[7] Outstanding Teaching Assistant Award, Office of Provost, Purdue University, 2007.

[8] Magoon Award for exceptional service as a teaching assistant, School of Electrical and Computer Engineering, Purdue University, 2007.

[9] Certificates of merit for excellent academic performance (top 7% in the batch) in the first, second, sixth and seventh semesters, IIT Delhi, 2002-2006.

[10] National Talent Search Examination (NTSE) Scholarship, 2000.

Professional Experience

Aug. 2020 – Present	Associate Professor of Electrical and Computer Engineering, Purdue University, West Lafayette IN.
Jan. 2018 – Aug. 2020	Assistant Professor of Electrical and Computer Engineering, Purdue University, West Lafayette IN.
Jan. 2014 – Dec. 2017	Assistant Professor of Electrical Engineering, The Pennsylvania State University, University Park PA.
Oct. 2012 – Jan. 2014	Senior Engineer, Qualcomm Inc., San Diego CA.
Sept. 2010 – Oct. 2012	Research Assistant, Nanoelectronics Research Lab, School of Electrical and Computer Engineering, Purdue University, West Lafayette IN.
May 2010 – Sept. 2010	Summer Intern, Intel Corporation, Hillsboro OR.
Aug. 2008 – May 2010	Research Assistant, Nanoelectronics Research Lab, School of Electrical and Computer Engineering, Purdue University, West Lafayette IN.
June 2008 – Aug. 2008	Graduate Instructor, School of Electrical and Computer Engineering, Purdue University, West Lafayette IN.
Jan. 2008 - May 2008	Intern, Advanced Micro Devices Inc., Boston MA.
Aug. 2006 – Dec. 2007	Teaching Assistant, School of Electrical and Computer Engineering, Purdue University, West Lafayette IN.
May 2005 - July 2005	Summer Intern, National Semiconductor, Bangalore, India.

Research Grants and Contracts Received

[1] Co-Principal Investigator (with Kaushik Roy, PI and others), Semiconductor Research Corporation (SRC) and Defense Advanced Research Project Agency (DARPA) - Part of the Center for Brain Inspired Computing (C-BRIC), "Neuromorphic Design Flow," January 1, 2021 – December 31, 2022, $394,542 (Prof. Gupta responsible for $372,833).

[2] Principal Investigator (with Kaushik Roy, Co-PI), National Science Foundation, "FET: Small: Ferroelectric Transistor based Spiking Neural Networks with Adaptive Learning for Edge AI: from Devices to Algorithms," Contract No. 2008412, June, 2020 – May, 2023, $499,998 (Prof. Gupta responsible for $325,591).

[3] Principal Investigator (Single PI Grant), Semiconductor Research Corporation (SRC), "Material, Device and Circuit-Compatible Modeling for Ferroelectric and Anti-Ferroelectric FETs," Contract No. 2020-LM-2959, January, 2020 – December, 2023, $225,000 (Prof. Gupta responsible for $225,000).

[4] Principal Investigator (with Anand Raghunathan, Co-PI and Saptarshi Das, Co-PI), Army Research Office, "Low Power Compact Non-Volatile Memory and In-Memory Compute Architectures enabled by 2D Piezoelectric Transistors," Contract No. W911NF1910488, September, 2019 – August, 2022, $1,169,993 (Prof. Gupta responsible for $359,997).

[5] Co-Principal Investigator (with Ashraf Alam, PI, Peide Ye Co-PI), Applied Materials, "Comprehensive Modeling Framework for Ferroelectric FETs," April, 2019 – October, 2019, $45,000 (Prof. Gupta responsible for $15,000).

[6] Co-Principal Investigator (with Zhihong Chen, PI, Joerg Appenzeller, Co-PI, Joshua Robinson, Co-PI, Robert Wallace, Co-PI, John Heron, Co-PI, Chris Hinkle. Co-PI, Masimmo Fischetti, Co-PI and Stacey Bent, Co-PI), Semiconductor Research Corporation (SRC) and National Institute of Standards and Technology (NIST), "NEW LIMITS – New Materials for Logic, Memory and Interconnects," Contract No. 18100041, January 1, 2018 – December 31, 2022, $4,500,000 (Prof. Gupta responsible for $232,419).

[7] Principal Investigator (Single PI Grant), National Science Foundation (NSF), "SHF: Small: Ferroelectric Transistor based Coupled Oscillators for Non-Boolean Computing," Award No. 1814756, July 15, 2017 – June 30, 2021, $450,000 (Prof. Gupta responsible for $450,000).

[8] Co-Principal Investigator (with Saptarshi Das, PI and Jack Sampson, Co-PI), Semiconductor Research Corporation (SRC) and National Science Foundation (NSF), "E2CDA: Type II: 2D Electrostrictive FETs for Ultra-Low Power Circuits and Architectures," Contract No. 2016-NE-2699 (SRC), ECCS-1640020 (NSF), October 1, 2016 – September 30, 2019-20, $600,000 (Prof. Gupta responsible for $136,000).

[9] Principal Investigator (Single PI Grant), Defense Advanced Research Project Agency (DARPA), "Ultra-Low Power Non-Volatile Processors Enabled by Ferroelectric Transistors," Contract No. D16AP00109, September 15, 2016 – March 14, 2019, $463,295 (Prof. Gupta responsible for $463,295).

[10] Co-Principal Investigator (with Suman Datta, PI), Semiconductor Research Corporation–Global Research Collaboration (SRC-GRC), "Ferroelectric Field Effect Transistor with Steep Switching Slope and Non-Volatile Functionality," Contract No. 2016-LM-2657, January 1, 2016 – December 31, 2018, $300,000 (Prof. Gupta responsible for $75,000).

[11] Co-Principal Investigator (with Suman Datta, PI and Supratik Guha, Co-PI), Semiconductor Research Corporation (SRC) and Defense Advanced Research Project Agency (DARPA) - Part of the Center for Low Energy Systems (LEAST), "Orbital Ordering Driven Threshold Switches for Select Devices in 3D X-Point Memories," Contract No. 202092-PENN, December 1, 2015 – December 31, 2017, $500,000 (Prof. Gupta responsible for $150,000).

PhD Thesis Supervision Completed

Ahmedullah Aziz	August 2019, "Device-Circuit Co-design Employing Phase Transition Materials for Low Power Electronics" ***(Currently an Assistant Professor at The University of Tennessee, Knoxville)***
Sandeep Thirumala	December 2020, "Enabling Logic-Memory Synergy using Integrated Non-Volatile Memory Technologies for Energy Efficient Computing" ***(Currently at Micron)***

Master's Thesis Supervision Completed

Shreya Gupta	Aug. 2017, "Device-Circuit Analysis of Ferroelectric FETs for Low Power Logic" ***(Currently at Intel)***
Niharika Thakuria	Aug. 2018, "2D Electrostrictive FET based Circuits: Compact Modeling and Device-Circuit Co-Design" ***(Currently a Ph.D. student in Gupta's group)***
Sandeep Thirumala	Aug. 2018, "Non-volatile Ferroelectric Transistor based Memory Design: Device-Circuit Analysis Considering Gate Leakage" ***(Continued as a Ph.D. student in Gupta's group)***

Master's Paper Supervision Completed (At Penn State)

Danni Wang	May 2016, "Ferroelectric Transistor based Non-volatile Flip-flops" ***(Currently at General Electric, China)***
Ahmedullah Aziz	May 2016, "Steep Switching Hybrid Phase Transition FETs (Hyper-FET) for Low Power Applications" ***(Continued as a Ph.D. student in Gupta's group)***
Anupriya Chakraborty	Aug. 2018, "Design and Analysis of HYPERFET based DRAM Cell" ***(Currently at Micron)***

Master's and PhD Thesis Students Currently Being Supervised

A. K. Saha	PhD	(Took his preliminary exam in Feb. 2019)
N. Thakuria	PhD	(Took her preliminary exam in April 2020)
K. Cho	PhD	
C. Wang	PhD	
X. Chen	PhD	
T. Paul	PhD	
R. Koduru	PhD	
J. Louis	PhD	
A. Malhotra	PhD	

Publications [Citations: 2662, h-index: 28, i10-index: 61]
($^{G/UG}$ indicate Gupta's graduate/under-graduate student)

Research Book Contributions and Books Published

As Faculty Member

[1] A. Aziz^{G}, S. K. Thirumala^{G}, D. Wang^{G}, S. George, X. Li, S. Datta, V. Narayanan and **S. K. Gupta**, "Sensing Techniques for Ferroelectric based Capacitors and Transistors for Non-Volatile Memory and Logic Applications", Sensing of Non-Volatile Memory Demystified, 2019 (Ed. S. Ghosh), Springer Cham.

[2] X. Li, M. S. Kim, S. George, A. Aziz^{G}, M. Jerry, N. Shukla, J. Sampson, **S. K. Gupta**, S. Datta, and V. Narayanan, "Emerging Steep-Slope Devices and Circuits: Opportunities and Challenges", Beyond-CMOS Technologies for Next Generation Computer Design, 2019 (Ed. R. Topaloglu, H. S. Wong), Springer Cham.

As Graduate Student

[3] **S. K. Gupta** and K. Roy, "Low Power Robust FinFET based SRAM Design in Scaled Technologies" *Circuit Design for Reliability*, 2015 (Ed. R. Reis, Yu Cao and G. Wirth), Springer New York.

As Undergraduate Student

[4] V. Venkataraman, **S. K. Gupta** and M. J. Kumar, "Laser Processing of Materials in Nanotechnology," *Encyclopedia of Nanoscience and Nanotechnology*, 2nd Edition, 2008, (Ed. H.S. Nalwa), American Scientific Publishers, CA, USA.

Serial Journal Articles

As Faculty Member

[1] A. K. Saha[G], and **S. K. Gupta,** "Negative Capacitance Effects in Ferroelectric Heterostructures: A Theoretical Perspective", *Journal of Applied Physics*, vol. 129, issue 8, Feb 2021, DOI: 10.1063/5.0038971. **Tier-1. (Invited) (Cover feature)**

[2] A. K. Saha[G], M. Si, P. D. Ye, and **S. K. Gupta,** "α-In2Se3 based Ferroelectric-Semiconductor Metal Junction for Non-Volatile Memories", *Applied Physics Letters*, vol. 117, no. 183504, Nov 2020, DOI: https://doi.org/10.1063/5.0021395. **Tier-1.**

[3] N. Thakuria[G], D. Schulman, S. Das and **S. K. Gupta**, " 2D Strain FET (2D-SFET) based SRAMs – Part I: Device-Circuit Interactions", *IEEE Transactions on Electron Devices,* vol. 67, no. 11, pp: 4866-4874, Nov 2020, DOI: 10.1109/TED.2020.3022344. **Tier-1**

[4] N. Thakuria[G], D. Schulman, S. Das and **S. K. Gupta**, " 2D Strain FET (2D-SFET) based SRAMs – Part II: Back Voltage Enabled Designs", *IEEE Transactions on Electron Devices,* vol. 67, no. 11, pp: 4875-4883, Nov 2020, DOI: 10.1109/TED.2020.2999317. **Tier-1**

[5] S. K. Thirumala[G], Y. Hung, S. Jain, A. Raha, N. Thakuria[G], V. Raghunathan, A. Raghunathan, Z. Chen and **S. K. Gupta**, "Valley-Coupled-Spintronic Non-Volatile Memories with Compute-In-Memory Support", *IEEE Transactions on Nanotechnology*, vol. 19, pp: 635-647, July 2020, DOI: 10.1109/TNANO.2020.3012550. **Tier-1**

[6] A. K. Saha[G] and **S. K. Gupta** "Multi-Domain Negative Capacitance Effects in Metal-Ferroelectric-Insulator-Semiconductor (Metal) Stacks: A Phase-field Simulation Based Study", *Scientific Reports,* 10, No. 10207, June 2020, https://doi.org/10.1038/s41598-020-66313-1. **Tier-1**

[7] I. Chakraborty, A. Jaiswal, A. K. Saha[G], **S. K. Gupta** and K. Roy, "Pathways to Efficient Neuromorphic Computing with Non-Volatile Technologies", *Applied Physics Reviews,* 7, 021308 (2020); https://doi.org/10.1063/1.5113536. **Tier-1**

[8] S. Jain, **S. K. Gupta** and A. Raghunathan, "TiM-DNN: Ternary in-Memory accelerator for Deep Neural Networks," *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 28, no. 7, pp: 1567-1577, July 2020. DOI: 10.1109/TVLSI.2020.2993045 **Tier-1**

[9] M. Si, A. K. Saha[G], S. Gao, G. Qiu, J. Qin, Y. Duan, J. Jian, C. Niu, H. Wang, W. Wu, **S. K. Gupta** and P. D. Ye, "A ferroelectric semiconductor field-effect transistor", *Nature Electronics*, 2, 580-586 (2019). DOI: https://doi.org/10.1038/s41928-019-0338-7. **Tier-1**

[10] A. A. Saki, S. H. Lin, A. Alam, S. K. Thirumala[G], **S. K. Gupta** and S. Ghosh, "A Family of Compact Non-Volatile Flip-Flops with Ferroelectric FET", *IEEE Transactions on Circuits and Systems – I*, vol. 66, no. 11, pp. 4219-4229, November 2019. DOI: 10.1109/TCSI.2019.2927347. **Tier-1**

[11] M. Si, A. K. Saha[G], P-Y Liao, S. Gao, S. Neumayer, J. Jian, J. Qin, W. Balke, H. Wang, P. Maksymovuch, W, Z, Wu, **S. K. Gupta**, P. D. Ye, "Room Temperature Electrocaloric Effect in 2D Ferroelectric $CuInP_2S_6$ for Nano-refrigerators", *ACS Nano*, vol. 13, no. 8, pp:8760-8765, August 2019. DOI: 10.1021/acsnano.9b01491. **Tier-1**

[12] A. K. Saha[G], K. Ni, S. Dutta, S. Datta and **S. K. Gupta**, "Phase Field Modeling of Domain Dynamics and Polarization Accumulation in Ferroelectric HZO," *Applied Physics Letters*, vol. 114, no.202903, pp. 1-6, May 2019. DOI: 10.1063/1.5092707. **Tier-1**

[13] N. Thakuria[G], A. K. Saha[G], B. Jung and **S. K. Gupta**, "Oscillators Utilizing Ferroelectric-Based Transistors and Their Coupled Dynamics", *IEEE Transactions on Electron Devices*, vol. 66, no. 5, pp. 2415-2423, May 2019. DOI: 10.1109/TED.2019.2902107. **Tier-1**

[14] S. Thirumala[G] and **S. K. Gupta**, "Reconfigurable Ferroelectric Transistor – Part I: Device Design and Operation", *IEEE Transactions on Electron Devices*, vol. 66, no. 6, pp. 2771-2779, June 2019. DOI: 10.1109/TED.2019.2897960. **Tier-1**

[15] S. Thirumala[G] and **S. K. Gupta**, "Reconfigurable Ferroelectric Transistor – Part II: Applications in Low Power Non-Volatile Memories", *IEEE Transactions on Electron Devices*, vol. 66, no. 6, pp. 2780-2788, June 2019. DOI: 10.1109/TED.2019.2912562. **Tier-1**

[16] Z. Shen[UG], S. R. Srinivasa, A. Aziz[G], S. Datta, V. Narayanan and **S. K. Gupta**, "SRAMs and DRAMs with Separate Read-Write Ports Augmented by Phase Transition Materials", *IEEE Transactions on Electron Devices*, vol. 66, no. 2, pp: 929-937, February 2019. DOI: 10.1109/TED.2018.2888913. **Tier-1**

[17] A. Aziz[G] and **S. K. Gupta**, "Threshold Switch Augmented STT MRAM: Design Space Analysis and Device-Circuit Co-design", *IEEE Transactions on Electron Devices*, vol. 65, no. 12, pp: 5381 – 5389, December, 2018. DOI: 10.1109/TED.2018.2873738. **Tier-1**

[18] Y. Liang, X. Li, S. George, S. Srinivasa, Z. Zhu, **S. K. Gupta,** S. Datta, V. Narayanan, " Influence of Body Effect on Sample-and-Hold Circuit Design Using Negative Capacitance FET", *IEEE Transactions on Electron Devices,* vol. 65, no. 9, pp: 3903- 3914. August 2018. DOI: 10.1109/TED.2018.2852679. **Tier-1**

[19] S. George, X. Li, M. J. Liao, K. Ma, S. Srinivasa, K. Mohan, A. Aziz[G], J. Sampson, **S. K. Gupta**, and V. Narayanan, "Symmetric 2D-Memory Access to Multi-Dimensional Data", *IEEE Transactions on Very Large Scale Integrated Circuits*, vol. 26, no. 6, pp: 1040 – 1050, June 2018. DOI: 10.1109/TVLSI.2018.2801302. **Tier-1**

[20] S. Srinivasa, X. Li, M. F. Chang, J. Sampson, **S. K. Gupta**, and V. Narayanan, "Compact 3D-SRAM Memory with Concurrent Row and Column Data Access Capability Using Sequential Monolithic 3D Integration", *IEEE Transactions on Very Large Scale Integrated Circuits*, vol. 26, no. 4, pp:671-683, April 2018. DOI: 10.1109/TVLSI.2017.2787562. **Tier-1**

[21] A. Saha[G], S. Datta and **S. K. Gupta**, "'Negative Capacitance' Effect in Resistor-Ferroelectric and Ferroelectric-Dielectric Networks: Apparent or Intrinsic?", *Journal of Applied Physics*, vol. 123, no. 105102, March 2018. DOI: 10.1063/1.5016152. **Tier-1 (Cover feature)**.

[22] S. Gupta[G], M. Steiner[UG], A. Aziz[G], V. Narayanan, S. Datta and **S. K. Gupta**, "Device-Circuit Analysis of Ferroelectric FETs for Low-Power Logic", *IEEE Transactions on Electron Devices*, vol. 64, no. 8, pp. 3092-3100, August 2017. DOI: 10.1109/TED.2017.2717929. **Tier-1**

[23] X. Li, J. Sampson, A. Khan, K. Ma, S. George, A. Aziz[G], **S. K. Gupta**, S. Salahuddin, M.F. Chang, S. Datta and V. Narayanan, "Enabling Energy-Efficient Nonvolatile Computing With Negative Capacitance FET", *IEEE Transactions on Electron Devices*, vol. 64, no. 8, pp. 3452-3458, August 2017. DOI: 10.1109/TED.2017.2716338. **Tier-1**

[24] X. Li, K. Ma, S. George, W.-S Khwa, J. Sampson, **S. K. Gupta**, Y. Liu, M.-F. Chang, S. Datta, and V. Narayanan, "Design of Nonvolatile SRAM with Ferroelectric FETs for Energy-Efficient Backup and Restore", *IEEE Transactions on Electron Devices*, vol. 64, no. 7, pp. 3037-3040, July 2017. DOI: 10.1109/TED.2017.2707664. **Tier-1**

[25] X. Li, S. George, K. Ma, W-Yu Tsai, A. Aziz[G], J. Sampson, **S. K. Gupta**, M. F. Chang, Y. Liu, S. Datta, and V. Narayanan, "Advancing Nonvolatile Computing With Nonvolatile NCFET Latches and Flip-Flops", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 11, pp. 2907-2919, November 2017. DOI: 10.1109/TCSI.2017.2702741. **Tier-1**

[26] A. Aziz[G], N. Shukla, S. Datta and **S. K. Gupta**, "Steep Switching Hybrid Phase Transition FETs (Hyper-FET) for Low Power Applications: A Device-Circuit Co-design Perspective: Part I", *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 1350-1357, March 2017. DOI: 10.1109/TED.2016.2642884. **Tier-1**

[27] A. Aziz[G], N. Shukla, S. Datta and **S. K. Gupta**, "Steep Switching Hybrid Phase Transition FETs (Hyper-FET) for Low Power Applications: A Device-Circuit Co-design Perspective: Part II", *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 1358-1365, March 2017. DOI: 10.1109/TED.2017.2650598. **Tier-1**

[28] A. Aziz[G], N. Jao[UG], S. Datta and **S. K. Gupta**, "Analysis of Functional Oxide based Selectors for Cross-Point Memories", *IEEE Transactions on Circuits and Systems – I*, vol. 63, no. 12, pp. 2222-2235, December 2016. DOI: 10.1109/TCSI.2016.2620475. **Tier-1**

[29] S. Srinivasa, A. Aziz[G], N. Shukla, X. Li, J. Sampson, S. Datta, J. P. Kulkarni, V. Narayanan and **S. K. Gupta**, "Correlated Material Enhanced SRAMs with Robust Low Power Operation", *IEEE Transactions on Electron Devices*, vol. 63, no. 12, pp. 4744-4752, December 2016. DOI: 10.1109/TED.2016.2621125. **Tier-1**

[30] A. Aziz[G], S. Ghosh, S. Datta and **S. K. Gupta**, "Physics-Based Circuit-Compatible SPICE Model for Ferroelectric Transistors", *IEEE Electron Device Letters*, vol. 37, no. 6, pp: 805-808, June 2016. DOI: 10.1109/LED.2016.2558149. **Tier-1**

[31] M. S. Kim, W C- Wissing[UG], X. Li, J. Sampson, S. Datta, **S. K. Gupta** and V. Narayanan, "Comparative Area and Parasitics Analysis in FinFET and Hetero-junction Vertical TFET Standard Cells", *ACM Journal of Emerging Technologies in Computing*, vol. 12, no. 4, pp: 38.1-38:23, July 2016. DOI: 10.1145/2914790. **Tier-1**

[32] A. Aziz[G] and **S. K. Gupta**, "Hybrid Multiplexing (HYM) for Read- and Area-Optimized MRAMs with Separate Read-Write Paths," *IEEE Transactions on Nanotechnology*, vol. 15, no. 3, pp. 473-483, May 2016. DOI: 10.1109/TNANO.2016.2544860. **Tier-1**

[33] N. Shukla, A. V. Thathachary, A. Agrawal, H. Paik, A. Aziz[G], D. G. Schlom, **S. K. Gupta**, R. E. Herbert and S. Datta, "A steep slope transistor based on abrupt electronic phase transition", *Nature Communications*, vol. 6, no. 7812, pp: 1-6, August 2015. DOI: 10.1038/ncomms8812. **Tier-1**

As Graduate Student

[34] W. S. Cho, **S. K. Gupta** and K. Roy, "Device-Circuit Analysis of Double-Gate MOSFETs and Schottky-Barrier FETs: A Comparison Study for Sub-10nm Technologies", *IEEE Transactions on Electron Devices*, vol. 61, no. 12, pp: 4025 – 4031, December 2014. DOI: 10.1109/TED.2014.2364791. **Tier-1**

[35] S. H. Choday, **S. K. Gupta** and K. Roy, "Write-Optimized STT-MRAM Bit-cells Using Asymmetrically Doped Transistors", *IEEE Electron Device Letters*, vol. 35, no. 11, pp: 1100 – 1102, November 2014. DOI: 10.1109/LED.2014.2358998. **Tier-1**

[36] **S. K. Gupta** and K. Roy, "Device-Circuit Co-optimization for Robust Design of FinFET-based SRAMs", *IEEE Design & Test of Computers*, vol. 30, no. 6, pp:29-39, December 2013 **(Invited)**. DOI: 10.1109/MDAT.2013.2266394. **Tier-1**

[37] **S. K. Gupta**, J. P Kulkarni and K. Roy, "Tri-Mode Independent Gate FinFET-based SRAM with Pass-Gate Feedback: A Device-Circuit Co-design Approach for Enhanced Cell Stability", *IEEE Transactions on Electron Devices*, vol. 60, no. 11, pp: 3696 - 3704, November 2013. DOI: 10.1109/TED.2013.2283235. **Tier-1**

[38] **S. K. Gupta**, J. P Kulkarni, S. Datta and K. Roy, "Heterojunction Intra-band Tunneling (HIBT) FETs for Low Voltage SRAMs", *IEEE Transactions on Electron Devices*, vol. 59, no.12, pp: 3533 - 3542, December 2012. DOI: 10.1109/TED.2012.2221127. **Tier-1**

[39] **S. K. Gupta**, G. Panagopoulos and K. Roy, "NBTI in n-type SOI access FinFETs in 6T SRAM and its impact on cell stability and performance", *IEEE Transactions on Electron Devices*, vol. 59, no. 10, pp: 2603 - 2609, October. 2012. DOI: 10.1109/TED.2012.2209182. **Tier-1**

[40] M. Sharad, **S. K. Gupta**, S. Raghunathan, P. Irazoqui and K. Roy, "Low-Power Architecture for Epileptic Seizure Detection Based on Reduced Complexity DWT", *ACM Journal on Emerging Technologies in Computing Systems*, vol. 8, no. 2, pp: 1-14, June 2012. DOI: 10.1145/2180878.2180882. **Tier-1**

[41] F. Moradi, **S. K. Gupta**, G. Panagopoulos, H. Mahmoodi, D. T. Wisland and K. Roy, "Asymmetrically-doped (AD) FinFET for Low Power Robust SRAMs", *IEEE Transactions on Electron Devices*, vol. 58, no. 12, pp: 4241 - 4249, December 2011. DOI: 10.1109/TED.2011.2169678. **Tier-1**

[42] **S. K. Gupta**, S. P. Park and K. Roy, "Tri-mode Independent Gate FinFETs for Dynamic Voltage/Frequency Scalable 6T SRAMs", *IEEE Transactions on Electron Devices*, vol. 58, no. 11, pp: 3837 – 3846, November 2011. DOI: 10.1109/TED.2011.2166117. **Tier-1**

[43] S. Raghunathan, **S. K. Gupta**, H. Markandeya, P.P. Irazoqui and K. Roy, "Ultra-Low-Power Algorithm design for Implantable Devices- Application to Epilepsy Prostheses", *Journal of Low Power Electronics and Applications*, vol. 1, no. 1, pp: 175-203, May 2011 **(Invited)**. DOI: 10.3390/jlpea1010175. **Tier-1**

[44] N. N. Mojumder, **S. K. Gupta**, S. H. Choday, D. E. Nikonov and K. Roy, "Three-Terminal Dual-Pillar STT-MRAM Device for High-Performance Robust Memory Applications," *IEEE Transactions on Electron Devices*, vol. 58, no. 5, pp: 1508 – 1516, May 2011. DOI: 10.1109/TED.2011.2116024. **Tier-1**

[45] A. Goel, **S. K. Gupta** and K. Roy, "Asymmetric Drain Spacer Extension (ADSE) FinFETs for Low Power and Robust SRAMs", *IEEE Transactions on Electron Devices*, vol. 58, no. 2, pp: 296 - 308, February 2011. DOI: 10.1109/TED.2010.2090421. **Tier-1**

[46] S. Raghunathan, **S. K. Gupta**, H. Markandeya, K. Roy and P. P. Irazoqui, "A hardware-algorithm co-design approach to optimize seizure detection algorithms for implantable applications", *Journal of Neuroscience Methods*, vol. 193, no. 1, pp: 106-117, October 2010. DOI: 10.1016/j.jneumeth.2010.08.008. **Tier-1**

[47] **S. K. Gupta**, A. Raychowdhury and K. Roy, "Digital computation in sub-threshold regime for ultra-low power operation: A device-circuit-architecture codesign perspective", *Proceedings of the IEEE*, vol. 98, no. 2, pp: 160 – 190, February 2010 **(Invited)**. DOI: 10.1109/JPROC.2009.2035060. **Tier-1**

[48] S. Raghunathan, **S. K. Gupta**, M. P. Ward, R. M Worth, K. Roy and P. Irazoqui, "The design and hardware implementation of a low-power real-time seizure detection algorithm", *Journal of Neural Engineering*, vol. 6, no. 056005, pp: 1-13, October 2009. DOI: 10.1088/1741-2560/6/5/056005. **Tier-1**

[49] **S. K. Gupta**, A. Raychowdhury and K. Roy, "Compact models considering incomplete voltage swing in CMOS circuits at ultra-low voltages: A circuit perspective on limits of switching energy", *Journal of Applied Physics*, vol. 105, no. 094901, pp: 1-10, May 2009. DOI: 10.1063/1.3123763. **Tier-1**

As Undergraduate Student

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As Faculty Member

[1] A. K. Saha[G], and **S. K. Gupta**, "Effective Ferroelectric Permittivity in Metal-Ferroelectric-Insulator-Semiconductor (MFIS) Heterostructures: The Implications of Hard and Soft Domain Walls", *Material Research Society (MRS) Meeting*, 2021 (Abstract) (**Invited).**

[2] A. K. Saha[G], M. Si, K. Ni, S. Datta, P. D. Ye, and **S. K. Gupta**, "Ferroelectric Thickness Dependent Domain Interactions in FEFETs for Memory and Logic: A Phase-field Model based Analysis", *International Electron Device Meetings (IEDM)*, 2020 (4 pages).

[3] S. K. Thirumala[G], A. Raha, V. Raghunathan and **S. K. Gupta**, "IPS-CiM: Enhancing Energy Efficiency of Intermittently Powered Systems with Compute-in-Memory", *International Conference on Computer Design (ICCD)*, 2020 (8 pages).

[4] K. Cho[G], S. K. Thirumala[G], X. Liu, N. Thakuria[G], Z. Chen and **S. K. Gupta**, "Utilizing Valley-Spin Hall Effect in WSe_2 for Low Power Non-Volatile Flip-Flop Design," *Device Research Conference (DRC)*, 2020 (2 pages).

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[7] K. Ni, A. K. Saha[G], W. Chakraborty, H. Ye, B. Grisafe, J. Smith, G. B. Rayner, **S. K. Gupta** and S. Datta, " Equivalent Oxide Thickness (EOT) Scaling With Hafnium Zirconium Oxide High-κ Dielectric Near Morphotropic Phase Boundary", *International Electron Device Meetings (IEDM)*, 2019 (4 pages).

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[33] **S. K. Gupta**, D. Wang[G], S. George, A. Aziz[G], X. Li, S. Datta and V. Narayanan, "Harnessing Ferroelectrics for Non-volatile Memories and Logic", *IEEE International Symposium on Quality Electronic Design (ISQED)*, Santa Clara CA, USA, March 14-15, 2017. (6 pages). **(Invited).** DOI: 10.1109/ISQED.2017.7918288**.**

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As Undergraduate Student

[65] M. J. Kumar, V. Venkataraman and **S. K. Gupta**, "A New Grounded Lamination Gate (GLG) SOI MOSFET for Diminished Fringe Capacitance Effects," *NSTI Nanotechnology Conference and Trade Show*, Boston MA, USA, May 7-11, 2006 (4 pages).

Invited Lectures

[1] "Energy Efficient and Non-Volatile Circuit Design based on Ferroelectric Transistors", Beyond-CMOS Circuits and Systems Workshop, University of Notre Dame, 2016.

[2] "Low Power Robust Design of FinFET-based Circuits using a Technology-Circuit Co-Optimization Approach", *Keynote Talk* in 9th International Front-End Electronics (FEE) Conference, 2014.

Pending Publications

[1] A. K. Saha[G], M. Si, P. D. Ye, and **S. K. Gupta**, "Multi-domain Polarization Switching in HZO-Dielectric Stack: The Role of Dielectric Thickness" Under Review in *IEEE Electron Device Letters.*

[2] S. K. Thirumala[G], S. Choudhary, and **S. K. Gupta**, "Symmetric Reconfigurable Ferroelectric Transistor for Non-Volatile Memories to Diminish the Effects of Gate Leakage" Under Review in *IEEE Transactions on Electron Devices.*

Patents Approved and Patent Applications

[1] S. K. Thirumala, **S. K. Gupta**, T. Hung and Z. Chen, "Valley Spin Hall Effect based Non-Volatile Memory" Application number 16909971, Filed June 23, 2020.

[2] **S. K. Gupta**, A. Aziz, N, Shukla, S. Datta, X. Li and V. Narayanan, "Low Power Sense Amplifier based on Phase Transition Material" Patent issued. (Patent No: US20190172514).

[3] V. Narayanan, X. Li, S. George, J. Sampson, **S. K. Gupta**, and S. Datta, "Nonvolatile Digital Computing with Ferroelectric FET" Patent issued. (Patent No: US20180330791).

Courses Developed

At Penn State

EE 597A Advanced Digital VLSI Design (Spring 2015, 2017)

Courses "In Charge Of"

At Purdue

ECE 695	Advanced VLSI Design (Spring 2020, Spring 2021)
ECE 202	Linear Circuit Analysis II (Spring, Fall 2019)
ECE 559	MOS VLSI Design (Fall 2018)
ECE 255	Electronic Circuit Analysis and Design (Spring 2018)

At Penn State

EE 310	Electronic Circuit Design I (Spring 2016, 2017)
EE 597A	Advanced Digital VLSI Design (Spring 2015, 2017)
EE 416	Digital Integrated Circuits (Fall 2014, 2015, 2016, 2017)

Others

EE 200	Design Tools (As co-instructor with Prof. Schiano, Penn State) (Spring 2014))
ECE 202	Linear Circuit Analysis II (as Graduate Instructor) (Summer 2008)
ECE 255	Electronic Circuit Analysis and Design (as Teaching Assistant) (Fall 2006, Spring 2007, Fall 2017)

School Committee Activities

At Purdue

Committee: Graduate Committee
Activity: Member, Aug. 2018- present

Committee: Admissions Committee, VC area
Activity: Member, 2019

At Penn State

Committee: Graduate Committee
Activity: Member, Aug. 2017- Dec. 2017

Committee: Undergraduate Committee
Activity: Member, Aug. 2014 – July 2017

Committee: Faculty Search Committee
Activity: Member, 2015-2017

Engineering-Wide Committee Activities

At Penn State

Committee: College of Engineering Research Computing Committee
Activity: Member, Sept. 2016 – Dec. 2017.

Editorial Activities

2020- Present	Editorial Board Member, Micromachines

Activities as a Referee

2018	National Science Foundation
2006-present	IEEE Transactions on Electron Devices (TED)
2014-present	Electron Device Letters (EDL)
2015-present	IEEE Transactions on Circuits and Systems (TCAS)
2015-present	IEEE Transactions on Computer Aided Design (TCAD)
2016-present	IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
2018-present	Applied Physics Letters (APL)
2017-present	IEEE Journal of Exploratory Solid-State Computational Devices and Circuits (JxCDC)
2015-2016	IEEE Transactions on Nanotechnology (TNANO)

Technical Program Committee in Conferences

[1] Member of Technical Program Committee, DRC (2020, 2021)

[2] Co-chair of Sub-committee on Design Technology Co-optimization, ISQED (2019, 2020)

[3] Chair of Sub-committee on Emerging Device Technologies, DAC (2018)

[4] Chair of VLSI Circuits and Low Power Track, GLSVLSI (2017, 2018)

[5] Member of Technical Program Committee, SISPAD (2018, 2019, 2021)

[6] Member of Technical Program Committee, ISCAS (2018, 2021)

[7] Member of Technical Program Committee, ISQED (2018-2021)

[8] Member of Technical Program Committee, DAC (2017, 2020, 2021)

[9] Member of Technical Program Committee, VLSIDAT (2017)

[10] Member of Technical Committee for DAC Ph.D. Forum (2016)

[11] Member of Technical Program Committee, GLSVLSI (2016)

[12] Member of Technical Program Committee, ISLPED (2015-2021)

[13] Member of Technical Committee, IEEE S3S Conference (2014-2016)

[14] Member of Technical Program Committee, Conference on VLSI Design and Embedded Systems, India (2014)

Special Sessions/Tutorials/Panel Discussions in Conferences

[1] Organizer of the short course on "Quantum Computing" (with Asif Khan, Georgia Tech), DRC (2021)

[2] Organizer of the Rump Session on "The Race to Non-Volatility: Which technologies will cross the finish line?" (with Mona Ebrish and Huili Grace Xing), DRC (2020).

[3] Co-organizer of a tutorial (with Prof. Vijay Narayanan and Prof. Arijit Raychowdhury) on "Emerging Computational Devices, Architectures and Computational Models", Conference on VLSI Design and Embedded Systems (2018).

[4] Organizer of special session on "Design Opportunities and Challenges in Non-Volatile Technologies" in ISQED (2017)

[5] Special session chair at Design Automation Conference (2015)

[6] Organizer of special session on Non-volatile Memories in ISVLSI (2015)

Other Activities:

[1] Organizer of the Seminar Series for ECE Faculty, Purdue University (Spring 2021)

[2] Hosted two students from under-represented groups under Summer Research Opportunity Program at Penn State (2016)

[3] Participated in school outreach program, Exploration-U at Penn State (2016)