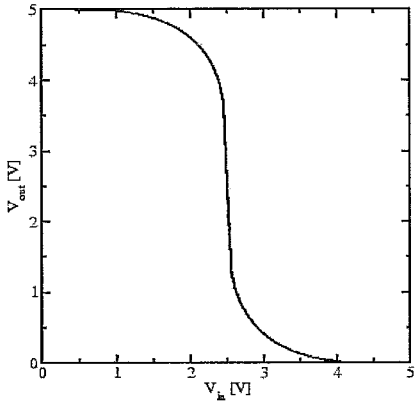
VC-1
August 2015 QE

Q1. (25 points): Consider the voltage transfer curve of a CMOS inverter given in the figure below. On this curve, label the following points: V_{OH}, V_{OL}, V_{IH}, V_{IL}, and V_M and explain how you came up with each of the points. You should also indicate any other lines and points on the curve required to define the above points. Clearly state any assumptions you make.



Q2. (30 points): Energy Delay Product (EDP) is a commonly used design metric in digital circuits that combines a measure of performance and energy consumption. Consider a static CMOS inverter, whose propagation delay can be approximated by the expression:

$$t_p \approx \frac{\propto \times C_L \times V_{DD}}{V_{DD} - V_{TE}}$$

where $V_{TE} = \left(V_T + \frac{V_{DSAT}}{2}\right)$ and $\propto$ is a technology dependent parameter. Suppose you are given that $V_{TE} = 0.8V$. For simplicity, you can make the assumption that leakage and short-circuit components of power consumption are negligible. For such a CMOS inverter switching at its maximum rate, the EDP can be calculated as:

$$EDP = \frac{C_L \times V_{DD}^2 \times t_p}{2}$$

Given the above information, you are interested in analyzing the impact of V_{DD} on the EDP.

(a) For the given parameters, calculate the value of V_{DD} that minimizes the EDP of the CMOS inverter. Clearly state any assumptions you make.

(b) Now consider a real transistor where leakage is non-zero with a transistor threshold voltage of V_t. Illustrate, using a qualitative figure, the expected relationship between EDP and V_{DD} and explain why the relationship is that way. Clearly state any assumptions you make.

Q3. (45 points): Implement the logic function F = ABD + CD using (a) a 4-input static CMOS logic gate and a single inverter, (b) a 4-input pseudo NMOS logic gate and a single inverter, and (c) a 4-input Domino CMOS logic gate and a single inverter. Clearly state any assumptions you make.