VC-1
August 2014 QE

Q1. [40 points] Consider building an inverter in 90nm technology with an NMOS transistor and a PMOS transistor. Assume that the PMOS transistor is sized to have similar characteristics as the NMOS transistor at a supply voltage of 1V. Also assume that the threshold voltages are 350mV for the NMOS transistor and -350mV for the PMOS transistor and all the experiments are performed at room temperature (300 K)

(a) Qualitatively draw the voltage transfer characteristic of the inverter, clearly marking and labeling the trip-point of the inverter. **[15 points]**

(b) On the same plot, show how the transfer characteristics and the trip point change: **[10 points]**

(i) If the PMOS transistor is made stronger than the NMOS transistor

(ii) If the NMOS transistor is made stronger than the PMOS transistor

(c) Qualitatively draw the voltage transfer characteristic when the supply voltage is scaled to 350mV, 200mV, and 25mV, respectively (assume that the PMOS and NMOS strengths are similar as in part (a)). **[15 points]**

Clearly explain your results and state any assumptions.

Q2. [60 points] I am interested in implementing the following logic of two cascaded 2-input AND gates in different circuit styles – (i) standard CMOS, (ii) Pseudo-NMOS, and (iii) Domino CMOS.

(a) Draw transistor-level schematics of the different circuit styles so that I can implement them. Clearly explain the circuit operation, especially for the Domino circuit style. **[30 points]**

(b) Qualitatively compare the different circuit styles you have drawn with respect to power consumption, delay, and noise immunity. I am interested in an implementation that is noise immune and fast. Please clearly explain your answer so that I can choose the proper circuit style for my implementation, given my design goals above. **[30 points]**

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