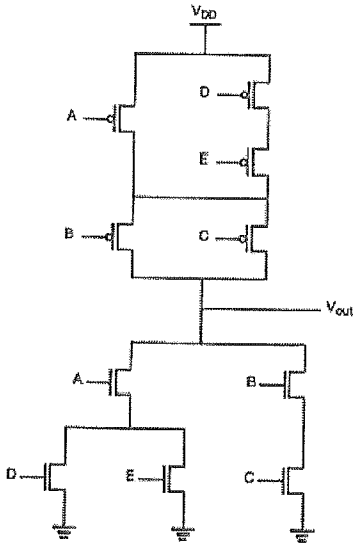
August 2011 QE

Question 1 (50 points): Consider the static CMOS logic gate shown in the figure. Determine, for each of the four cases listed below, a pair of input patterns for A, B, C, D, and E such that

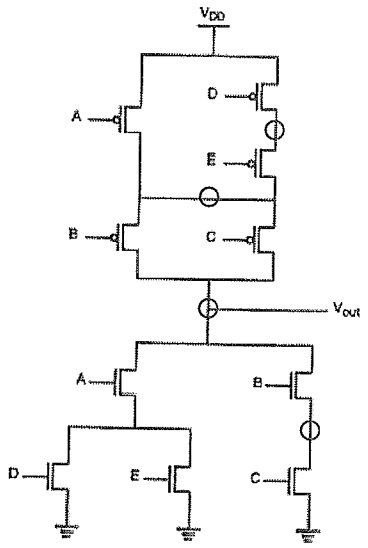
(a) The low-to-high transition is the slowest;
(b) The low-to-high transition is the fastest;
(c) The high-to-low transition is the slowest;
(d) The high-to-low transition is the fastest.

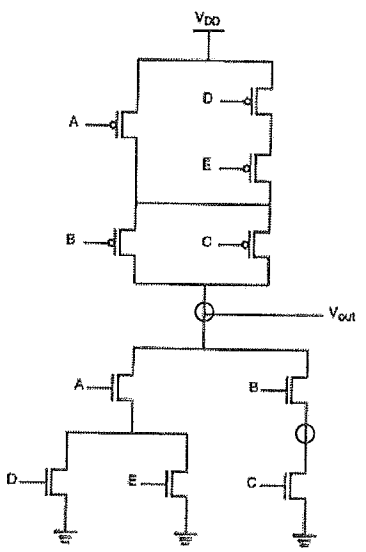


Consider for example a pair of input patterns (A = 0V, B = V_{DD}, C = 0V, D = 0V, E = 0V) and (A = 0V, B = V_{DD}, C = V_{DD}, D = 0V, E = 0V). Assume that we allow the capacitors in the logic gate to settle to their final values based on the first input pattern, the second input pattern will cause the output to switch from high to low. You can then use Elmore delay to determine the high-to-low transition delay based on the resistive network that is used to discharge the capacitors.

Use the Elmore delay model to find four pairs of input patterns that would result in the slowest and fastest transitions. Justify your answer.

Hint: For simplicity, assume that each diffusion region has a junction capacitance C_{eq}, every transistor has a resistance R_{eq}, and the load capacitance at the output is C_L. Assume that there is no sharing of diffusion regions. For example, the total capacitance at the output node is $4C_{eq} + C_L$. Assume that a capacitor will be charged fully to V_{DD} even if it resides in the pull-down network and that a capacitor will be discharged completely to 0V even if it resides in the pull-up network. The left figure below shows the capacitors (at the circled nodes) that will be charged for the first input pattern given above, and the right figure below shows the capacitors (at the circled nodes) that will be discharged for the second input pattern given above. The Elmore delay for the high-to-low transition is $R_{eq}(6C_{eq}+C_L) + R_{eq}(4C_{eq}+C_L) = R_{eq}(10C_{eq}+2C_L)$.





Write in Exam Book Only

2. Draw the schematic of a one transistor one capacitor dynamic random access memory. Describe the read and write operations. (20)

Assume a bit line capacitance of 1pF and a bit-line pre-charge voltage of 1.25V. The voltage over the cell capacitance (50fF) equals 1.9V and 0V, for a logic ONE and ZERO, respectively. Determine the voltage swing on the bit-lines during read operation (for reading both ONE and ZERO). (30)