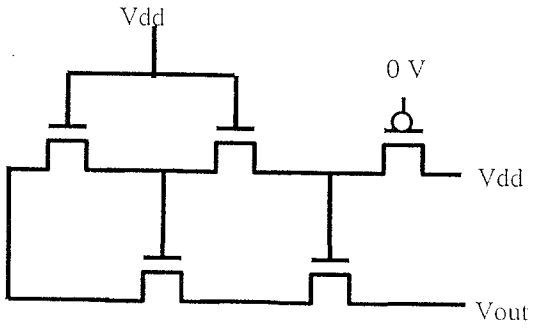
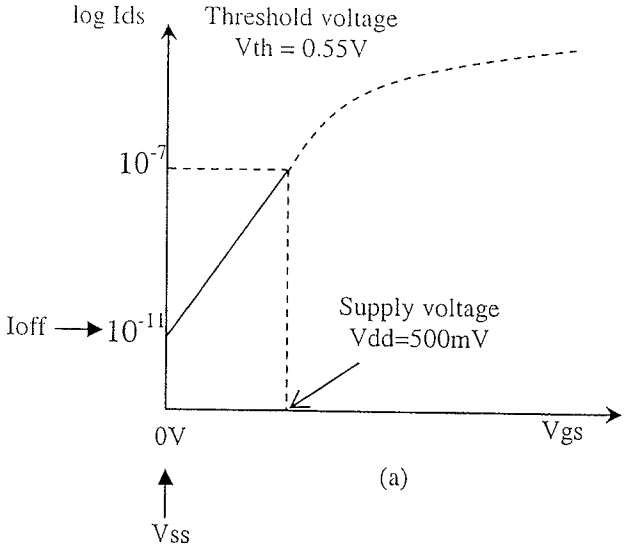
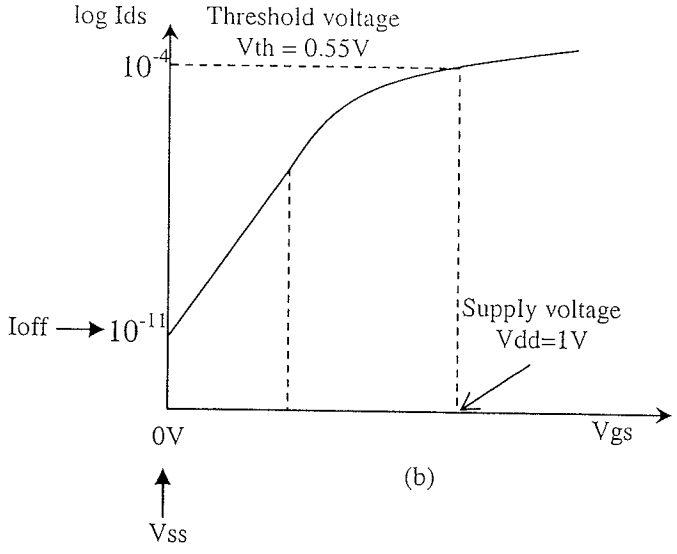
1. For the circuit diagram below, determine Vout? All NMOS bodies are connected to Ground and PMOS body to Vdd. Assume Vdd=5V and threshold voltage for NMOS is Vtp=1V, and for PMOS it is Vtp = -1V. Neglect body effect. [20 points]
What is the impact of body effect on Vout? Clearly explain your answer. [10 points]



2. Consider the following NMOS transistor current-voltage characteristic (Fig. (a): Vdd and Vss have their usual significance in circuit design). Assume a complementary characteristic for PMOS transistor. Can you design a CMOS inverter that effectively utilizes the I-V characteristic? Clearly state your reasons. [15 points]
Can you qualitatively compare the voltage transfer characteristic (VTC) of this inverter with a standard CMOS inverter designed with standard transistors (I-V characteristics shown below: Fig. (b)). Compare the sharpness of the VTC curves and sensitivity to device parameters (process variations) [15 points]





3. Consider an inverter of minimum size (input capacitance of Ci) driving a load Cl where Cl = x.Ci The size of the PMOS transistor is *a* times larger than the NMOS transistor. You decide to introduce two inverters (u and u^2 times larger than the first) between the minimum sized inverter and the load Cl. What should u be to minimize the delay. If x=64, does it make sense to introduce the extra inverters? [40 points]

   Assume Proportionality Factor $\gamma = C_{int}/C_g = 1$
   where C_{int} is the intrinsic output capacitance of the inverter, and C_g is the input gate capacitance of the inverter. For minimum size inverter, $C_g = Ci$.

   Hint: Calculate the delay as a function of t_{po} and fan-out. t_{po} is the intrinsic delay of the inverter; the delay of the inverter only loaded by its own intrinsic capacitance.