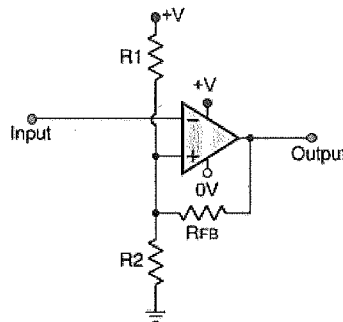


VC-1
August 2017 QE

Question 1 (30 points): Draw the transistor-level schematic for the implementation of a full adder circuit using (i) static CMOS, (ii) NORA dynamic CMOS, and (iii) complementary pass transistor logic (CPL). (10 points for each logic style)

Question 2 (30 points): Consider an inverter of minimum size (with an input capacitance of C_{in}) driving a load C_L , which is 'F' times as large as C_{in} . The PMOS transistor is 'A' times larger than the NMOS transistor. You introduce another inverter ('X' times larger than the first inverter) between the minimum-sized inverter and the load C_L . Determine the value of X to minimize the delay of the chain. When does it make sense to introduce this inverter? Clearly state all your assumptions.

Question 3 (40 points): Consider the following inverting Schmitt Trigger circuit, with the supply voltage (+V) being equal to 5V, $R1 = 15K\Omega$, $R2 = 30K\Omega$, and $R_{FB} = 25 K\Omega$.



(a) (20 points) Compute the high and low trip thresholds of this Schmitt Trigger circuit.

(b) (20 points) Draw the voltage waveform at the output if the following waveform is input to the above Schmitt Trigger circuit.

