1. (a) Consider a CMOS inverter, driving a capacitive load of 6fF. The size of the pull-up transistor of the inverter is 4 times larger than the pull-down transistor. Determine the energy needed to charge and discharge the capacitance if the supply voltage is 2.5V.

(b) Assume that the inverter is switched at the maximum possible rate of 32.5ps. Determine the dynamic power consumption of the circuit.

2. Consider the inverter discussed in Problem 1. Assume that the output capacitance is charged to $V_{DD}$. Now, if you have an ideal rising input transition (from 0 to $V_{DD}$), determine the output fall time ($0.9V_{DD}$ to $0.1V_{DD}$). Clearly state your assumptions.

3. Draw the schematic of a three input NAND gate with an output capacitive load of $C$. Label the inputs as $X$, $Y$, and $Z$. If the three inputs to the NAND gate have different arrival times, determine the ordering of inputs in the schematic for fastest operation. Clearly state the reasons for your ordering.