We want to consider a conventional n-type silicon MOSFET with a channel length of \( L = 1 \mu m \), a channel width of \( W = 0.5 \mu m \) and a gate dielectric of \( t_{ox} = 10 \)nm SiO\(_2\) (\( \varepsilon_r \approx 3.9 \)). The doping level of the channel is \( N_A = 2 \times 10^{18} cm^{-3} \). The device exhibits a threshold voltage of \( V_T = 0.5 V \) (Note that a non-zero flat-band voltage has been assumed). The two n-type regions next to source and drain are heavily doped at a level of \( 5 \times 10^{19} cm^{-3} \). At a gate voltage of 1V transport measurements reveal a channel mobility of 300 cm\(^2\) V\(^{-1}\)s\(^{-1}\).

![Diagram of a MOSFET](image)

In order to contact the device, silicided source and drain regions are created. The contact resistance between those silicided regions in source and drain and the n-doped portion of the n-MOSFET turned out to be \( R_{source} = R_{drain} = 2000 \Omega \) due to an accident during the manufacturing process. This contact resistance value is independent of the applied gate and drain voltage.

1) Considering both transition regions, the one next to the source as well as the drain electrode, calculate the current through the device in the linear \( I_d-V_{ds} \) region for \( V_{ds} = 10 mV \) and \( V_{gs} = 1 V \) and indicate how much less current flows through the FET if compared to the ideal condition of \( R_{source} = R_{drain} = 0 \Omega \). Assume that the system can be modeled by a series of resistors. Ignore the contributions of the n-doped silicon regions to the resistor network. Use \( \varepsilon_0 \varepsilon_r = 3.4 \times 10^{-11} \) As/Vm for your calculation. (30 pts.)

While the designers worked hard to create a long-channel MOSFET, one where the gate rather than the drain controls the electrostatics inside the channel region, the processing error that resulted in the above high contact resistance also impacted the all-over appearance of the device characteristics. The chief-engineer noticed clear signs of short-channel effects (SCEs) in the output as well as subthreshold characteristics of the MOSFET.

2) Indicate what signs of short-channel effects the chief-engineer saw when evaluating the \( I_d-V_{ds} \) characteristics in the current saturation region of the output characteristics by sketching \( I_d-V_{ds} \) for three different gate voltages. (Note that the dependence of \( I_d \) on \( V_{gs} \) is not critical in the context of this task.) Explain your findings qualitatively. (10 pts.)

Besides the on-state performance, the off-state performance of the devices was impacted as well. A high interface trap capacitance \( C_{it} = 6 \times 10^{-16} F \) was identified as the reason for this behavior. One of the measures to characterize the deteriorated FET performance in the off-state is the inverse subthreshold slope \( S = \ln 10 \cdot \frac{dV_{gs}}{d(\ln I_d)} \). The current in this gate voltage regime is given by \( I_d = A \exp \left( \frac{qV_{gs}}{KT} \right) \), with \( A \) being a constant and \( V_{gs} \) being the potential at the gate-oxide/silicon interface (see the capacitor network below for the details of the potential distribution).
3) Derive the expression for $S$ using the equations for $S$ and $I_d$ from above. To find the relation between $V_{gs}$ and $V_{gs'}$ utilize the capacitance network shown in the figure. ($C_{dep}$ is the depletion capacitance.) (30 pts.)

4) Noting that the ideal $S$-value of a conventional MOSFET is $S_{ideal} = \ln 10 \times kT/q$, calculate $S/S_{ideal}$ in the presence of the aforementioned interface traps assuming for simplicity $C_{dep} = 0$. (10 pts.)

In order to fix at least the on-state problem the chief-engineer looked into a variety of different device parameters that are known to impact the long-channel versus short-channel behavior of an FET. He carefully evaluated the impact of the following parameters: gate oxide thickness, mobility, channel width, carrier concentration, junction depth, effective mass, source/drain depletion width at the contact junctions, and gate voltage range.

5) Indicate which of the above parameters need indeed to be considered to ensure that long-channel type device characteristics are obtained for a given channel length $L$. (10 pts.)

6) Explain for those parameters in your answer to 5) whether they should be made larger or smaller to improve the device — to make it behave more like a long-channel transistor. (10 pts.)