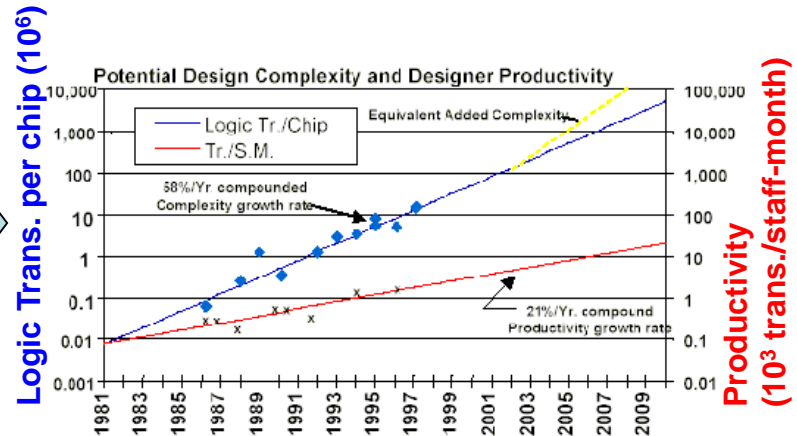


# ECE 595Z

## Digital Systems Design Automation

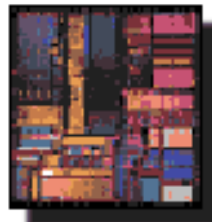
Anand Raghunathan, raghunathan@purdue.edu

- **How do you design chips with over 1 Billion transistors?**
  - **Human designer capability grows far slower than Moore's law!**
  - **Virtually all complex chips are designed using electronic design automation (EDA) tools**

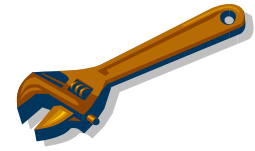


### Course description:

This course will provide an introduction to the tools used to design and analyze circuits at the logic level of abstraction (where circuits are composed of gates and flip-flops). Digital chips used in microprocessors, graphics processors, chips used in network routers, cell phones, digital audio/video appliances, automotive electronics are largely designed using EDA tools. ECE595Z will focus on the foundations of logic-level EDA tools, including the steps involved and algorithms used. Students taking the course can expect a better understanding of how tools work. This course will (i) help designers become “power users” who can get the most out of the tools, and (ii) provide necessary background for students seeking to do research (or employment) in companies that make or use EDA tools.



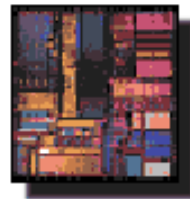
Spring 2018, EE 117, T-Th 10:30-11:45AM



# **ECE 595Z**

## **Digital Systems Design Automation**

**(Catalog number: 19731 - ECE 59500 - 002)**

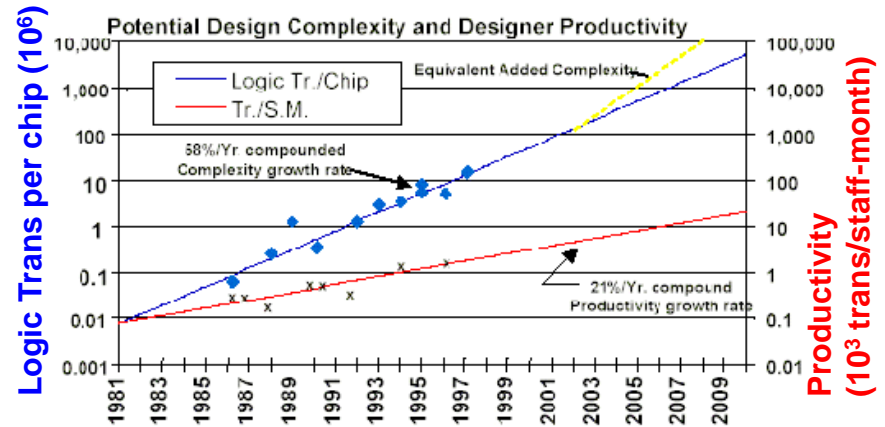


Anand Raghunathan  
raghunathan@purdue.edu

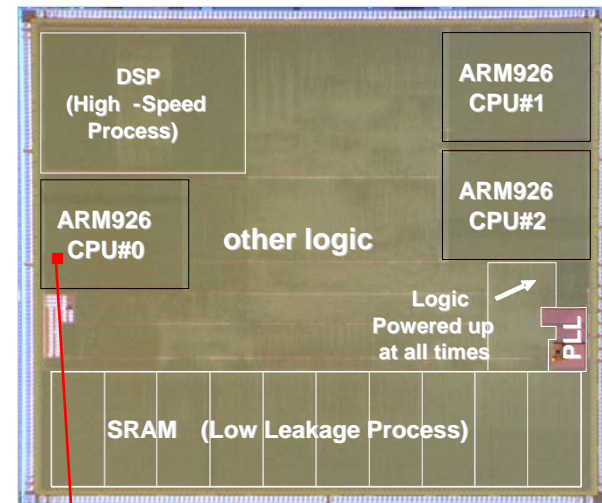
**Spring 2018, EE 117, T-Th 10:30-11:45PM**

# What is this course about?

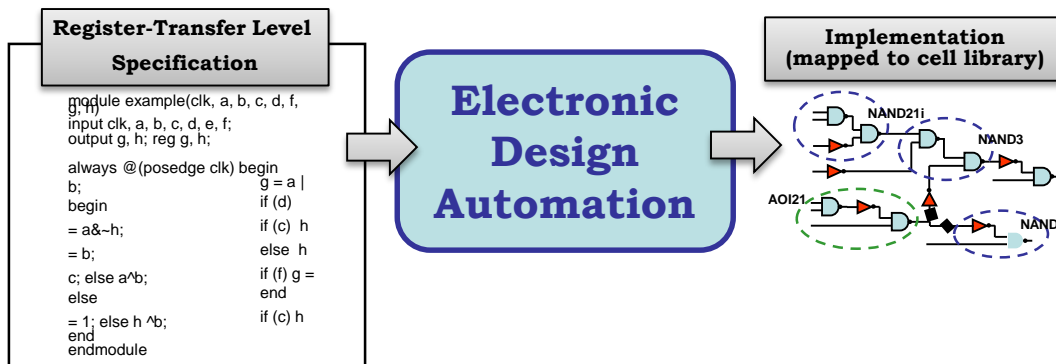
- How to automatically design and analyze digital VLSI circuits at the logic level (gates & Flip-Flops)
- Virtually all semiconductor chips are designed (synthesized, analyzed, and verified) using design automation tools
  - Microprocessors, graphics processors, and chips used in network routers, cell phones, digital audio/video appliances, automotive electronics, ...
  - Design complexity mandates the use of automation



NEC's MP211 processor for mobile phones



ALU (typical VLSI design class project!)



## Register-Transfer Level Specification

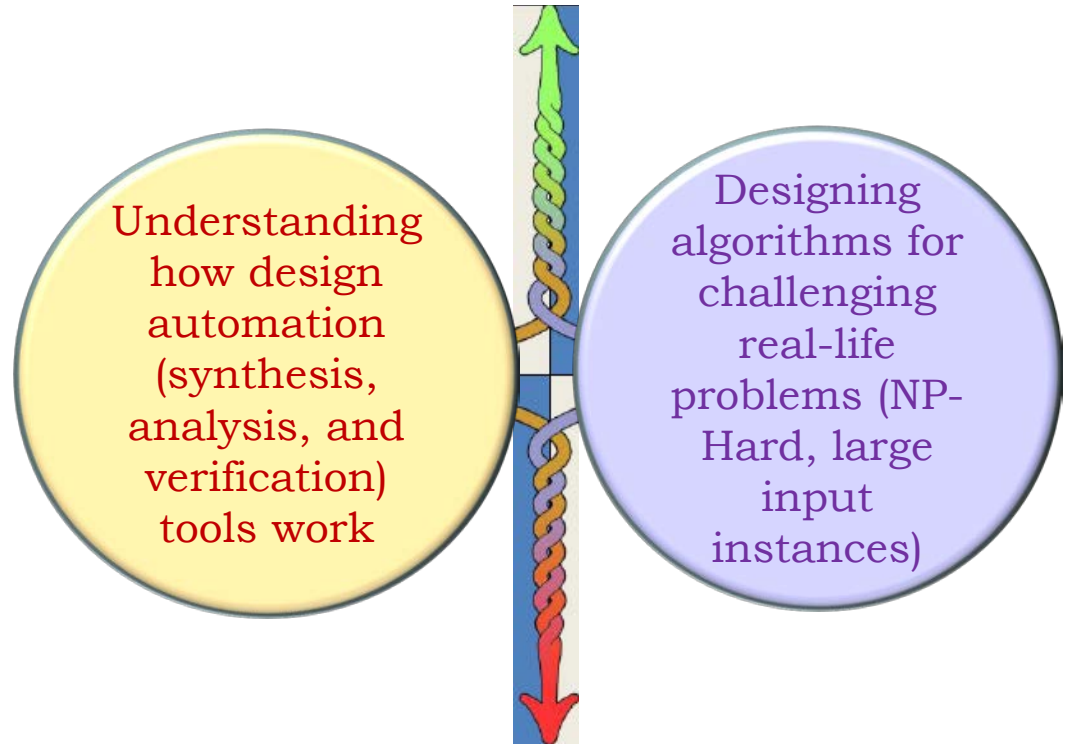
```

module example(clk, a, b, c, d, f,
g, h)
input clk, a, b, c, d, e, f;
output g, h; reg g, h;

always @(posedge clk) begin
b;
begin
= a&~h;          if (c) h
= b;              else h
c; else a^b;      if (f) g =
else              end
= 1; else h ^b;  if (c) h
end
endmodule
    
```

# Course Objectives and Required Background

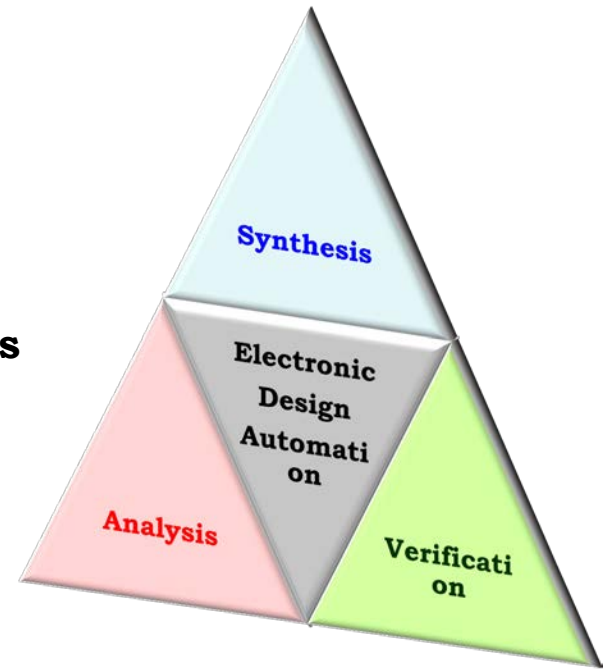
- **Hardware perspective:**  
Better understanding of how tools work
  - Steps involved and algorithms used
  - Designers should know this to become “power users”
  - Useful background for research or employment in VLSI design and EDA
- **Software perspective:**  
How to develop optimization algorithms for challenging real-life problems
  - Most EDA tools need to solve NP-Hard computational problems on large instances
  - EDA is often a driver of algorithmic advances that are used in other domains (covering, SAT, ..)



Required background: Digital logic design, Programming (C/C++), Elementary knowledge of data structures and algorithms

# Course Outline

- **Overview of the IC design flow**
- **Advanced Boolean Algebra**
  - Re-cap of basics and advanced concepts
- **Two-level minimization of combinational circuits**
  - Review of Quine-McCluskey method
  - Exact and heuristic algorithms (Espresso)
- **Multi-level logic synthesis**
  - Technology-independent optimizations
  - Technology mapping
- **Sequential logic optimization**
  - Finite State Machine (FSM) minimization, retiming, regular expressions and FSMs
- **Basics of logic verification**
  - Boolean Satisfiability (SAT)
  - Compact Boolean function representations - Binary Decision Diagrams (BDDs)
  - Combinational equivalence checking, sequential verification
- **Timing Analysis**
  - Longest true path, path sensitization criteria, algorithms for computing true delay, statistical timing analysis
- **Power Analysis and Optimization**
  - Gate-level power estimation, technology mapping for low power, automatic clock gating and power management
- **Design Automation for new (nanoscale) devices and circuit technologies**
  - Threshold logic, multi-valued logic, reversible, etc.



# Grading

- Grading policy
  - Homeworks: 30%
  - Midterm: 20%
  - Class participation: 10%
  - Project: 40%