

Job description: ASIC RTL Engineer

Company

Wearable Brain is a VC-backed, fast-growing, stealth-mode startup developing an electronic brain to augment our biological brain. We are investing in some major technological breakthroughs to make this happen: ultra-low power communication (50x lower than BLE), ultra-low power sensing, and computation (100 micro-watt keyword detection, object detection, imager, and speech transcription among others). We are assembling a team of the leading experts in the field of IC/system design/computer vision/ hardware engineers with an appetite for taking on the next big thing.

Team and Role Overview

We are seeking an RTL Design Engineer to join our RF/Mixed-Signal team. As an RTL Design Engineer, you will be responsible for digital signal processing hardware designs, specifically data path as well as control intensive digital designs. You will work with the System architect, as well as other ASIC designers to micro-architect and implement low-power communication system designs integrated into Wearable Brain.

Candidate Profile

You have experience with RTL design, preferably in the industry.

Skills We're Stoked About

- Bachelor's degree in Science, Engineering, or related field.
- 2+ years ASIC design, verification, or related work experience.
- Strong skills in RTL logic design (VHDL or Verilog) and verification
- Should have extensively used the ASIC RTL Synthesis, LEC, Power Extraction tools (PTPX), Primetime, RTL Linting tools and extensive usage of simulation tools.
- Experience with ASIC ECO flow, RTL sanity tools specific to Design Rule Checking and Clock Domain Crossing checks
- Familiarity with MBIST and DFT flow
- Gate level Simulation debug and usage of power extraction tools a plus

Preferred skills

- 5+ years of RTL design experience on-chip with custom digital logic
- Experience with digital signal processing is a bonus
- Tcl/Perl/Python shell-scripting expertise

The position can be remote but requires regular visits to our West Lafayette, IN (Purdue Research Park) office.