Job Title: Engineer-RET Design

We, the Resolution Enhancement Techniques (RET) team, are looking to fill a RET Engineer position! We are part of the Advanced Mask Development (AMD) group under the Technology Development (TD) department. We have deep understanding of RET methodologies and Optical Proximity Correction (OPC) software tools, and work side-by-side with the Recipe and Tool Development (RTD) team which is also part of AMD group. You will also work collaboratively with Process Integration and Photolithography teams as well as OPC vendors to deliver reticle solutions with production-worthy patterning fidelity on wafer. You will be involved in groundbreaking RET solutions, resolve important patterning issues, investigate creative tapeout flows, and introduce innovative software functions and applications to AMD group. In addition, you will need to dedicatedly engage with teams in Design, Device, and Systems to integrate an effective and efficient tapeout flow for not only pilot parts but also derivative parts throughout the life span of each node of advanced memory products.

Responsibility

- Build OPC model to validate and to predict wafer patterning for both R&D pilot chip and production parts.
- Build recipes of OPC and Sub-resolution Assist Feature (SRAF), extend application to full chip scale.
- Improve RET strategies, including, but not limited to: modeling, OPC, illumination, SRAF, reticle blanks, design rules, and layout.
- Collaboratively work with multidisciplinary groups to generate robust and manufacturable layout for process development and yield improvement.
- Contribute documents of Best Known Methods based from wafer learning, and to detail the thought process and the supporting data.

Qualifications

Successful candidates for this position will have:

- 3+ years experience in reticle development in the semiconductor industry, preferably with direct input on data correction from design and layout to improve printability of the process.
- Experience with photolithography simulation packages, such as Sentaurus Litho, ProLith, etc.
- Experience with software packages developed by any EDA vendor (Synopsys, Mentor Graphics, BRION, Cadence, etc.), preferably in the areas of rule or model based assist feature design, OPC empirical model creation and lithography simulations.
- Strong knowledge in photolithography theory, including optics, diffraction, phase shifting and resist modeling. Must have experience with 248 nm, 193 nm and 193 nm immersion lithography.
- Strong computer skills, including familiarity with Windows, Linux, UNIX, and some experience with programming languages (Perl/C/C++/TCL/Python).
- Knowledge of automation tools, layout and DRC tools like Cadence DF2 and Hercules. (Preferred)
- Knowledge of semiconductor processing, the structure and function of memory devices, emerging technology, and lithography.
• Strong communication, interpersonal, and presentation skills to coordinate work across multiple groups.

• The ability to be highly motivated, ambitious, goal oriented, and to actively focus on solving problems both as part of a team and individually.

• Proficient verbal and written communication skills to be effective.

• Validated ability to manage and lead projects effectively to meet deadlines and work independently with minimal supervision.

**Education**

M.S. or Ph.D. in engineering or relevant sciences (i.e., Physics, Optics, etc.) is required.

We recruit, hire, train, promote, discipline and provide other conditions of employment without regard to a person's race, color, religion, sex, age, national origin, disability, sexual orientation, gender identity and expression, pregnancy, veteran's status, or other classifications protected under law. This includes providing reasonable accommodation for team members' disabilities or religious beliefs and practices.

Each manager, supervisor and team member is responsible for carrying out this policy. The EEO Administrator in Human Resources is responsible for administration of this policy. The administrator will monitor compliance and is available to answer any questions on EEO matters.

To request assistance with the application process, please contact Micron’s Human Resources Department at 1-800-336-8918 (or 208-368-4748).

Keywords: Boise || Idaho (US-ID) || United States (US) || Technology Development || College || Regular || Engineering || #LI-DK1 ||