Project 1: Analysis and Design of a Buck Converter

Due: Feb. 11, 2013 (in the class)

Given the following specifications:
An input voltage of $15V < V_{in} < 20V$ and an output of $V_{out} = 10V$ over a load range of $5W < P_{out} < 200W$. Switching frequency is $f_{sw} = 500kHz$.

a) Design the inductor (L) and capacitor (C). The current ripple $\Delta i_L$ should be below 5% of the average inductor current $I_L$ at the maximum load. The steady state ripple $\Delta V_{out}$ is below 0.5 % of the steady-state value of the output voltage. For the designed L, find the value of $I_{out, crit}$ at the boundary of DCM and CCM. Plot $I_{out, crit}$ vs. $V_{in}$.

b) Determine the rated values for switch, diode, and capacitor. Research and determine a manufacturer part number for your switch, diode, and capacitor. Provide data sheets for each.

c) Analytically determine and draw the expected current and voltage waveforms for each component in your circuit at both light and heavy load.

d) Using SimPowerSystems toolbox of MATLAB/SIMULINK software, simulate the circuit under the heavy and light load conditions. Plot the voltage and current of each component over 3 switching intervals in the steady-state. Validate that the output of your simulation matches your analytical calculations in c).

e) Analytically determine the effect of the following non-idealities on each of the waveforms of your circuit.
   i) The diode has an on-state voltage drop of $V_{D_{on}}$.
   ii) The transistor has an on-state voltage drop of $V_{T_{on}}$.
   iii) Find an expression for the efficiency of the non-ideal buck converter in CCM.
   vi) Edit your simulation model you created in d) to include the non-idealities in e).

f) Assuming values of $V_{D_{on}} = 0.5V$ and $V_{T_{on}} = 0.9V$, compute the efficiency of your circuit at heavy load conditions by hand.

g) Measure the efficiency of your circuit versus load by simulation and compare with what you calculate in part f).

h) Assuming the non-ideal condition of part f), determine the start-up response with the assumption that the input voltage is fixed at a specified value in the range of $15V < V_{in} < 20V$ and D is set to give an output voltage of $V_{out} = 10V$. Analytically plot the input current and the output voltage during the start-up and compare with simulation.

Write a report that documents the results and observations from parts a-h. Make sure all plots are well labeled and that explanations contain solid analytical foundations.